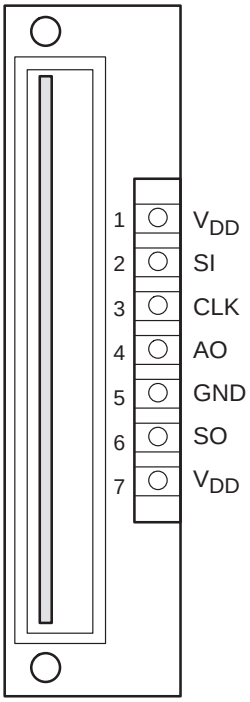
- **512 × 1 Sensor Element Organization**
- **200-Dots-per-Inch Sensor Pitch**
- **Extendable Data I/O for Expanding the Number of Arrays**
- **Analog Buffer With Sample-and-Hold Circuitry for Analog Output Over Full Clock Period**
- **500-kHz Shift-Clock Operation**
- **Single 5-V Supply**
- **Advanced LinCMOS™ Technology**

TSL218 PACKAGE
(TOP VIEW)

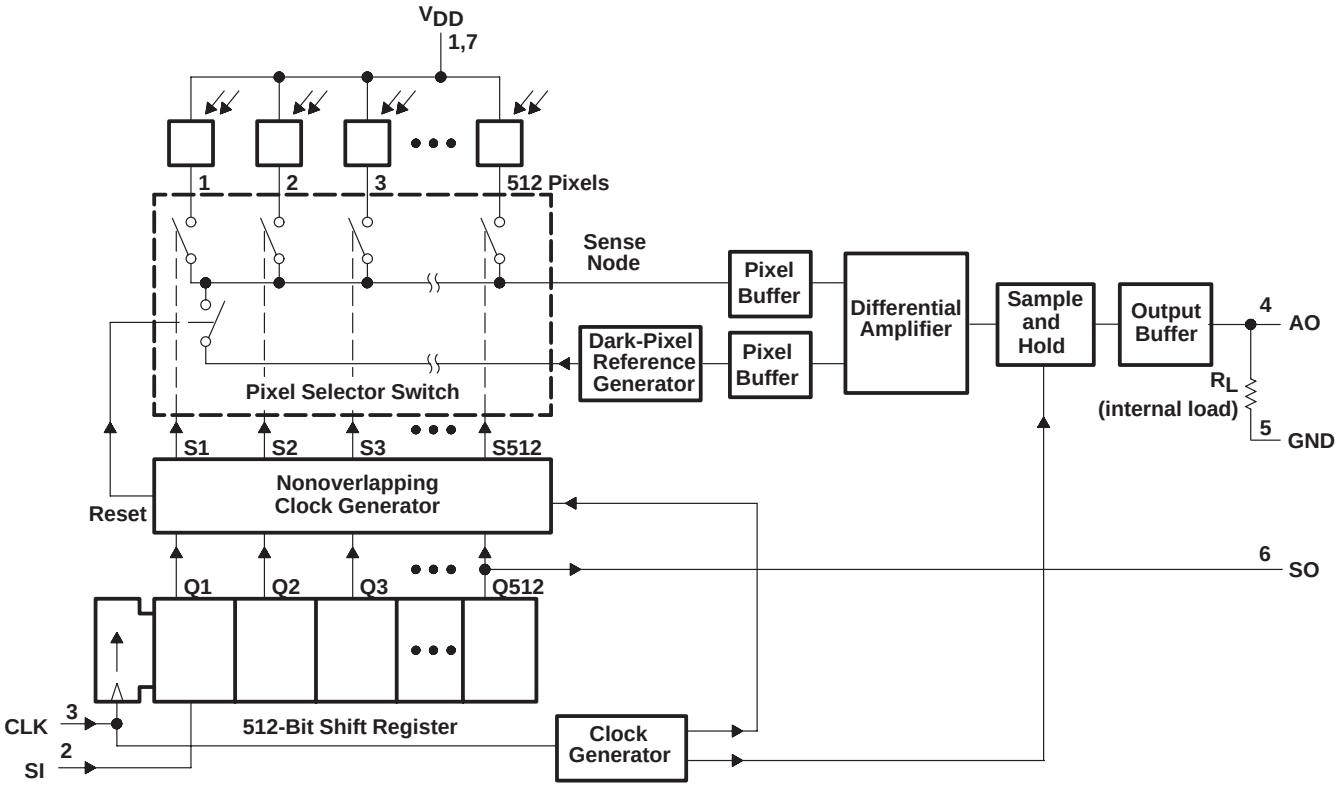


description

The TSL218 intelligent optosensor consists of eight sections of 64 charge-mode pixels arranged in a 512 × 1 linear array. Each pixel measures 120 µm × 70 µm with 125-µm center-to-center spacing. Operation is simplified by internal logic requiring only clock and serial-input pulse signals.

The TSL218 is intended for use in a wide variety of applications including contact imaging, bar-code reading, edge detection and positioning, level detection, and linear encoding.

functional block diagram



Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
AO	4	Analog output
CLK	3	Clock. The clock controls charge transfer, pixel output, and reset.
GND	5	Ground (substrate). All voltages are referenced to the substrate.
SI	2	Serial input. SI defines the start of the data-out sequence.
SO	6	Serial output. SO signals the end of the data-out sequence.
V_{DD}	1, 7	Supply voltage for both analog and digital circuits

detailed description

sensor elements

The line of sensor elements, called pixels, consists of 512 discrete photosensing areas. Light energy striking a pixel generates electron-hole pairs in the region under the pixel. The field generated by the bias on the pixel causes the electrons to collect in the element while the holes are swept into the substrate. The amount of charge accumulated in each element is directly proportional to the amount of incident light and the integration time.

device operation

Operation of the 512 × 1 array sensor is a function of two time periods—an integration period during which a charge is accumulated in the pixels and an output period during which signals are transferred to the output. The integration period is defined by the interval between the externally supplied SI pulses and includes the output period (see Figure 1). The required length of the integration period depends on the amount of incident light and the desired output-signal level.

sense node

On completion of the integration period, the charge contained in each pixel is transferred in turn to the sense node under the control of the CLK and SI signals. The signal voltage generated at this node is directly proportional to the amount of charge and inversely proportional to the capacitance of the sense node.

reset

An internal reset signal is generated by the nonoverlapping clock generator (NOCG) and occurs every clock cycle. Reset establishes a known voltage on the sense node in preparation for the next charge transfer. This voltage is used as a reference level for the differential signal amplifier.

shift register

The 512-bit shift register controls the transfer of charge from the pixels to the output stages and provides timing signals for the NOCG. The serial input (SI) signal provides the input to the shift register and is shifted under direct control of CLK out to the serial output (SO) on the 512th clock cycle. This SO pulse can then be used as the SI pulse for the next device.

The output period is initiated by the presence of the SI input pulse coincident with a rising edge of CLK (see Figures 1 and 2). The analog output voltage corresponds to the level of the first pixel after settling time (t_S) and remains constant for a minimum time (t_V). A voltage corresponding to each succeeding pixel is available at each rising edge of CLK. The output period of the device ends when it sees the rising edge of the 513th clock cycle, at which time the output assumes the high-impedance state. Once the output period has been initiated by an SI pulse, CLK must be allowed to complete 513 positive-going transitions in order to reset the internal logic to a known state. To achieve minimum integration time, the SI pulse may be present on the 514th rising clock to immediately restart the output phase.

sample-and-hold

The sample-and-hold signal generated by the NOCG holds the analog output voltage of each pixel constant until the next pixel is clocked out. The signal is sampled while CLK is high and held constant while CLK is low.

nonoverlapping clock generators

The NOCG circuitry provides internal control signals for the sensor, including reset and pixel-charge sensing. The signals are synchronous and are controlled by the outputs of the shift register.

initialization

Initialization of the sensor elements may be necessary on power up or during operation after any period of CLK or SI inactivity exceeding the integration time. The initialization phase consists of 12 to 15 consecutively performed output cycles and clears the pixels of any charge that may have accumulated during the inactive period.

multiple-unit operation

Multiple-sensor devices can be connected together in a serial or parallel configuration. The serial connection is accomplished by connecting analog outputs (AO) together and connecting the SO output of each sensor device to the SI input of the next device. The SI signal is applied to only the first device. Each succeeding device receives its SI input from the SO output of the preceding device. For m-cascaded devices, the SI pulse is applied to the first device after every m × 512th positive-going CLK transition. A common clock signal is applied to all the devices simultaneously. Parallel operation of multiple devices is accomplished by supplying CLK and SI signals to all the devices simultaneously. The output of each device is then separately used for processing.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.5 V to 7 V
Digital output voltage range, V_O . . . . . –0.5 V to V_{DD} + 0.5 V
Digital output current, I_O . . . . . 3 mA
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Wavelength of light source, λ	565		700	nm
Clock frequency, f_{clock}	10		500	kHz
Sensor integration time, t_{int} (see Figures 1 and 2)	1.028	5		ms
Pulse duration, CLK low, $t_{w(CLKL)}$	1			μs
Setup time, SI before CLK↑, $t_{su(SI)}$ (see Figure 2)	50			ns
Hold time, SI after CLK↑, $t_{h(SI)}$ (see Note 1) (see Figure 2)	50			ns
Operating free-air temperature, T_A	0		70	°C

NOTE 1: SI must go low before the rising edge of the next clock pulse.

electrical characteristics at f_{clock} = 200 kHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 660 nm, t_{int} = 5 ms, E_e = 20 μW/cm^2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog output voltage (white, average over 512 pixels)		1.75	2.2		V
Analog output voltage (dark, each pixel)			0.25	0.4	V
Dispersion of analog output voltage	See Note 2			±20%	
Linearity of analog output voltage	See Note 3	0.85		1.15	
Analog output saturation	E_e = 60 μW/cm^2	3	3.4		V
Supply current			16	24	mA
High-level input current	$V_I = V_{DD}$			0.5	μA
Low-level input current	V_I = 0			0.5	μA
Input capacitance			5		pF

NOTES: 2. Dispersion is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
3. Linearity of analog-output voltage is calculated by averaging over 512 pixels and measuring the maximum deviation of the voltage at 3 ms and 4.5 ms from a line drawn between the voltage at 3 ms and 6 ms.

operating characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(SO)}$	Rise time, SO	C_L = 30 pF		25		ns
$t_{f(SO)}$	Fall time, SO			25		ns
$t_{pd(SO)}$	Propagation delay time, SO			70		ns
t_S	Settling time				1	µs
t_V	Valid time				1/2 f_{clock}	µs

PARAMETER MEASUREMENT INFORMATION

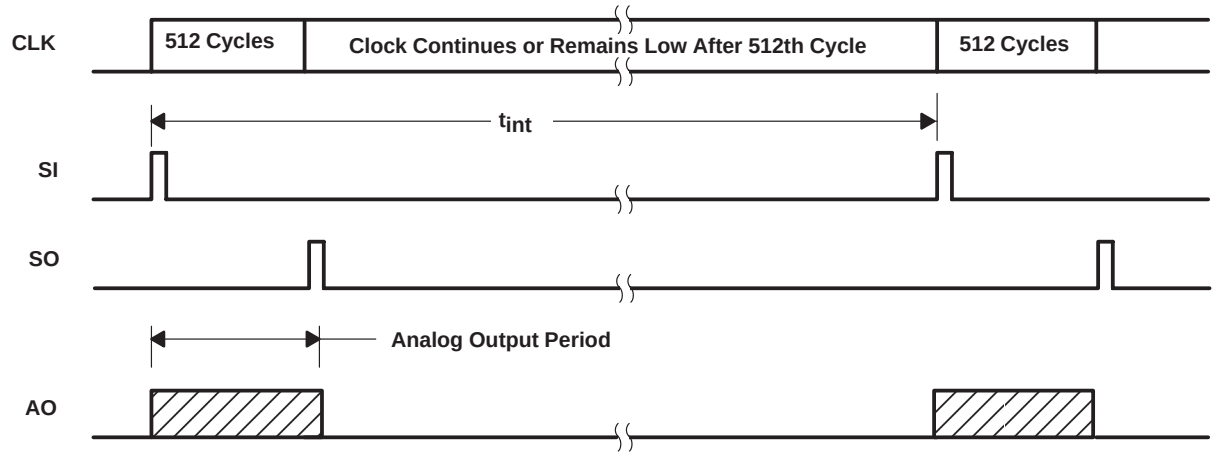


Figure 1. Timing Diagram

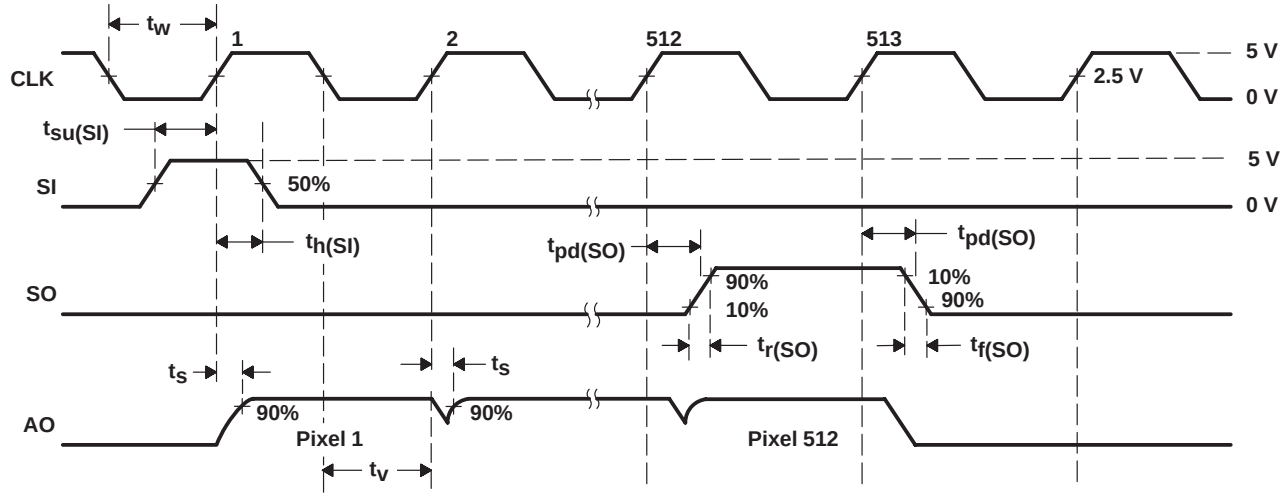
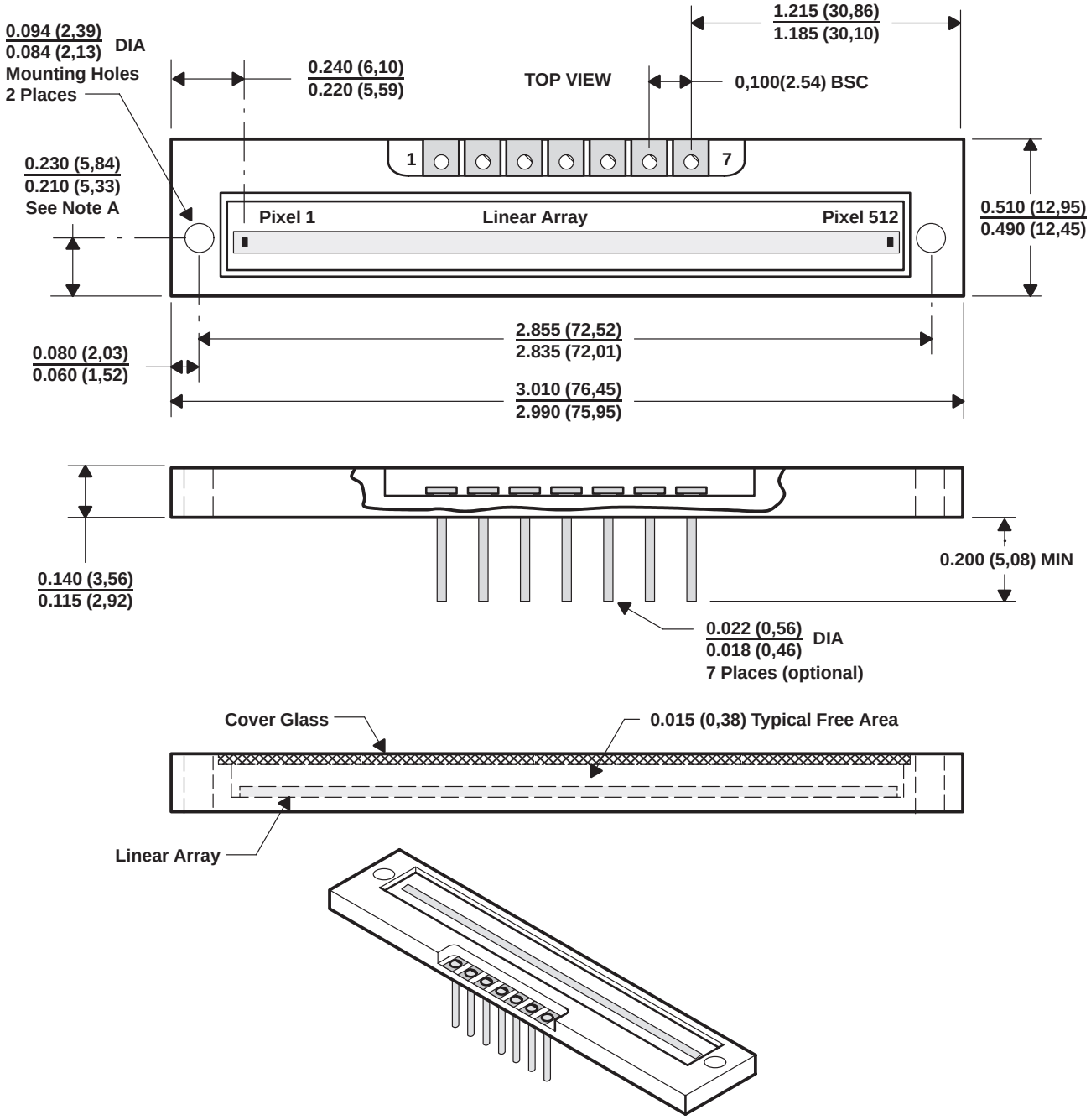


Figure 2. Operational Waveforms

APPLICATION INFORMATION

The device consists of eight cascaded 64 × 1 arrays mounted in a single, glass-epoxy substrate with a cover glass for protection. Mounting holes are standard and pins are optional.



NOTES: A. All linear dimensions are in inches(millimeters).
B. This drawing is subject to change without notice.
C. The pixel centers are in line with center line of mounting holes.

Figure 3. TSL218 Mechanical Specifications

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