

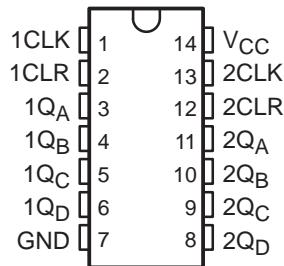
- Dual 4-Bit Binary Counters With Individual Clocks
- Direct Clear for Each 4-Bit Counter
- Can Significantly Improve System Densities by Reducing Counter Package Count by 50 Percent
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

### description

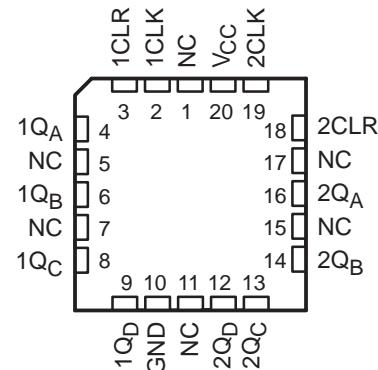
The 'HC393 contain eight flip-flops and additional gating to implement two individual 4-bit counters in a single package. The 'HC393 comprise two independent 4-bit binary counters, each having a clear (CLR) and a clock (CLK) input. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The 'HC393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

The SN54HC393 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC393 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54HC393 . . . J OR W PACKAGE  
SN74HC393 . . . D, DB, OR N PACKAGE  
(TOP VIEW)



SN54HC393 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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 **TEXAS  
INSTRUMENTS**

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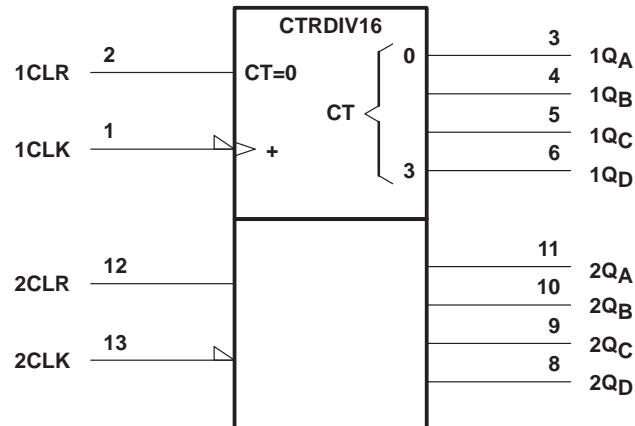
# SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

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FUNCTION TABLE COUNT SEQUENCE  
(each counter)

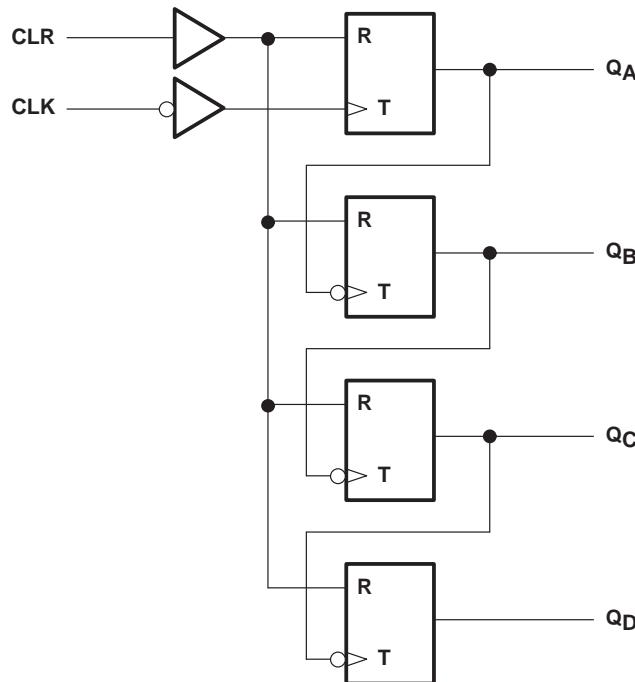
COUNT	OUTPUTS			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, DB, J, N, and W packages.

## logic diagram, each counter (positive logic)



absolute maximum ratings over operating free-air temperature range†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

# SN54HC393, SN74HC393 DUAL 4-BIT BINARY COUNTERS

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## recommended operating conditions

			SN54HC393			SN74HC393			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5			1.5			V
		V <sub>CC</sub> = 4.5 V	3.15			3.15			
		V <sub>CC</sub> = 6 V	4.2			4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0	0.5		0	0.5		V
		V <sub>CC</sub> = 4.5 V	0	1.35		0	1.35		
		V <sub>CC</sub> = 6 V	0	1.8		0	1.8		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
t <sub>t</sub> <sup>†</sup>	Input transition (rise and fall) time	V <sub>CC</sub> = 2 V	0	1000		0	1000		ns
		V <sub>CC</sub> = 4.5 V	0	500		0	500		
		V <sub>CC</sub> = 6 V	0	400		0	400		
T <sub>A</sub>	Operating free-air temperature		-55		125	-40		85	°C

<sup>†</sup>If this device is used in the threshold region (from V<sub>IL</sub>max = 0.5 V to V<sub>IH</sub>min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>t</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC393		SN74HC393		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998	1.9		1.9		V
			4.5 V	4.4	4.499	4.4		4.4		
			6 V	5.9	5.999	5.9		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7		3.84		V
			6 V	5.48	5.8	5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.002	0.1	0.1		0.1		V
			4.5 V	0.001	0.1	0.1		0.1		
			6 V	0.001	0.1	0.1		0.1		
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26	0.4		0.33	V
			6 V		0.15	0.26	0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8		160		80	μA
C <sub>i</sub>		2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC393		SN74HC393		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency			2 V	0	6	0	4.2	0	5	MHz
	4.5 V	0	31	0	21	0	25				
	6 V	0	36	0	25	0	28				
t <sub>w</sub>	Pulse duration	CLK high or low	2 V	80		120		100		ns	
			4.5 V	16		24		20			
			6 V	14		20		18			
		CLR high	2 V	80		120		100			
			4.5 V	16		24		20			
			6 V	14		20		18			
t <sub>su</sub>	Setup time, CLR inactive	2 V	25		25		25			ns	
		4.5 V	5		5		5				
		6 V	5		5		5				

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC393		SN74HC393		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>	CLK	QA	2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		28		
t <sub>pd</sub>	CLK	QA	2 V	50	120		180		150		ns
			4.5 V	15	24		36		30		
			6 V	13	20		31		26		
		QB	2 V	72	190		285		240		
			4.5 V	22	38		57		47		
			6 V	18	32		48		40		
		QC	2 V	91	240		360		300		
			4.5 V	28	48		72		60		
			6 V	22	41		61		51		
		QD	2 V	100	290		430		360		
			4.5 V	32	58		87		72		
			6 V	24	50		74		62		
t <sub>PHL</sub>	CLR	Any	2 V	45	165		250		205		ns
			4.5 V	17	33		49		41		
			6 V	14	28		42		35		
t <sub>t</sub>		Any	2 V	28	75		110		95		ns
			4.5 V	8	15		22		19		
			6 V	6	13		19		16		

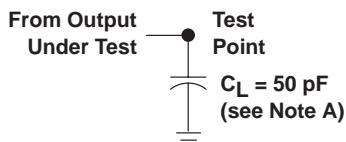
operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per counter	No load	40	pF

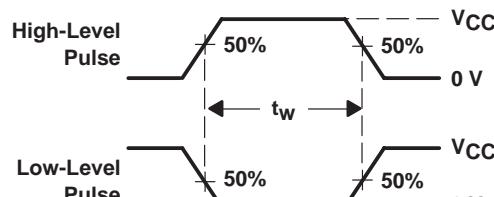
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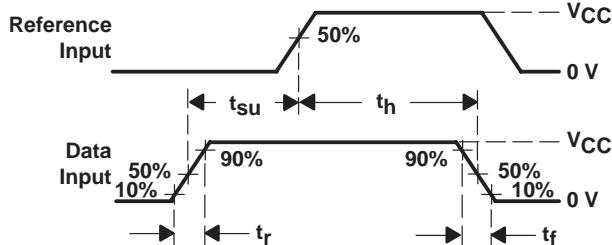
## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

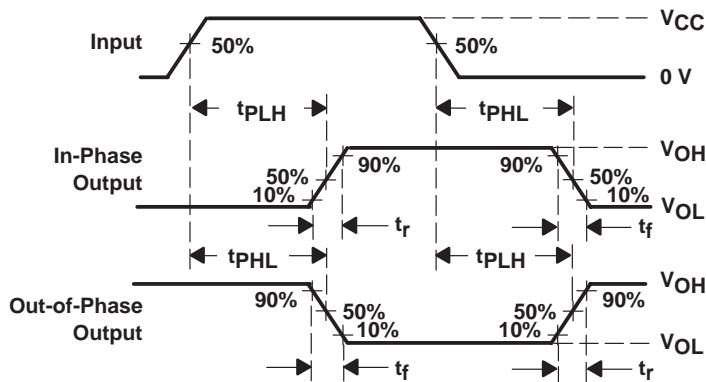


VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS

SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES:

- $C_L$  includes probe and test-fixture capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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