WJA1505

+5V Active-Bias InGaP HBT Gain Block

Product Features

- Cascadable gain block
- 50 – 1000 MHz
- 19 dB Gain
- +19 dBm P1dB
- +37 dBm OIP3
- +51dBm OIP2
- Operates from +5V @ 65mA
- Robust 1000V ESD, Class 1C
- RoHS-compliant SOT-89 package

Applications

- IF Amplifier
- VHF/UHF Transmission
- Wireless Infrastructure
- General Purpose
- CATV / FTTH

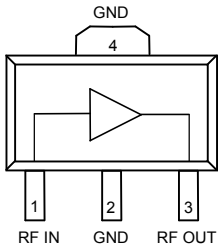
Product Description

The WJA1505 is a cascadable gain block that offers high linearity in a low-cost surface-mount package. At 200 MHz, the WJA1505 typically provides 19 dB gain, +37 dBm OIP3, and +19 dBm P1dB. The device is housed in a RoHS-compliant SOT-89 industry-standard SMT package using a NiPdAu plating to eliminate the possibility of tin whiskering.

The WJA1505 consists of Darlington pair amplifiers using a high reliability InGaP/GaAs HBT process technology. The MMIC amplifier is internally matched to 50Ω and only requires DC-blocking capacitors and a bias inductor for operation. An internal active bias is designed to enable stable performance over temperature. A dropping bias resistor is not required allowing the device to be biased directly from +5V supply voltage.

The amplifier is targeted for high performance IF applications in existing and next generation wireless technologies. The WJA1505 is ideal for general purpose applications such as LO buffering, IF amplification and pre-driver stages within the 50 to 1000 MHz frequency range.

Functional Diagram



Function	Pin No.
Input	1
Output/Bias	3
Ground	2, 4

Specifications (1)

Parameter	Units	Min	Typ	Max
Operational Bandwidth	MHz	50		1000
Test Frequency	MHz		200	
Gain	dB	17.7	19.3	20.7
Input Return Loss	dB		19	
Output Return Loss	dB		20	
Output P1dB	dBm		+19.3	
Output IP3 (2)	dBm	+33	+36.6	
Output IP2	dBm		+51.0	
Noise Figure	dB		4.7	
Device Voltage	V		5	
Device Current	mA	55	65	75

1. Test conditions: 25 ºC, Supply Voltage = +5 V, 50 Ω System. S-parameters and 3OIP measured at device pins. All other specifications measured on evaluation board.
2. 3OIP measured with two tones at an output power of +6 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.

Typical Performance (3)

Parameter	Units	Typical				
Frequency	MHz	70	170	240	500	900
S21	dB	19.4	19.2	19.0	18.5	17.3
S11	dB	-15	-18	-19	-18	-14
S22	dB	-22	-22	-20	-15	-10
Output P1dB	dBm	+19.1	+19.2	+19.2	+18.9	+17.7
Output IP3 (2)	dBm	+35.8	+36.7	+36.9	+37.7	+33.6
Output IP2	dBm	+50.7	+51.4	+51.0	+54.1	+52.9
Noise Figure	dB	4.6	4.7	4.7	4.9	5.5

3. Listed typical performance parameters measured on evaluation board

Not Recommended For New Designs

Recommended replacement parts:

TQP3M9008

Absolute Maximum Rating

Parameter	Rating
Storage Temperature	-55 to +150 °C
Supply Voltage	+6.5 V
Input Power	+24 dBm
θ_{jc} (junction to paddle)	83.8 °C / W
Maximum Junction Temperature	150 °C

Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

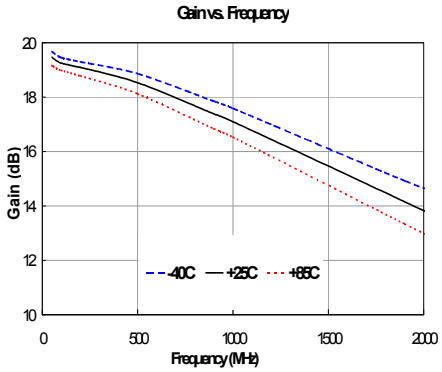
Part No.	Description
WJA1505	+5V Active Bias InGaP HBT Gain Block (lead-free/green/RoHS-compliant SOT-89 Package)

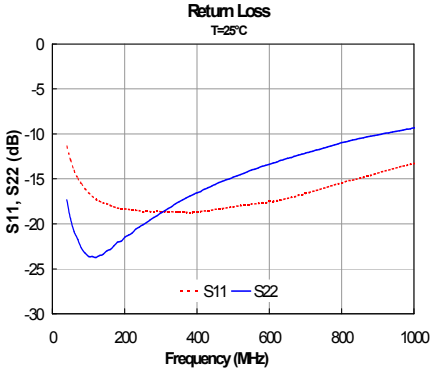
Standard tape / reel size = 1000 pieces on a 7″ reel

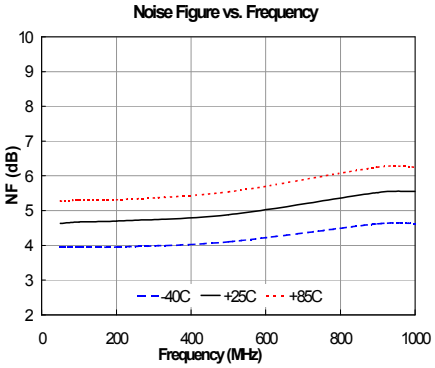
Specifications and information are subject to change without notice

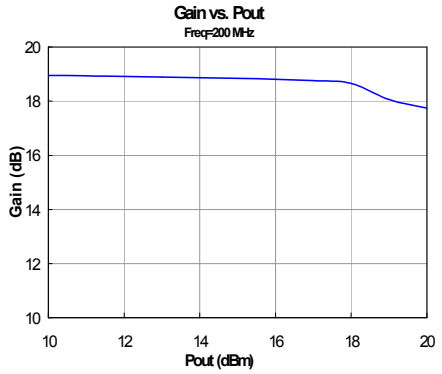
Typical Evaluation Board RF Performance Plots
Supply Bias = +5V, I_{cc} = 65 mA

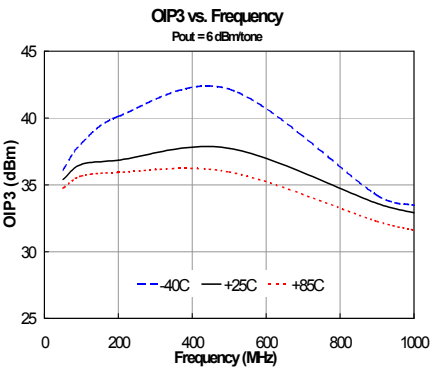
1. Test conditions: T = 25 ºC, Supply Voltage = +5 V, Icc = 65 mA typical, 50 Ω System.
2. 3OIP measured with two tones at an output power of 6 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using a 2:1 rule.

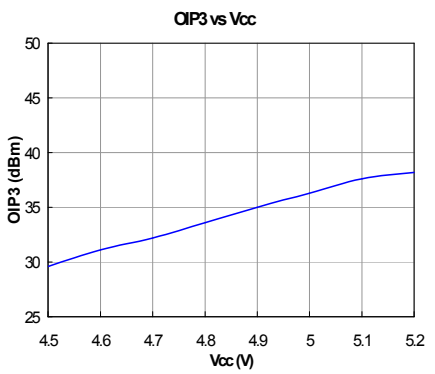


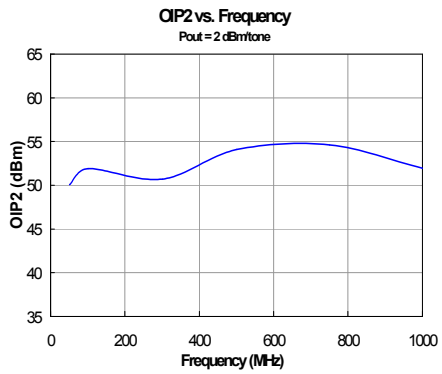


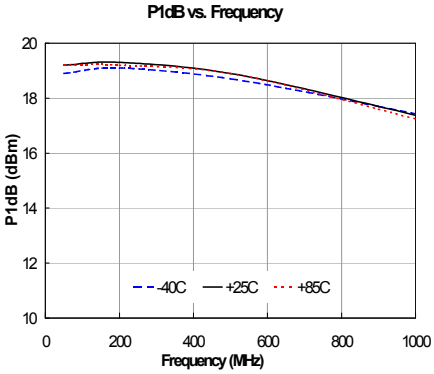


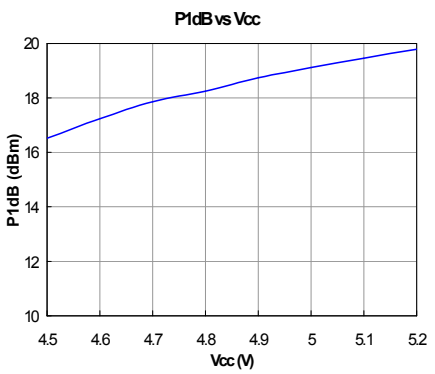


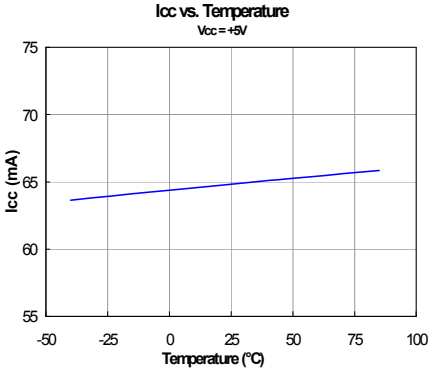


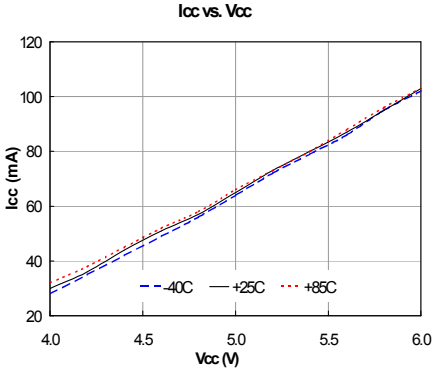




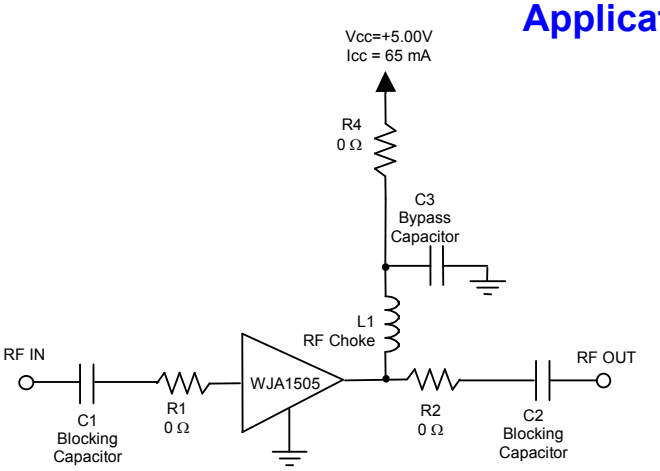


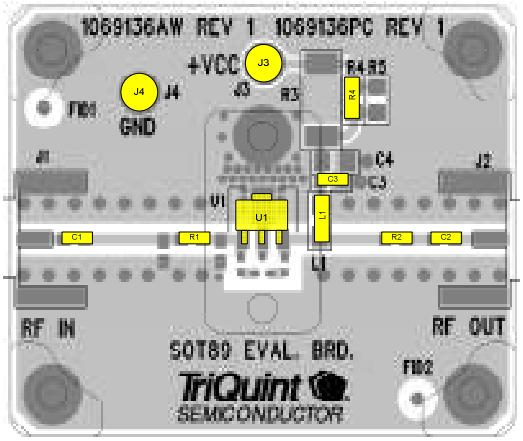






Application Circuit





Recommended Component Values [1]

Ref. Name	Value / Type	Size
L1	470 nH ferrite core wire wound inductor [2]	0805
C1, C2	1000 pF NPO chip capacitor	0603
C3	0.018 µF chip capacitor	0603
R1, R2, R4	0 Ω [3]	0603
C4, R3, R5	Do Not Place [3]	

1. The listed values are contained on the evaluation board to achieve optimal broadband performance
2. For lower cost and performance (100 – 1000 MHz) option use 470 nH air core wire wound inductor.
3. Place holders for the 0Ω resistors and "Do Not Place" references are not needed for final design.

Typical Device Data

S-Parameters (V_{device} = +5V, I_{CC} = 65 mA, T = 25 °C, calibrated to device leads)

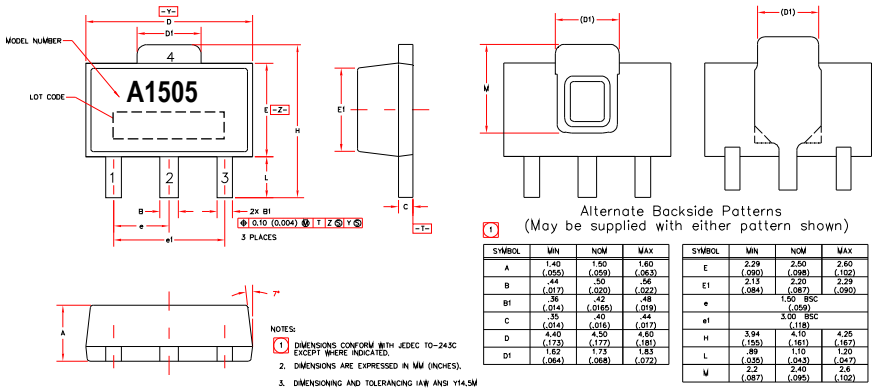
Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
10	-12.67	-58.61	21.75	167.36	-24.85	17.99	-8.64	-37.42
50	-18.42	-130.48	19.70	169.11	-22.91	3.86	-17.79	-54.38
100	-19.18	-148.50	19.51	168.07	-22.83	0.52	-19.90	-52.53
150	-19.47	-152.58	19.44	164.59	-22.82	-1.55	-19.93	-55.18
200	-19.15	-153.65	19.33	160.75	-22.78	-3.28	-19.73	-61.49
250	-19.00	-152.93	19.29	157.20	-22.76	-4.67	-19.03	-65.79
300	-18.57	-151.79	19.24	153.26	-22.81	-6.19	-18.33	-70.81
350	-18.14	-149.00	19.22	148.84	-22.83	-7.01	-17.58	-74.98
400	-17.86	-147.88	19.15	144.57	-22.81	-8.91	-17.03	-78.76
450	-17.23	-144.33	19.08	140.96	-22.81	-9.47	-16.18	-83.41
500	-16.91	-144.72	19.00	136.61	-22.72	-11.09	-15.86	-86.26
550	-16.57	-143.95	18.91	132.60	-22.84	-12.81	-15.28	-90.85
600	-16.12	-142.62	18.80	128.59	-22.87	-14.21	-14.83	-93.72
650	-15.74	-140.46	18.73	124.73	-22.83	-15.17	-14.31	-96.80
700	-15.35	-139.57	18.59	120.30	-22.88	-16.10	-13.66	-100.65
750	-15.02	-138.44	18.50	117.30	-22.83	-18.04	-13.25	-103.10
800	-14.78	-138.82	18.37	112.84	-22.81	-19.26	-12.88	-106.20
850	-14.49	-137.73	18.29	108.55	-22.88	-20.49	-12.32	-109.14
900	-14.27	-136.56	18.12	105.01	-22.87	-21.55	-11.80	-112.10
950	-13.99	-135.73	18.07	101.23	-22.85	-23.17	-11.34	-114.90
1000	-13.92	-135.99	17.93	97.14	-22.96	-24.51	-10.99	-117.96
1050	-13.67	-135.66	17.75	93.36	-22.90	-25.55	-10.55	-120.27
1100	-13.31	-135.44	17.58	89.63	-22.87	-27.17	-10.16	-123.01
1150	-13.11	-134.80	17.50	85.77	-22.91	-28.65	-9.76	-125.23
1200	-12.91	-134.82	17.33	81.40	-23.05	-29.42	-9.48	-127.90

Device S-parameters are available for download from the website at: http://www.triquint.com

Mechanical Information

This package is lead-free/Green/RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the leads is NiPdAu.

Outline Drawing

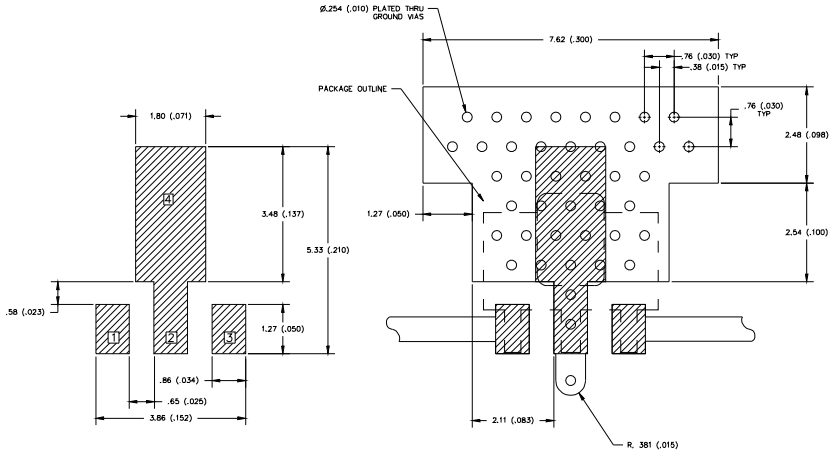


SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e		1.50 BSC (.059)	
e1		3.00 BSC (.118)	
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

NOTES:
1. DIMENSIONS CONFORM WITH JEDEC TO-243C EXCEPT WHERE INDICATED.
2. DIMENSIONS ARE EXPRESSED IN MM (INCHES).
3. DIMENSIONING AND TOLERANCING IAW ANSI Y14.5M

Land Pattern



Product Marking

The WJA1505 will be marked with an "A1505" designator with an alphanumeric lot code marked below the part designator.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.

MSL / ESD Rating

Caution! ESD sensitive device.

ESD Rating: Class 1C
Value: Passes ≥ 1000V min.
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 1000V min.
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3 at +260 °C convection reflow
Standard: JEDEC Standard J-STD-020

Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz. Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.