74AUP2G07

Low-power dual buffer with open-drain output Rev. 7 — 29 November 2012

Product data sheet

General description 1.

The 74AUP2G07 provides two non-inverting buffers with open-drain output. The output of the device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Schmitt-trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. **Features and benefits**

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
 - ◆ JESD8-12 (0.8 V to 1.3 V)
 - ◆ JESD8-11 (0.9 V to 1.65 V)
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 5000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Low static-power consumption; $I_{CC} = 0.9 \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



Low-power dual buffer with open-drain output

3. Ordering information

Table 1. Ordering information

Type number	Package							
	Temperature range	Name	Description	Version				
74AUP2G07GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363				
74AUP2G07GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1.45 \times 0.5 mm	SOT886				
74AUP2G07GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1 \times 0.5 mm	SOT891				
74AUP2G07GN	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115				
74AUP2G07GS	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 \times 1.0 \times 0.35 mm	SOT1202				

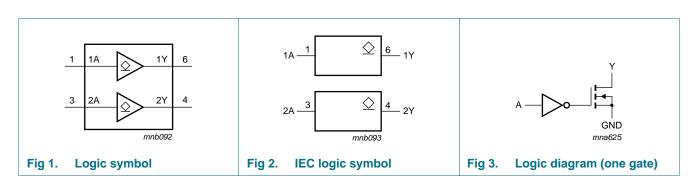
4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74AUP2G07GW	p7
74AUP2G07GM	p7
74AUP2G07GF	p7
74AUP2G07GN	p7
74AUP2G07GS	p7

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

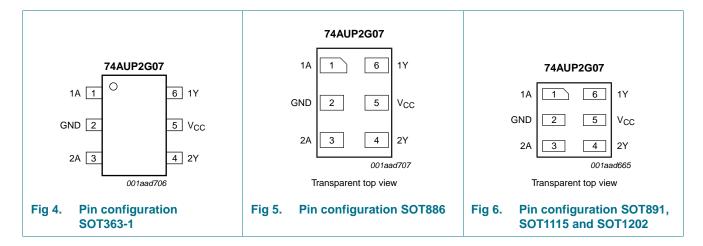
5. Functional diagram



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6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

	The state of the s	
Symbol	Pin	Description
1A	1	data input
GND	2	ground (0 V)
2A	3	data input
2Y	4	data output
V _{CC}	5	supply voltage
1Y	6	data output

7. Functional description

Table 4. Function table[1]

Input	Output
nA	nY
L	L
H	Z

- [1] H = HIGH voltage level;
 - L = LOW voltage level;
 - Z = high-impedance OFF state.

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
VI	input voltage		[<u>1</u>] -0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
Vo	output voltage	Active mode and Power-down mode	[<u>1</u>] -0.5	+4.6	V
I _O	output current	$V_O = 0 V \text{ to } V_{CC}$	-	20	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[2] _	250	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		8.0	3.6	V
V_{I}	input voltage		0	3.6	V
Vo	output voltage	Active mode and Power-down mode	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 0.8 V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$T_{amb} = 2$	25 °C					
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	-	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.9	V

74AUP2G07

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^[2] For SC-88 package: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K. For XSON6 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

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Table 7. Static characteristics ...continued
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Uni
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μ A; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		$I_O = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}$; $V_{CC} = 1.4 \text{ V}$	-	-	0.31	V
		$I_O = 1.9 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$	-	-	0.31	V
		$I_{O} = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.31	V
		$I_{O} = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.44	V
		$I_{O} = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.31	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.44	V
I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μΑ
OZ	OFF-state output current	$V_I = V_{IH}$; $V_O = 0 \text{ V to } 3.6 \text{ V}$; $V_{CC} = 0 \text{ V}$ to 3.6 V	-	-	±0.1	μΑ
OFF	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.2	μΑ
Δl _{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.2	μΑ
CC	supply current	$V_I = GND \text{ or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.5	μΑ
∆l _{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	40	μΑ
Cı	input capacitance	V_{CC} = 0 V to 3.6 V; V_{I} = GND or V_{CC}	-	0.7	-	рF
Co	output capacitance	$V_O = GND; V_{CC} = 0 V$	-	0.9	-	рF
Γ _{amb} = –	40 °C to +85 °C					
/ _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		V _{CC} = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.6	-	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
√ _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		V _{CC} = 0.9 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
/ _{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20 \mu A$; $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}$; $V_{CC} = 1.4 \text{ V}$	-	-	0.37	V
		$I_O = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.35	V
		$I_O = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.33	V
		$I_O = 3.1 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$	-	-	0.45	٧
		$I_O = 2.7 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	-	-	0.33	٧
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.45	٧
I	input leakage current	$V_1 = GND \text{ to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.5	μΑ
oz	OFF-state output current	$V_I = V_{IH}$; $V_O = 0 \text{ V to } 3.6 \text{ V}$; $V_{CC} = 0 \text{ V}$ to 3.6 V	-	-	±0.5	μΑ

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 Table 7.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{OFF}	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.5	μΑ
ΔI_{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.6	μА
I _{CC}	supply current	$V_I = GND \text{ or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.9	μΑ
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	50	μΑ
T _{amb} = -	40 °C to +125 °C					
V_{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	$0.75 \times V_{CC}$	-	-	V
		V _{CC} = 0.9 V to 1.95 V	$0.70 \times V_{CC}$	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	$0.25 \times V_{CC}$	V
		V _{CC} = 0.9 V to 1.95 V	-	-	$0.30 \times V_{CC}$	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μ A; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		$I_O = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.33 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.41	V
		$I_O = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.39	V
		$I_O = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.36	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.50	V
		$I_O = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.50	V
I _I	input leakage current	$V_I = GND$ to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.75	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$; $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V to 3.6 V	-	-	±0.75	μΑ
I _{OFF}	power-off leakage current	V_I or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.75	μΑ
ΔI_{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.75	μΑ
I _{CC}	supply current	V_I = GND or V_{CC} ; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	1.4	μΑ
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	75	μΑ

Low-power dual buffer with open-drain output

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions		25 °C		–40 °C to +125 °C			Unit
				Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
$C_L = 5 pl$	F		•	'	'				'
t _{pd}	propagation delay	nA to nY; see Figure 7							
	ри 1 1 3 ,	$V_{CC} = 0.8 V$	-	11.6	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	2.1	4.1	7.5	1.7	9.1	10.0	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	1.6	3.0	5.1	1.3	6.1	6.7	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.6	2.7	4.0	1.2	5.0	5.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.1	2.1	3.2	0.9	4.0	4.4	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.4	2.2	2.8	1.1	3.3	3.6	ns
C _L = 10	pF								
t _{pd}	propagation delay	nA to nY; see Figure 7							
		$V_{CC} = 0.8 V$	-	14.7	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	3.0	5.1	9.0	2.4	11.2	12.3	ns
		V _{CC} = 1.4 V to 1.6 V	2.3	3.8	6.1	2.0	7.4	8.1	ns
		V _{CC} = 1.65 V to 1.95 V	2.4	3.6	4.8	1.8	6.1	6.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	2.8	3.8	1.3	4.8	5.3	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.2	3.1	4.2	1.6	4.5	5.0	ns
C _L = 15	pF								
t _{pd}	propagation delay	nA to nY; see Figure 7							
		$V_{CC} = 0.8 V$	-	17.7	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	3.5	6.1	10.4	3.2	13.1	14.5	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	3.0	4.5	6.8	2.6	8.6	9.4	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2.8	4.4	6.7	2.2	7.8	8.6	ns
		V_{CC} = 2.3 V to 2.7 V	2.4	3.4	4.5	1.9	5.3	5.8	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.2	4.0	5.7	1.9	6.1	6.7	ns
$C_L = 30$	pF								
t_{pd}	propagation delay	nA to nY; see Figure 7							
		$V_{CC} = 0.8 V$	-	26.7	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	4.8	9.0	15.6	4.3	18.8	20.7	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	4.1	6.7	9.4	3.7	11.8	13.0	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	3.8	6.8	9.7	3.2	11.0	12.1	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	3.7	5.2	6.7	3.0	7.1	7.8	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.6	6.4	9.7	2.8	10.4	11.4	ns

Low-power dual buffer with open-drain output

 Table 8.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions		25 °C		25 °C —40 °C to +125 °C			125 °C	Unit
				Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)		
$C_L = 5 pl$	F, 10 pF, 15 pF and	30 pF		'						
C_{PD}	C _{PD} power dissipation	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	[3][4]							
	capacitance	$V_{CC} = 0.8 \text{ V}$	-	0.5	-	-	-	-	pF	
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	-	0.6	-	-	-	-	pF	
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	-	0.6	-	-	-	-	pF	
	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	0.7	-	-	-	-	pF		
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	0.9	-	-	-	-	pF	
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	1.2	-	-	-	-	pF	

- [1] All typical values are measured at nominal V_{CC} .
- [2] t_{pd} is the same as t_{PZL} and t_{PLZ} .
- [3] All specified values are the average typical values over all stated loads.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N$ where:

f_i = input frequency in MHz;

V_{CC} = supply voltage in V;

N = number of inputs switching.

12. Waveforms

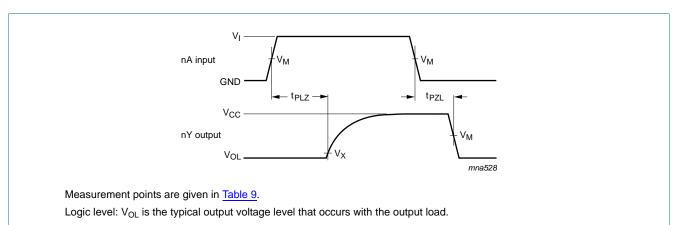
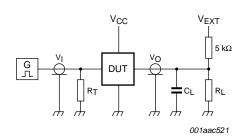


Fig 7. The data input (nA) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output			
V _{CC}	V _M	V _M	V _X		
0.8 V to 1.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V _{OL} + 0.1 V		
1.65 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V _{OL} + 0.15 V		
3.0 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V _{OL} + 0.3 V		

Low-power dual buffer with open-drain output



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Supply voltage Input		Load		V _{EXT}		
V _{CC}	VI	t _r , t _f	CL	R _L [1]	t_{PLH} , t_{PHL}	t_{PZH} , t_{PHZ}	t_{PZL},t_{PLZ}
0.8 V to 3.6 V	V_{CC}	\leq 3 ns	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	$2\times V_{CC}$

^[1] For measuring enable and disable times R_L = 5 k Ω , for measuring propagation delays, set-up and hold times and pulse width R_L = 1 M Ω .

Low-power dual buffer with open-drain output

13. Package outline

Plastic surface-mounted package; 6 leads

SOT363

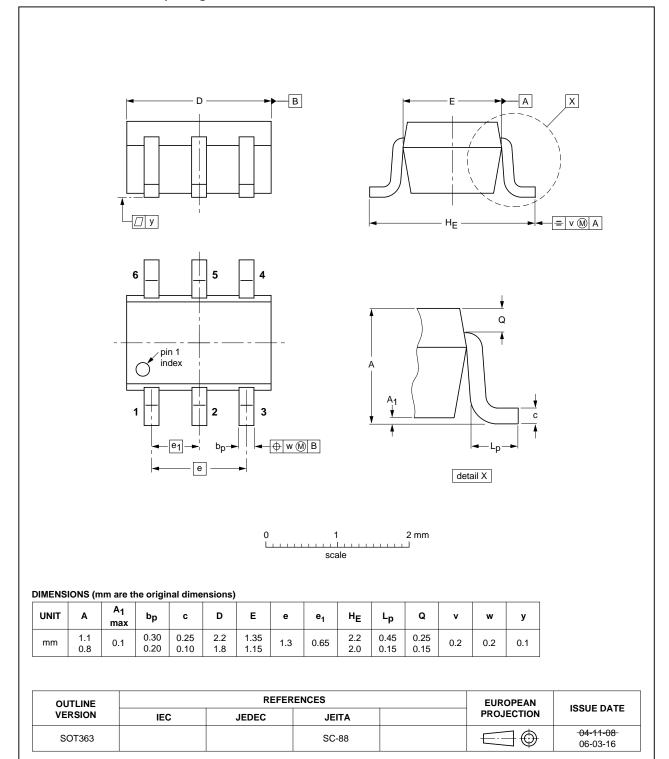


Fig 9. Package outline SOT363 (SC-88)

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Low-power dual buffer with open-drain output

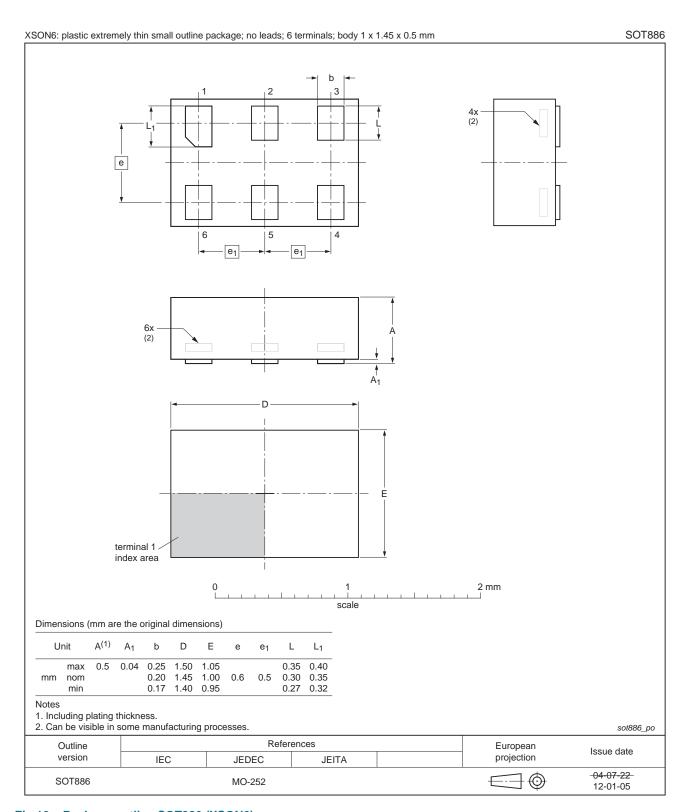


Fig 10. Package outline SOT886 (XSON6)

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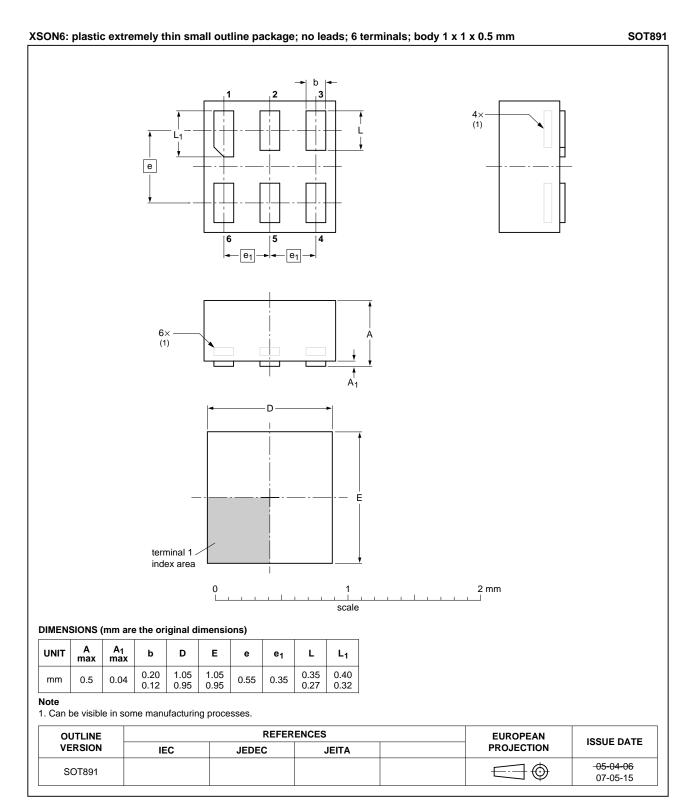


Fig 11. Package outline SOT891 (XSON6)

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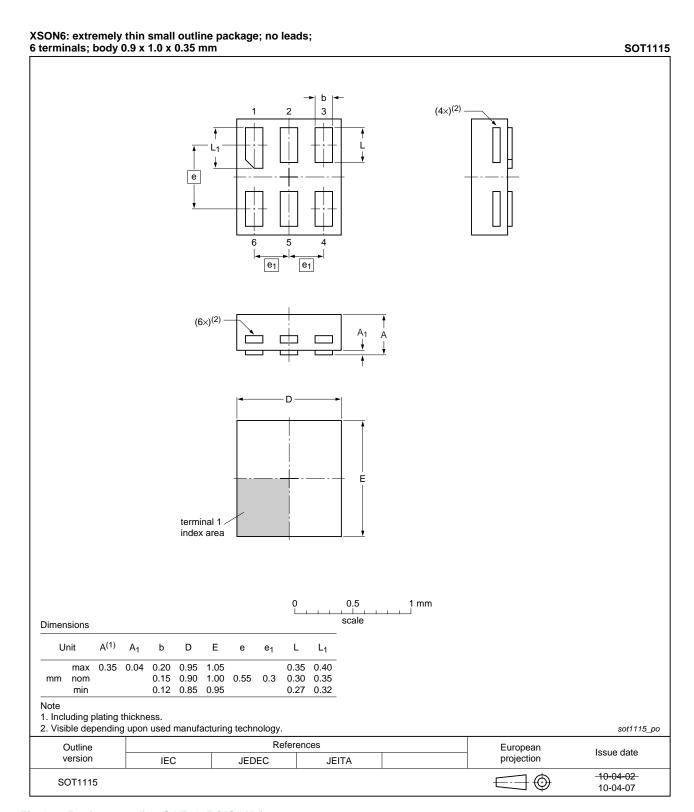


Fig 12. Package outline SOT1115 (XSON6)

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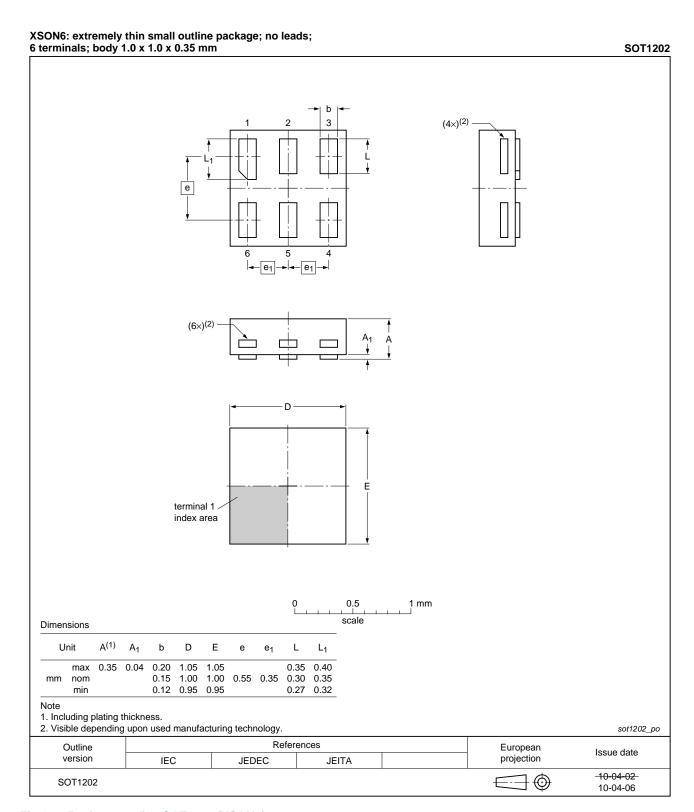


Fig 13. Package outline SOT1202 (XSON6)

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14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

15. Revision history

Table 12. Revision history

	•			
Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G07 v.7	20121129	Product data sheet	-	74AUP2G07 v.6
Modifications:	 Package ou 	tline drawing of SOT886 (F	igure 10) modified.	
74AUP2G07 v.6	20111202	Product data sheet	-	74AUP2G07 v.5
74AUP2G07 v.5	20100909	Product data sheet	-	74AUP2G07 v.4
74AUP2G07 v.4	20090611	Product data sheet	-	74AUP2G07 v.3
74AUP2G07 v.3	20071016	Product data sheet	-	74AUP2G07 v.2
74AUP2G07 v.2	20070612	Product data sheet	-	74AUP2G07 v.1
74AUP2G07 v.1	20061121	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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