

# IRFR/U120N

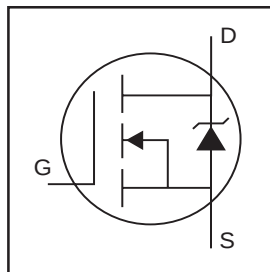
HEXFET® Power MOSFET

- Surface Mount (IRFR120N)
- Straight Lead (IRFU120N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

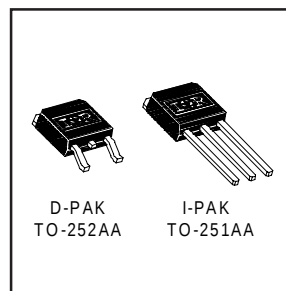
The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



$$V_{DS} = 100V$$

$$R_{DS(on)} = 0.21\Omega$$

$$I_D = 9.4A$$



## Absolute Maximum Ratings

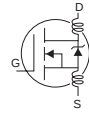
|                           | Parameter                                | Max.                   | Units |
|---------------------------|------------------------------------------|------------------------|-------|
| $I_D @ T_C = 25^\circ C$  | Continuous Drain Current, $V_{GS} @ 10V$ | 9.4                    | A     |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 6.6                    |       |
| $I_{DM}$                  | Pulsed Drain Current ①⑥                  | 38                     |       |
| $P_D @ T_C = 25^\circ C$  | Power Dissipation                        | 48                     | W     |
|                           | Linear Derating Factor                   | 0.32                   | W/°C  |
| $V_{GS}$                  | Gate-to-Source Voltage                   | $\pm 20$               | V     |
| $E_{AS}$                  | Single Pulse Avalanche Energy②⑥          | 91                     | mJ    |
| $I_{AR}$                  | Avalanche Current①⑥                      | 5.7                    | A     |
| $E_{AR}$                  | Repetitive Avalanche Energy①⑥            | 4.8                    | mJ    |
| $dv/dt$                   | Peak Diode Recovery $dv/dt$ ③            | 5.0                    | V/ns  |
| $T_J$                     | Operating Junction and                   | -55 to + 175           | °C    |
| $T_{STG}$                 | Storage Temperature Range                |                        |       |
|                           | Soldering Temperature, for 10 seconds    | 300 (1.6mm from case ) |       |

## Thermal Resistance

|                 | Parameter                          | Typ. | Max. | Units |
|-----------------|------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case                   | —    | 3.1  | °C/W  |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount) ** | —    | 50   |       |
| $R_{\theta JA}$ | Junction-to-Ambient                | —    | 110  |       |

Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

|                                 | Parameter                            | Min. | Typ. | Max. | Units               | Conditions                                                                    |
|---------------------------------|--------------------------------------|------|------|------|---------------------|-------------------------------------------------------------------------------|
| $V_{(BR)DSS}$                   | Drain-to-Source Breakdown Voltage    | 100  | —    | —    | V                   | $V_{GS} = 0V, I_D = 250\mu A$                                                 |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient  | —    | 0.12 | —    | V/ $^\circ\text{C}$ | Reference to $25^\circ\text{C}$ , $I_D = 1mA$                                 |
| $R_{DS(on)}$                    | Static Drain-to-Source On-Resistance | —    | —    | 0.21 |                     | $V_{GS} = 10V, I_D = 5.6A$ ④                                                  |
| $V_{GS(th)}$                    | Gate Threshold Voltage               | 2.0  | —    | 4.0  | V                   | $V_{DS} = V_{GS}, I_D = 250\mu A$                                             |
| $g_{fs}$                        | Forward Transconductance             | 2.7  | —    | —    | S                   | $V_{DS} = 25V, I_D = 5.7A$ ⑥                                                  |
| $I_{DSS}$                       | Drain-to-Source Leakage Current      | —    | —    | 25   | $\mu A$             | $V_{DS} = 100V, V_{GS} = 0V$                                                  |
|                                 |                                      | —    | —    | 250  |                     | $V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$                          |
| $I_{GSS}$                       | Gate-to-Source Forward Leakage       | —    | —    | 100  | nA                  | $V_{GS} = 20V$                                                                |
|                                 | Gate-to-Source Reverse Leakage       | —    | —    | -100 |                     | $V_{GS} = -20V$                                                               |
| $Q_g$                           | Total Gate Charge                    | —    | —    | 25   | nC                  | $I_D = 5.7A$                                                                  |
| $Q_{gs}$                        | Gate-to-Source Charge                | —    | —    | 4.8  |                     | $V_{DS} = 80V$                                                                |
| $Q_{gd}$                        | Gate-to-Drain ("Miller") Charge      | —    | —    | 11   |                     | $V_{GS} = 10V$ , See Fig. 6 and 13 ④ ⑥                                        |
| $t_{d(on)}$                     | Turn-On Delay Time                   | —    | 4.5  | —    | ns                  | $V_{DD} = 50V$                                                                |
| $t_r$                           | Rise Time                            | —    | 23   | —    |                     | $I_D = 5.7A$                                                                  |
| $t_{d(off)}$                    | Turn-Off Delay Time                  | —    | 32   | —    |                     | $R_G = 22\Omega$                                                              |
| $t_f$                           | Fall Time                            | —    | 23   | —    |                     | $R_D = 8.6\Omega$ , See Fig. 10 ④ ⑥                                           |
| $L_D$                           | Internal Drain Inductance            | —    | 4.5  | —    | nH                  | Between lead,<br>6mm (0.25in.)<br>from package<br>and center of die contact ⑤ |
| $L_S$                           | Internal Source Inductance           | —    | 7.5  | —    |                     |                                                                               |
| $C_{iss}$                       | Input Capacitance                    | —    | 330  | —    | pF                  | $V_{GS} = 0V$                                                                 |
| $C_{oss}$                       | Output Capacitance                   | —    | 92   | —    |                     | $V_{DS} = 25V$                                                                |
| $C_{rss}$                       | Reverse Transfer Capacitance         | —    | 54   | —    |                     | $f = 1.0MHz$ , See Fig. 5 ⑥                                                   |



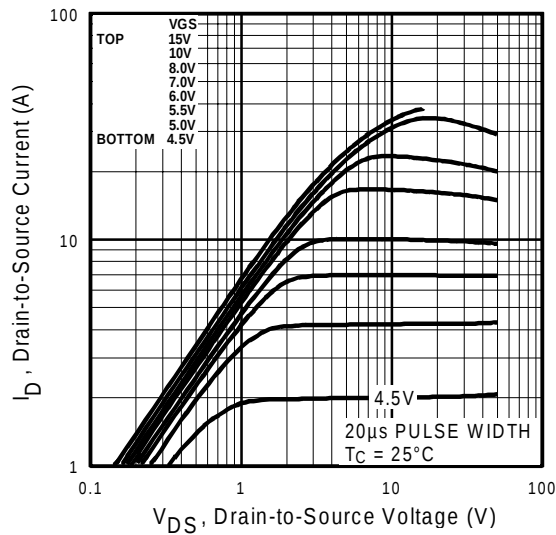
## Source-Drain Ratings and Characteristics

|          | Parameter                                 | Min.                                                                        | Typ. | Max. | Units | Conditions                                                              |
|----------|-------------------------------------------|-----------------------------------------------------------------------------|------|------|-------|-------------------------------------------------------------------------|
| $I_S$    | Continuous Source Current<br>(Body Diode) | —                                                                           | —    | 9.4  | A     | MOSFET symbol<br>showing the<br>integral reverse<br>p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current<br>(Body Diode) ① ⑥ | —                                                                           | —    | 38   |       |                                                                         |
| $V_{SD}$ | Diode Forward Voltage                     | —                                                                           | —    | 1.3  | V     | $T_J = 25^\circ\text{C}, I_S = 5.5A, V_{GS} = 0V$ ④                     |
| $t_{rr}$ | Reverse Recovery Time                     | —                                                                           | 99   | 150  | ns    | $T_J = 25^\circ\text{C}, I_F = 5.7A$                                    |
| $Q_{rr}$ | Reverse Recovery Charge                   | —                                                                           | 390  | 580  | nC    | $di/dt = 100A/\mu s$ ④ ⑥                                                |
| $t_{on}$ | Forward Turn-On Time                      | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ ) |      |      |       |                                                                         |

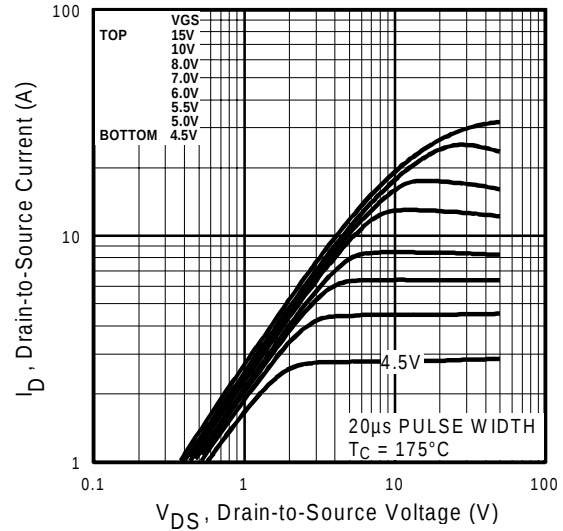
## Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ②  $V_{DD} = 25V$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 4.7mH$   
 $R_G = 25\Omega$ ,  $I_{AS} = 5.7A$ . (See Figure 12)
- ③  $I_{SD} \leq 5.7A$ ,  $di/dt \leq 240A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$
- ⑤ This is applied for I-PAK,  $L_S$  of D-PAK is measured between lead and center of die contact
- ⑥ Uses IRF520N data and test conditions

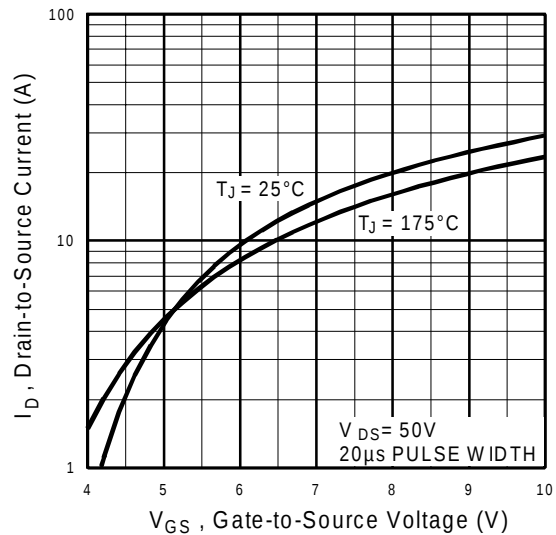
\*\* When mounted on 1" square PCB (FR-4 or G-10 Material ) .  
For recommended footprint and soldering techniques refer to application note #AN-994



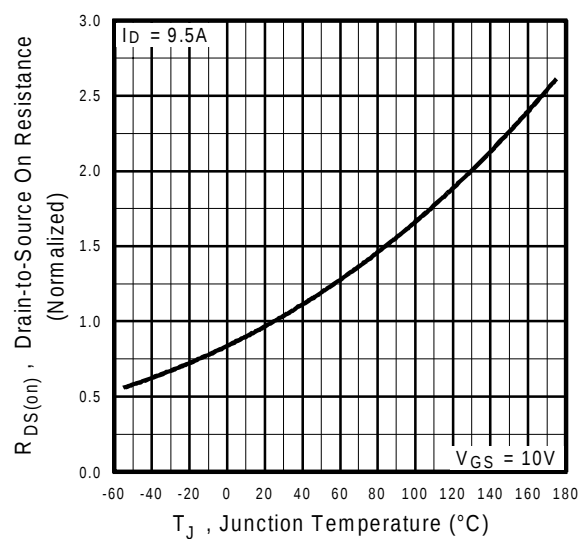
**Fig 1.** Typical Output Characteristics



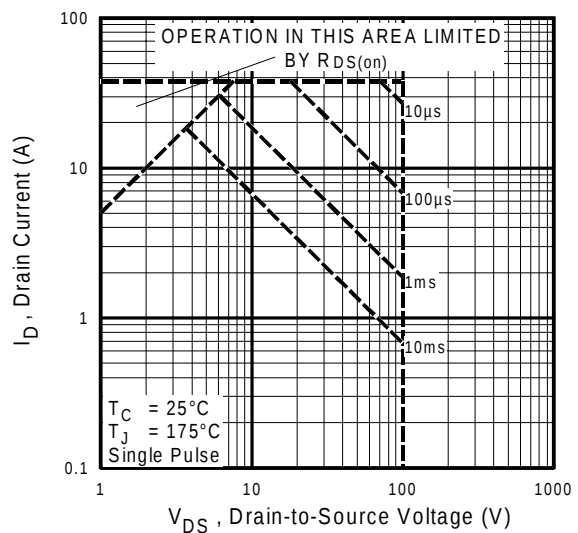
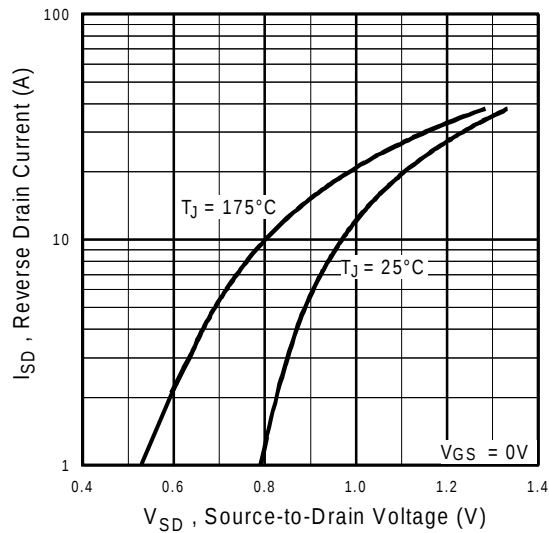
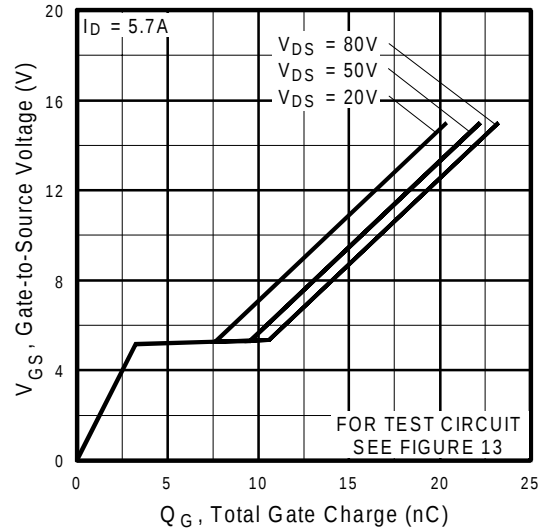
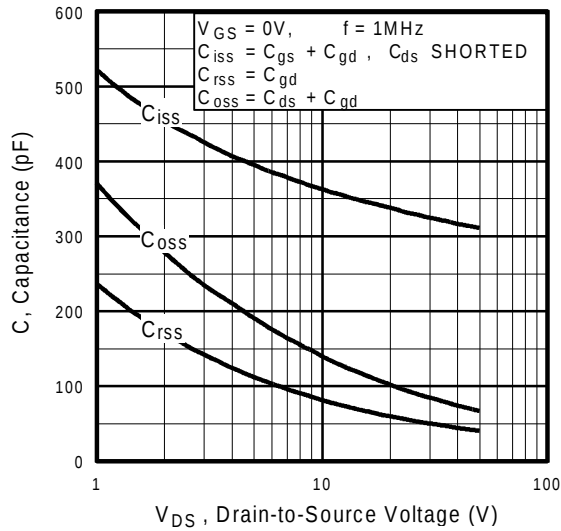
**Fig 2.** Typical Output Characteristics

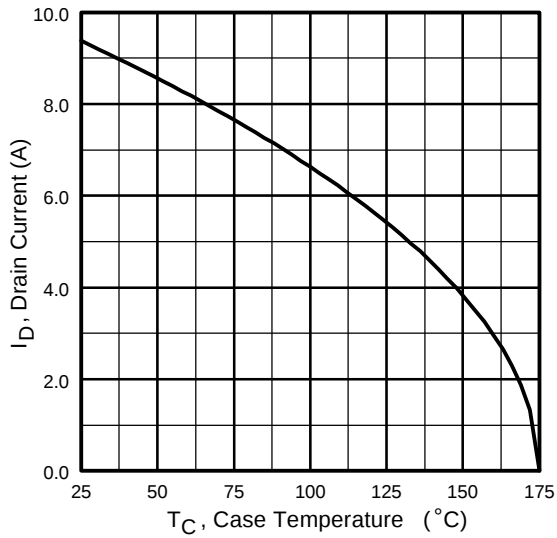


**Fig 3.** Typical Transfer Characteristics

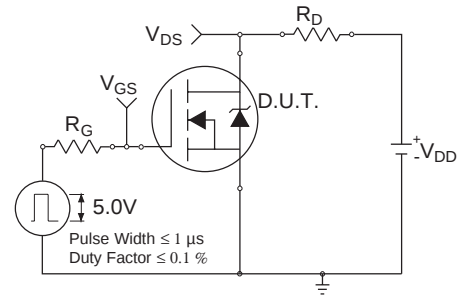


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

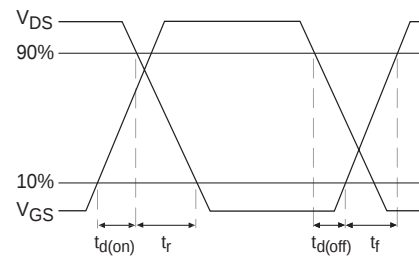




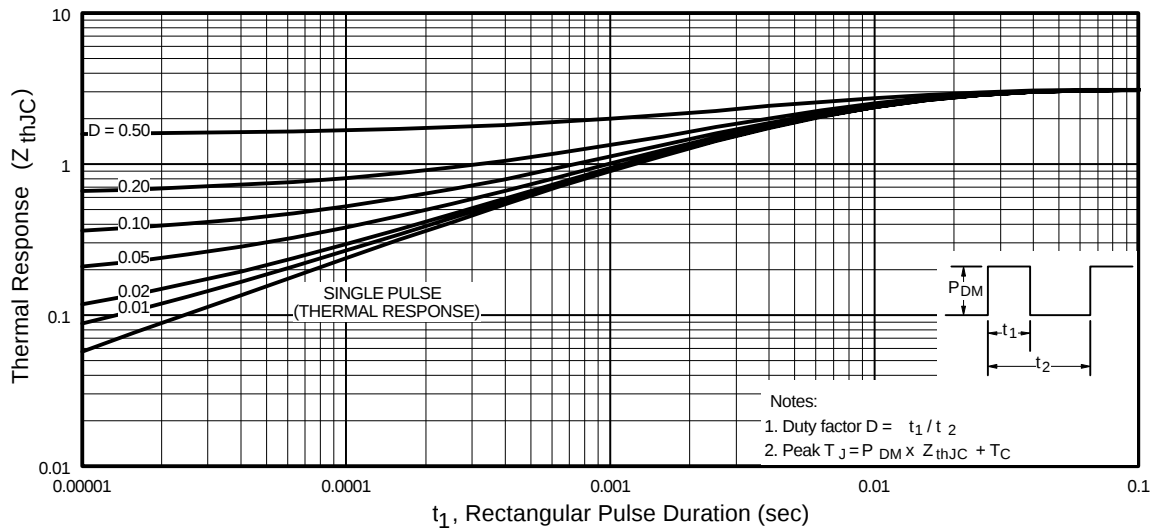
**Fig 9.** Maximum Drain Current Vs. Case Temperature



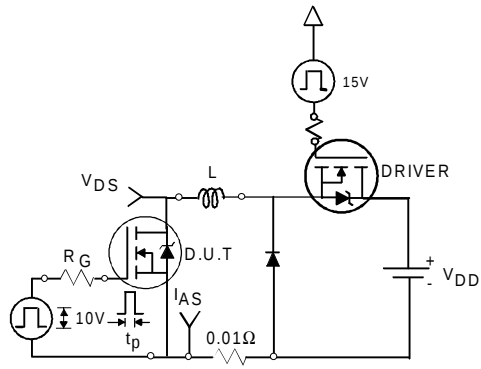
**Fig 10a.** Switching Time Test Circuit



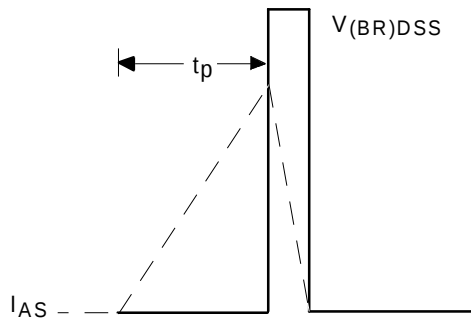
**Fig 10b.** Switching Time Waveforms



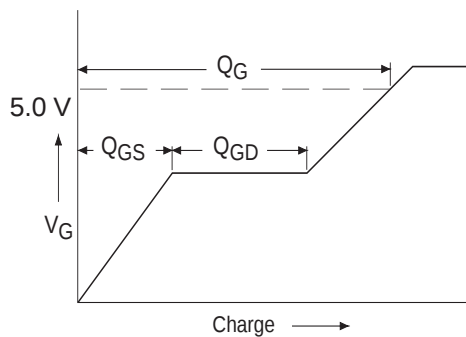
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



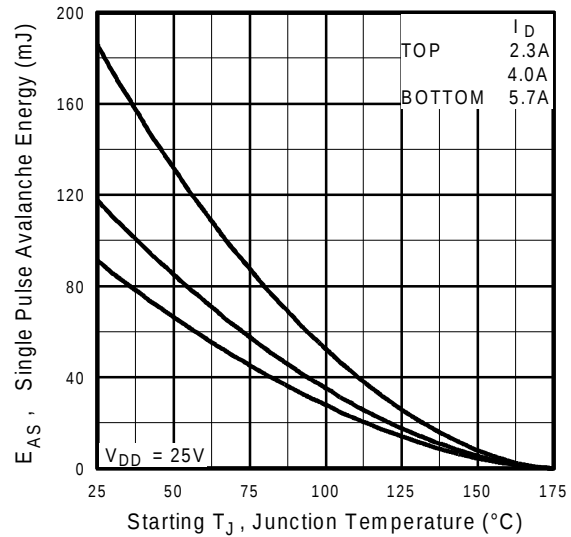
**Fig 12a.** Unclamped Inductive Test Circuit



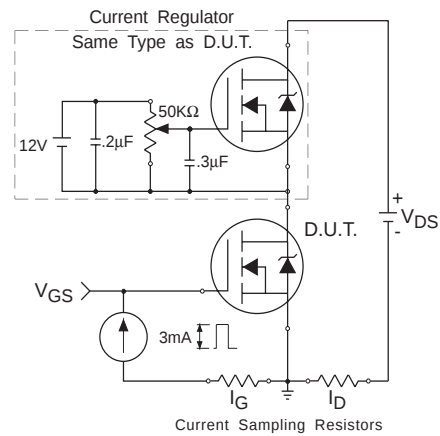
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

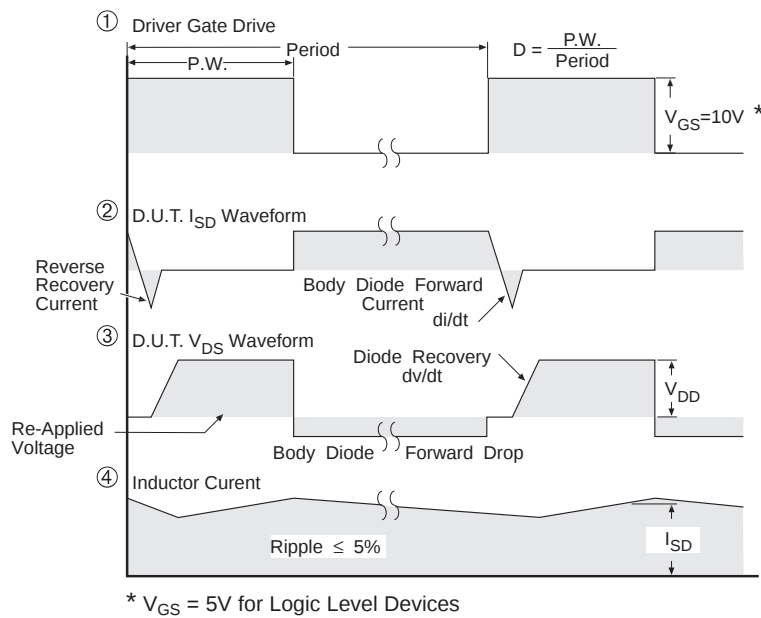
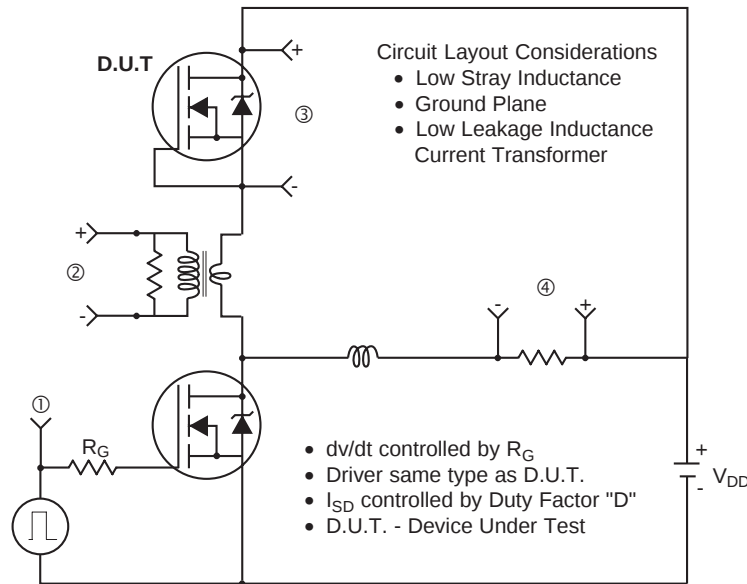


**Fig 12c.** Maximum Avalanche Energy  
Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

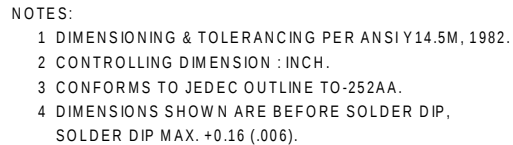
### Peak Diode Recovery dv/dt Test Circuit



**Fig 14.** For N-Channel HEXFETS

International  
**IOR** Rectifier

Dimensions are shown in millimeters (inches)



TO-252AA (D-PARK)

Diagram illustrating the markings on a MOSFET package (IRFR120P) and their corresponding labels:

- INTERNATIONAL RECTIFIER LOGO**: Points to the IR logo on the package.
- FIRST PORTION OF PART NUMBER**: Points to the "IRFR" marking.
- SECOND PORTION OF PART NUMBER**: Points to the "120" marking.
- ASSEMBLY LOT CODE**: Points to the "9U" marking.
- 1P**: Points to the "1P" marking, indicating the package type.

## TO-251AA Outline

6.73 (.265)  
6.35 (.250)  
- A -

5.46 (.215)  
5.21 (.205)

1.27 (.050)  
0.88 (.035)

4

1.52 (.060)  
1.15 (.045)

6.22 (.245)  
5.97 (.235)

1 2 3

- B -

2.28 (.090)  
1.91 (.075)

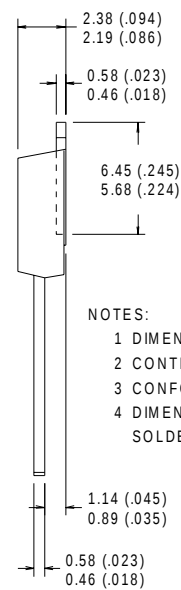
9.65 (.380)  
8.89 (.350)

1.14 (.045)  
0.76 (.030)  
3X

0.89 (.035)  
0.64 (.025)  
3X

2.28 (.090)  
2X

⊕ 0.25 (.010) M A M B



1 - GATE  
2 - DRAIN  
3 - SOURCE  
4 - DRAIN

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.  
2 CONTROLLING DIMENSION : INCH.  
3 CONFORMS TO JEDEC OUTLINE TO-252AA.  
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,  
SOLDER DIP MAX. +0.16 (.006).

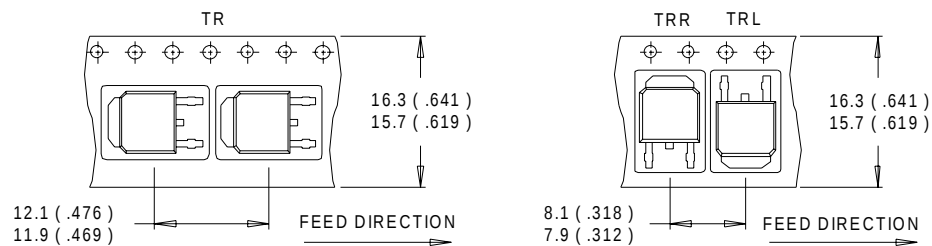
**TO-251AA (I-PARK)**

Diagram illustrating the markings on a MOSFET package (IRFU120P) and their corresponding labels:

- INTERNATIONAL RECTIFIER LOGO**: Points to the **IR** logo on the package.
- FIRST PORTION OF PART NUMBER**: Points to the **120** marking on the package.
- SECOND PORTION OF PART NUMBER**: Points to the **1P** marking on the package.
- ASSEMBLY LOT CODE**: Points to the **9U** marking on the package.

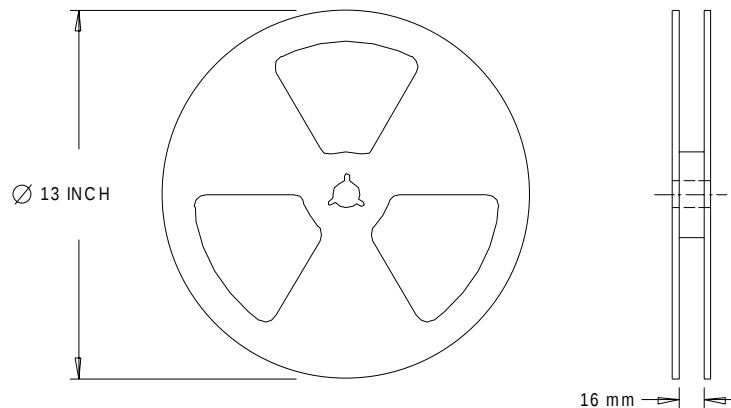
## Tape & Reel Information

### TO-252AA



#### NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



#### NOTES :

1. OUTLINE CONFORMS TO EIA-481.