GaAS MMIC SOT26 SPDT SWITCH DC - 3 GHz

FEBRUARY 2001 v01.0700

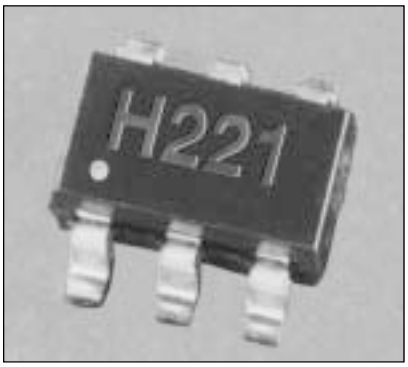
Features

LOW INSERTION LOSS: 0.4 dB

ULTRA SMALL PACKAGE: SOT26

INPUT IP3: +45 dBm

POSITIVE CONTROL: 0/+3V @ 10 µA



General Description

The HMC221 is a low-cost SPDT switch in a 6-lead SOT26 plastic package for use in general switching applications which require very low insertion loss and very small size. The device can control signals from DC to 3.0 GHz and is especially suited for 900 MHz, 1.8-2.2GHz, and 2.4GHz ISM applications with less than 1dB loss. The design provides exceptional insertion loss performance, ideal for filter and receiver switching. RF1 or RF2 is a reflective short when "Off". The two control voltages require a minimal amount of DC current and offer compatibility with most CMOS & TTL logic families. The HMC221 is especially suited for PCMCIA wireless card and cellular phone applications. See HMC197 for same performance in an alternate SOT26 pin-out.

Guaranteed Performance *Vctl = 0/+3 to +8 Vdc, -40 to +85 deg C*

Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		0.4 0.45 0.6 0.8	0.7 0.8 0.9 1.1	dB dB dB dB
Isolation	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz	24 24 21 14	28 28 25 18		dB dB dB dB
Return Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz	20 17 16 11	23 22 20 15		dB dB dB dB
Input Power for 1dB Compression (Vctl = 0/+5V)	0.5 - 1.0 GHz 0.5 - 3.0 GHz	25 23	30 29		dBm dBm
Input Third Order Intercept (Vctl = 0/+5V, +7 dBm each tone)	0.5 - 1.0 GHz 0.5 - 3.0 GHz	40 38	45 43		dBm dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 3.0 GHz		 3 10		 nS nS

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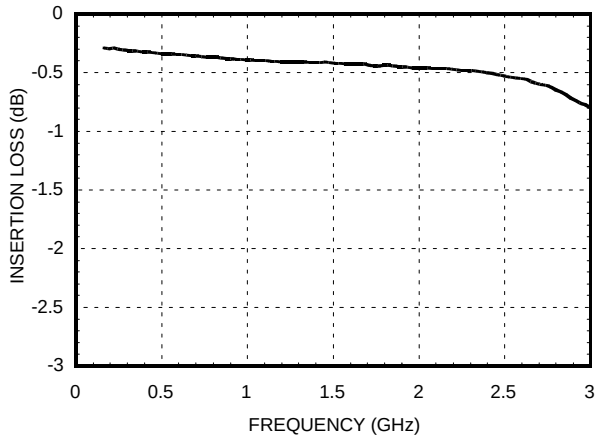
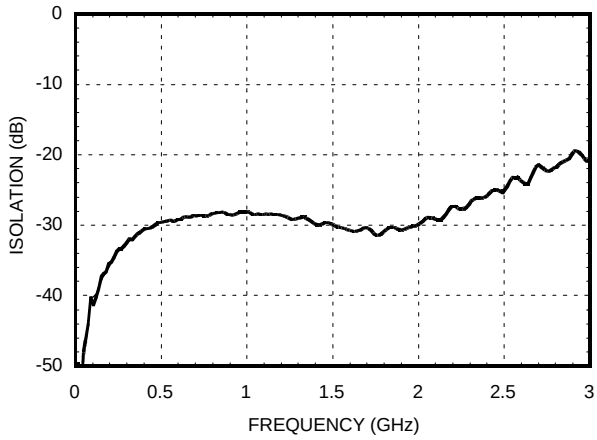
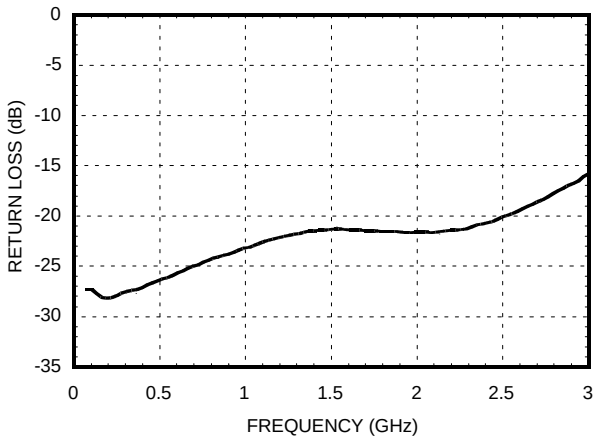
Insertion Loss



Isolation



Return Loss



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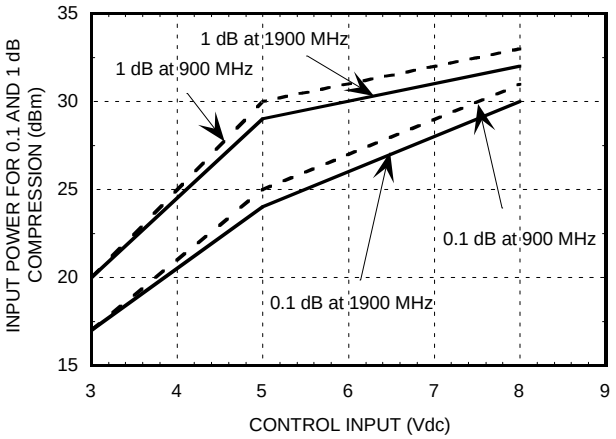
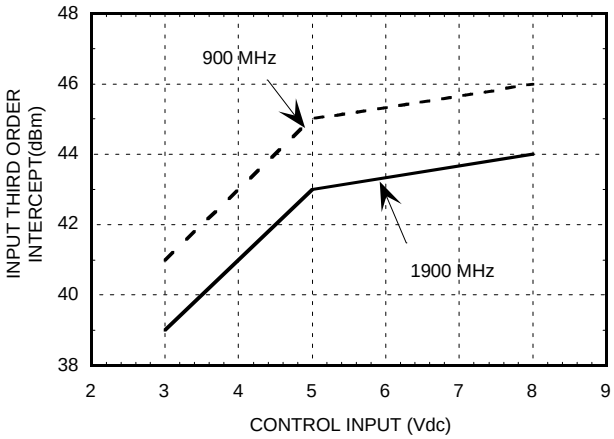
Input 0.1 and 1.0 dB Compression vs Control Voltage



Input Third Order Intercept vs Control Voltage



Compression vs Control Voltage

	Carrier at 900MHz		Carrier at 1900MHz	
Control Input	Input Power for 0.1dB Compression	Input Power for 1dB Compression	Input Power for 0.1dB Compression	Input Power for 1dB Compression
(Vdc)	(dBm)	(dBm)	(dBm)	(dBm)
+3	17	20	17	20
+5	25	30	24	29
+8	31	33	30	32

Caution: Do not operate in 1dB compression at power levels above +31 dBm (Vctl= +5 Vdc) and do not 'hot switch' power levels greater than +20 dBm (V_{CTL} = +5Vdc).

DC blocks are required at ports RFC, RF1 and RF2.

Distortion vs Control Voltage

Control Input	Third Order Intercept (dBm) +7 dBm Each Tone	
(Vdc)	900 MHz	1900 MHz
+3	41	39
+5	45	43
+8	46	44

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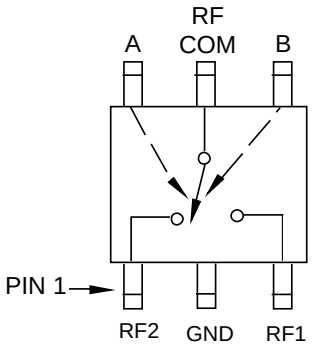
Functional Diagram



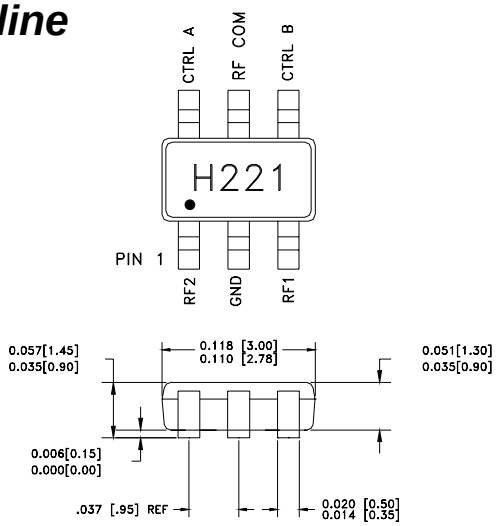
Truth Table **Control Input Tolerances are +/- 0.2 Vdc*

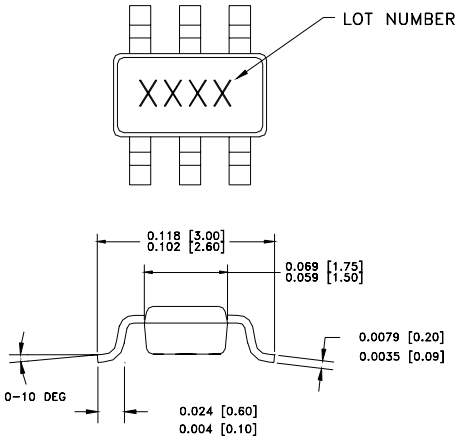
Control Input *		Control Current		Signal Path	
A (Vdc)	B (Vdc)	Ia (uA)	Ib (uA)	RF to RF1	RF to RF2
0	+3	-10	10	On	Off
+3	0	10	-10	Off	On
0	+5	-55	55	On	Off
+5	0	55	-55	Off	On
0	+7	-210	210	On	Off
+7	0	210	-210	Off	On
0	+8	-280	280	On	Off
+8	0	280	-280	Off	On

Absolute Maximum Ratings

Control Voltage Range (A & B)	-0.2 to +12Vdc
Storage Temperature	-65 to +150 deg. C
Operating Temperature	-40 to +85 deg. C

Outline





1) MATERIAL:
A) PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED
B) LEADFRAME MATERIAL: COPPER ALLOY
2. PLATING: LEAD-TIN SOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS)
UNLESS OTHERWISE SPECIFIED TOL. ARE ±0.005(±0.13)

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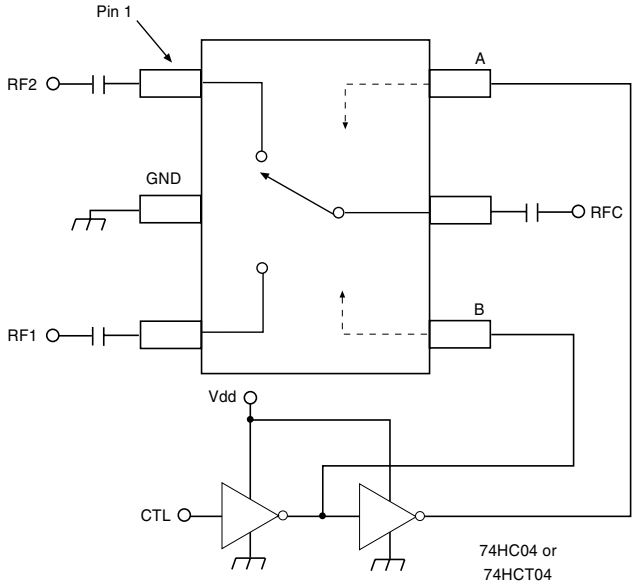
Typical Application Circuit



Notes:

1. Set logic gate and switch Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of 5 to 8 Volts applied to the CMOS logic gates.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with Vdd = +8V and A/B set to 0/+8V.

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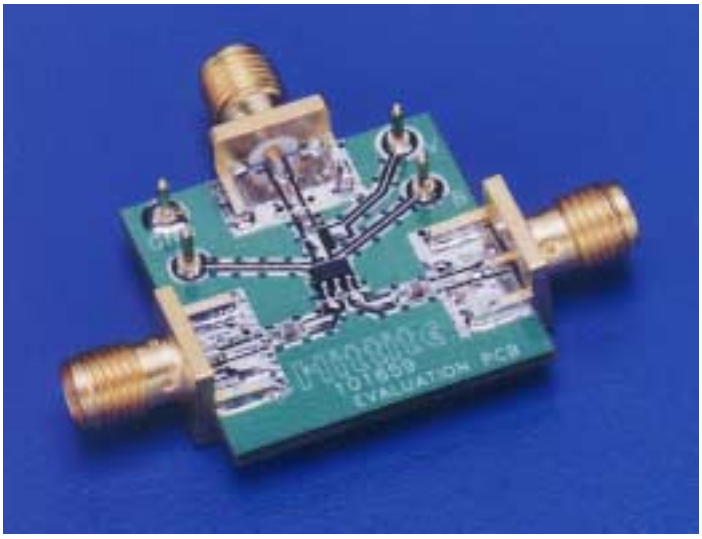
Evaluation Circuit Board



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown below. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board as shown is available from Hittite upon request.

Evaluation Circuit Board Layout Design Details

Layout Technique	Grounded Co-Planar Waveguide (GCPW)
Material	FR4
Dielectric Thickness	0.028" (0.71 mm)
50 Ohm Line Width	0.037" (0.94 mm)
Gap to Ground Edge	0.010" (0.25 mm)
Ground VIA Hole Diameter	0.014" (0.36 mm)
Connectors	SMA-F (EF - Johnson P/N 142-0701-806)