

# **HD74AC259**

### 8-bit Addressable Latch

REJ03D0264-0200Z (Previous ADE-205-385 (Z)) Rev.2.00 Jul.16.2004

#### **Description**

The HD74AC259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable or storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable.

#### **Features**

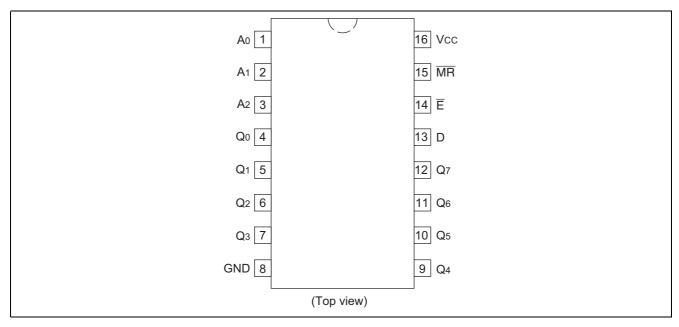
- Serial-to-Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random (Addressable) Data Entry
- · Active High Demultiplexing or Decoding Capability
- · Easily Expandable
- Common Clear
- Outputs Source/Sink 24 mA
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC259FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC259RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

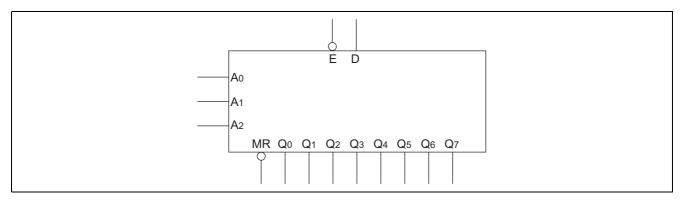
Notes: 1. Please consult the sales office for the above package availability.

2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

### **Pin Arrangement**



## **Logic Symbol**

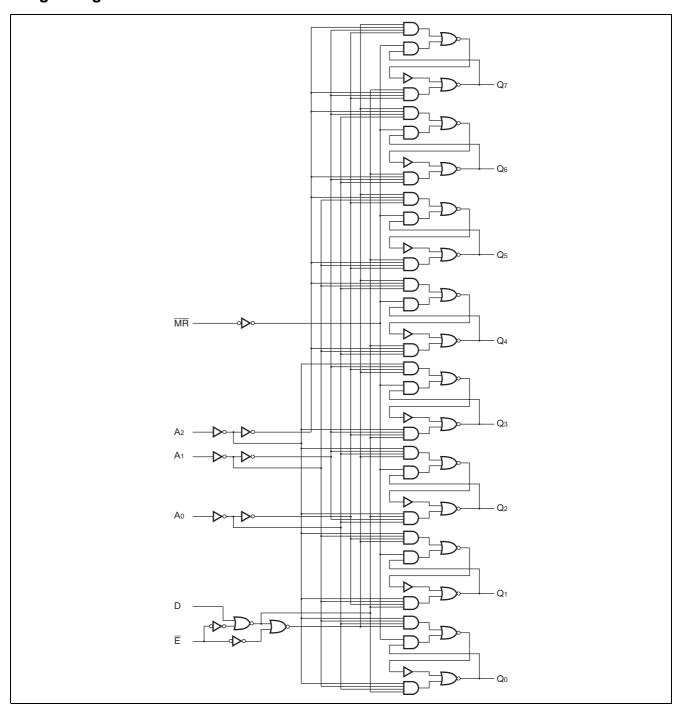


## **Pin Names**

 $\begin{array}{ll} A_0 - A_2 & Address \ Inputs \\ D & Data \ Inputs \end{array}$ 

 $Q_0 - Q_7$  Latch Outputs

## Logic Diagram



#### **Function Table**

	Inputs						Outputs							
Operating Mode	MR	Ē	D	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	$Q_0$	Q <sub>1</sub>	$Q_2$	$Q_3$	$Q_4$	$Q_5$	$Q_6$	Q <sub>7</sub>
Master reset	L	Н	Χ	Χ	Χ	Χ	L	L	L	L	L	L	L	L
Demultiplex	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
(Active HIGH	L	L	d	Н	L	L	L	Q = d	L	L	L	L	L	L
Decoder when	L	L	d	L	Н	L	L	L	Q = d	L	L	L	L	L
D = H)	L	L	d	Н	Н	L	L	L	L	Q = d	L	L	L	L
	L	L	d	L	L	Н	L	L	L	L	Q = d	L	L	L
	L	L	d	Н	L	Н	L	L	L	L	L	Q = d	L	L
	L	L	d	L	Н	Н	L	L	L	L	L	L	Q = d	L
	L	L	d	Н	Н	Н	L	L	L	L	L	L	L	Q = d
Store (Do nothing)	Н	Н	Х	Х	Χ	Х	$q_0$	q₁	$q_2$	$q_3$	$q_4$	$q_5$	$q_6$	q <sub>7</sub>
Addressable latch	Н	L	d	L	L	L	Q = d	q₁	$q_2$	$q_3$	$q_4$	$q_5$	$q_6$	q <sub>7</sub>
	Н	L	d	Н	L	L	$q_0$	Q = d	$q_2$	$q_3$	$q_4$	$q_5$	$q_6$	q <sub>7</sub>
	Н	L	d	L	Н	L	$q_0$	$q_1$	Q = d	$q_3$	$q_4$	$q_5$	$q_6$	$q_7$
	Н	L	d	Н	Н	L	$q_0$	$q_1$	$q_2$	Q = d	$q_4$	$q_5$	$q_6$	$q_7$
	Н	L	d	L	L	Н	$q_0$	$q_1$	$q_2$	$q_3$	Q = d	$q_5$	$q_6$	$q_7$
	Н	L	d	Н	L	Н	$q_0$	q₁	$q_2$	$q_3$	$q_4$	Q = d	$q_6$	$q_7$
	Н	L	d	L	Н	Н	$q_0$	$q_1$	$q_2$	$q_3$	$q_4$	$q_5$	Q = d	$q_7$
	Н	L	d	Н	Н	Н	$q_0$	$q_1$	$q_2$	$q_3$	$q_4$	$q_5$	$q_6$	Q = d

H: High Voltage Level
L: Low Voltage Level

X : Immaterial

d: High or Low data one setup time prior to the Low-to-High Enable transition.

q : Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

## **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V <sub>cc</sub>	-0.5 to 7	V	
DC input diode current	I <sub>IK</sub>	-20	mA	$V_1 = -0.5V$
		20	mA	$V_1 = Vcc+0.5V$
DC input voltage	V <sub>I</sub>	-0.5 to Vcc+0.5	V	
DC output diode current	I <sub>ok</sub>	-50	mA	$V_0 = -0.5V$
		50	mA	$V_O = Vcc+0.5V$
DC output voltage	V <sub>o</sub>	-0.5 to Vcc+0.5	V	
DC output source or sink current	Io	±50	mA	
DC V <sub>CC</sub> or ground current per output pin	$I_{CC}$ , $I_{GND}$	±50	mA	
Storage temperature	Tstg	-65 to +150	°C	

## **Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V <sub>CC</sub>	2 to 6	V	
Input and output voltage	$V_{I}, V_{O}$	0 to V <sub>CC</sub>	V	
Operating temperature	Та	-40 to +85	°C	
Input rise and fall time	tr, tf	8	ns/V	$V_{CC} = 3.0V$
(except Schmitt inputs)				$V_{CC} = 4.5 \text{ V}$
$V_{IN}$ 30% to 70% $V_{CC}$				V <sub>CC</sub> = 5.5 V

### **DC Characteristics**

Item	Sym- bol	Vcc (V)	٦	Га = 25°(	С	Ta = -40 to +85°C		Unit	Condition
			min.	typ.	max.	min.	max.		
Input Voltage	V <sub>IH</sub>	3.0	2.1	1.5	_	2.1	_	٧	$V_{OUT} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$
		4.5	3.15	2.25	_	3.15	_		
		5.5	3.85	2.75	_	3.85	_		
	V <sub>IL</sub>	3.0	_	1.50	0.9	_	0.9		$V_{OUT} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$
		4.5	_	2.25	1.35	_	1.35		
		5.5	_	2.75	1.65	_	1.65		
Output voltage	V <sub>OH</sub>	3.0	2.9	2.99	_	2.9	_	V	$V_{IN} = V_{IL}$ or $V_{IH}$
		4.5	4.4	4.49	_	4.4	_		$I_{OUT} = -50 \mu A$
		5.5	5.4	5.49	_	5.4	_		
		3.0	2.58	_	_	2.48	_		$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -12 \text{ mA}$
		4.5	3.94	_	_	3.80	_		$I_{OH} = -24 \text{ mA}$
		5.5	4.94	_	_	4.80	_		$I_{OH} = -24 \text{ mA}$
	V <sub>OL</sub>	3.0	_	0.002	0.1	_	0.1		$V_{IN} = V_{IL}$ or $V_{IH}$
		4.5	_	0.001	0.1	_	0.1		I <sub>OUT</sub> = 50 μA
		5.5	_	0.001	0.1	_	0.1		
		3.0	_	_	0.32	_	0.37		$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 12 \text{ mA}$
		4.5	_	_	0.32	_	0.37		$I_{OL} = 24 \text{ mA}$
		5.5	_	_	0.32	_	0.37		$I_{OL} = 24 \text{ mA}$
Input leakage	I <sub>IN</sub>	5.5	_	_	±0.1	_	±1.0	μΑ	V <sub>IN</sub> = V <sub>CC</sub> or GND
current									
Dynamic output	I <sub>OLD</sub>	5.5	_	_	_	86	_	mA	V <sub>OLD</sub> = 1.1 V
current*	I <sub>OHD</sub>	5.5	_	_	_	-75	_	mA	V <sub>OHD</sub> = 3.85 V
Quiescent supply current	I <sub>cc</sub>	5.5	_	_	8.0	_	80	μА	$V_{IN} = V_{CC}$ or ground

<sup>\*</sup>Maximum test duration 2.0 ms, one output loaded at a time.

### **AC Characteristics**

			Ta = +25°C C <sub>L</sub> = 50 pF			Ta = $-40$ °C to $+85$ °C C <sub>L</sub> = 50 pF		
Item	Symbol	V <sub>cc</sub> (V)*1	Min	Тур	Max	Min	Max	Unit
Maximum clock	f <sub>max</sub>	3.3	65	_	_	60	_	MHz
frequency		5.0	110	_	_	95	_	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	8.5	14.5	1.0	16.5	ns
MR to Q <sub>n</sub>		5.0	1.0	6.5	9.0	1.0	10.5	
Propagation delay	t <sub>PLH</sub>	3.3	1.0	7.0	10.5	1.0	12.0	ns
D <sub>n</sub> to Q <sub>n</sub>		5.0	1.0	5.5	7.5	1.0	8.5	l
Propagation delay	t <sub>PHL</sub>	3.3	1.0	7.0	10.5	1.0	12.0	ns
D <sub>n</sub> to Q <sub>n</sub>		5.0	1.0	5.5	7.5	1.0	8.5	
Propagaion delay	t <sub>PLH</sub>	3.3	1.0	11.5	18.5	1.0	21.5	ns
$A_n$ to $Q_n$		5.0	1.0	8.0	11.5	1.0	14.0	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	11.5	18.5	1.0	21.0	ns
$A_n$ to $Q_n$		5.0	1.0	8.0	11.5	1.0	13.5	
Propagation delay	t <sub>PLH</sub>	3.3	1.0	9.0	15.0	1.0	17.0	ns
Ē to Q		5.0	1.0	6.5	9.0	1.0	10.5	
Propagation delay	t <sub>PHL</sub>	3.3	1.0	9.0	14.0	1.0	16.0	ns
E to Q <sub>n</sub>		5.0	1.0	6.5	8.5	1.0	10.0	

Note: 1. Voltage Range 3.3 is  $3.3 \text{ V} \pm 0.3 \text{ V}$ Voltage Range 5.0 is  $5.0 \text{ V} \pm 0.5 \text{ V}$ 



## **AC Operating Requirements**

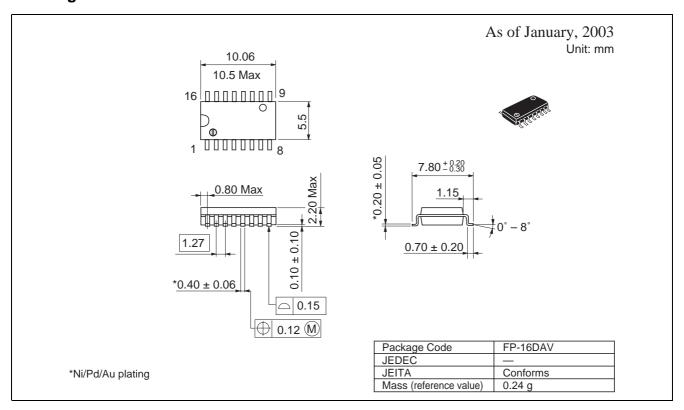
			Ta = +25°C C <sub>L</sub> = 50 pF		Ta = -40°C to +85°C C <sub>L</sub> = 50 pF	
Item	Symbol	V <sub>cc</sub> (V)*1	Тур	Guarantee	d Minimum	Unit
Setup time, HIGH or LOW	t <sub>su</sub>	3.3	1.0	3.5	3.5	ns
D to E		5.0	0.0	3.0	3.0	
Hold time, HIGH or LOW	t <sub>h</sub>	3.3	0.5	2.0	2.0	ns
D to E		5.0	0.5	2.0	2.0	
Setup time, HIGH or LOW	t <sub>su</sub>	3.3	1.0	6.0	7.0	ns
A <sub>n</sub> to E		5.0	0.0	4.5	5.0	
Hold time, HIGH or LOW	t <sub>h</sub>	3.3	-3.0	0.0	0.0	ns
A <sub>n</sub> to E		5.0	-1.0	0.0	0.0	
Pulse width	t <sub>w</sub>	3.3	3.0	5.5	7.0	ns
		5.0	3.0	4.5	5.0	

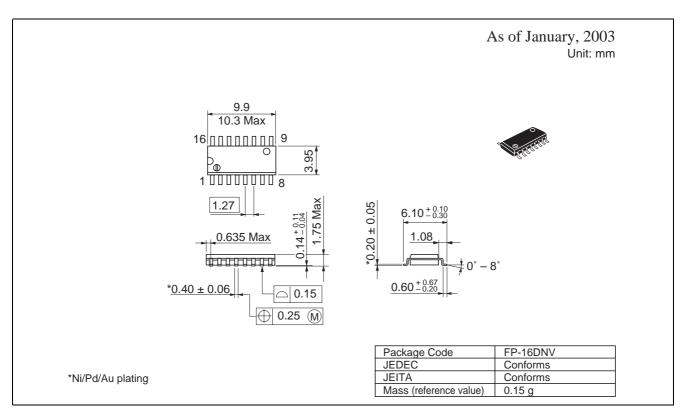
Note: 1. Voltage Range 3.3 is  $3.3 \text{ V} \pm 0.3 \text{ V}$ Voltage Range 5.0 is  $5.0 \text{ V} \pm 0.5 \text{ V}$ 

## Capacitance

Item	Symbol	Тур	Unit	Condition
Input capacitance	C <sub>IN</sub>	4.5	pF	$V_{CC} = 5.5 \text{ V}$
Power dissipation capacitance	C <sub>PD</sub>	35	pF	V <sub>CC</sub> = 5.0 V

### **Package Dimensions**





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Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632 Tel: <65> 6213-0200, Fax: <65> 6278-8001