

DTC114TCA / DTC114TSA

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making device design easy.

NPN digital transistor
(With single built in resistor)

B : Base
 C : Collector
 E : Emitter

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits(DTC114T□)					Unit
		E	UA	KA	CA	SA	
Collector-base voltage	V _{CBO}	50					V
Collector-emitter voltage	V _{CEO}	50					V
Emitter-base voltage	V _{EBO}	5					V
Collector current	I _C	100					mA
Collector power dissipation	P _C	150	200			300	mW
Junction temperature	T _j	150					℃
Storage temperature	T _{stg}	-55~+150					℃

●Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV _{CBO}	50	—	—	V	I _C =50 μA
Collector-emitter breakdown voltage	BV _{CEO}	50	—	—	V	I _C =1mA
Emitter-base breakdown voltage	BV _{EBO}	5	—	—	V	I _E =50 μA
Collector cutoff current	I _{CBO}	—	—	0.5	μA	V _{CB} =50V
Emitter cutoff current	I _{EBO}	—	—	0.5	μA	V _{EB} =4V
Collector-emitter saturation voltage	V _{CE(sat)}	—	—	0.3	V	I _C /I _B =10mA/1mA
DC current transfer ratio	h _{FE}	100	300	600	—	V _{CE} =5V, I _C =1mA
Input resistance	R _i	7	10	13	kΩ	—
Transition frequency	f _T	—	250	—	MHz	V _{CE} =10V, I _E =-5mA, f=100MHz *

* Transition frequency of the device

●Packaging specifications

Part No.	Package	EMT3	UMT3	SMT3	SST3	SPT
	Packaging type	Taping	Taping	Taping	Taping	Taping
	Code	TL	T106	T146	T116	TP
	Basic ordering unit (pieces)	3000	3000	3000	3000	5000
DTC114TE		○	—	—	—	—
DTC114TUA		—	○	—	—	—
DTC114TKA		—	—	○	—	—
DTC114TCA		—	—	—	○	—
DTC114TSA		—	—	—	—	○

● Electrical characteristic curves

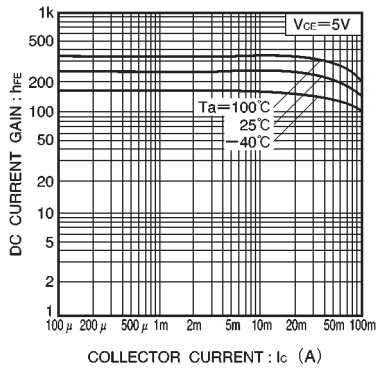


Fig.1 DC current gain vs. collector current

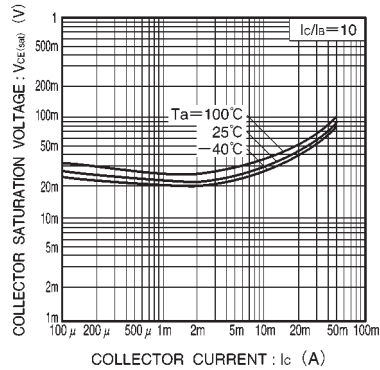


Fig.2 Collector-emitter saturation voltage vs. collector current