CAP200DG
CAPZero™-2

Zero[1] Loss Automatic X Capacitor Discharge IC

Product Highlights

- One part to cover X capacitor values from 100 nF to 6 μF
- Blocks current through X capacitor discharge resistors when AC voltage is connected
- Automatically discharges X capacitors through discharge resistors when AC is disconnected
- Simplifies EMI filter design – larger X capacitor allows smaller inductive components with no change in consumption
- Only two terminals – meets safety standards for use before or after system input fuse
- >4 mm creepage on package and PCB
- Self supplied – no external bias required
- High common mode surge immunity – no external ground connection
- High differential surge withstand – 1000 V internal MOSFETs
- NEMKO and CB certification

EcoSmart™– Energy Efficient

- <5 mW consumption at 230 VAC for all X capacitor values

Applications

- All AC-DC converters with X capacitors of 100 nF up to 6 μF
- Appliances requiring EuP Lot 6 compliance
- Adapters requiring ultra low no-load consumption
- All converters requiring very low standby power
- Lossless generation of zero crossing signal

Description

When AC voltage is applied, CAP200DG blocks current flow in the X capacitor safety discharge resistors, reducing the power loss to less than 5 mW, or essentially zero[1] at 230 VAC. When AC voltage is disconnected, CAP200DG automatically discharges the X capacitor by connecting the series discharge resistors. This operation allows total flexibility in the choice of the X capacitor to optimize differential mode EMI filtering and reduce inductor costs, with no change in power consumption.

Designing with CAP200DG is simply a matter of selecting the appropriate external resistor values for the X capacitor value being used to achieve the necessary time constant. The simplicity and ruggedness of the two terminal CAP200DG IC makes it an ideal choice in systems designed to meet EuP Lot 6 requirements.

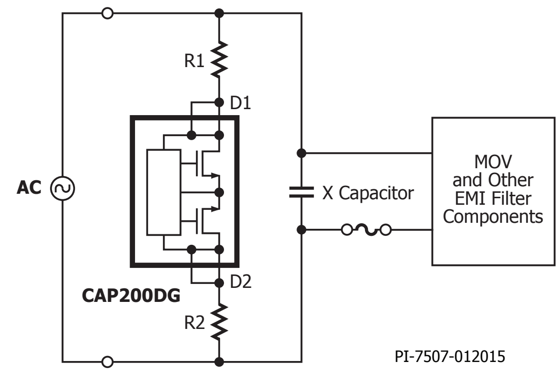


Figure 1. Typical Application – Not a Simplified Circuit.

Component Table

Product[3]	BV_{DSS}	Total X Capacitance	Total Series Resistance[2] (R1 + R2)
CAP200DG	1000 V	100 nF to 6 μF	7.5 MΩ to 142 kΩ

Table 1. Component Table.

Notes:
1. IEC 62301 clause 4.5 rounds standby power use below 5 mW to zero.
2. Values are nominal. RC time constant is <1 second.
3. Packages: D: SO-8.

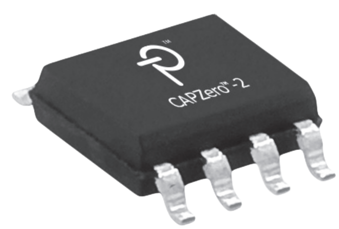


Figure 2. SO-8 D Package.

This Product is Covered by Patents and/or Pending Patent Applications.

Pin Functional Description

The pin configuration of Figure 3 ensures that the width of the SO-8 package is used to provide creepage and clearance distance of over 4 mm.

Although electrical connections are only made to pins 2, 3, 6 and 7, it is recommended that pins 1-4 and pins 5-8 are coupled together on the PCB – see Applications Section.

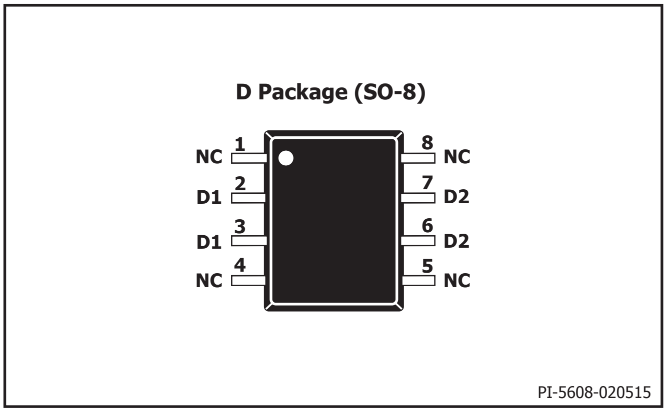


Figure 3. Pin Configuration.

Key Application Considerations

Breakdown Voltage Selection

The system configuration variables include the placement of the system MOV and X capacitor(s) as well as the differential surge voltage specifications of the application.

As shown in Table 1, the CAP200DG has a breakdown voltage of 1000 V. For applications where the system MOV is placed in position 1 (MOV_{POS1} in Figure 4), the CAP200DG will provide adequate voltage withstand for surge requirements of 3 kV or higher.

For MOV placement that is not directly across the X Capacitor1 (for example MOV_{POS2} in Figure 4) the 1000 V CAP200DG devices can be used up to a surge specification of 1.5 kV. For differential surge voltage specifications of >1.5 kV it is recommended that the MOV is always placed in the location shown in Figure 4 as MOV_{POS1}.

It is always recommended that the peak voltage between terminals D1 and D2 of CAP200DG is measured during surge tests in the final system. Measurements of peak voltage across CAP200DG during surge tests should be made with oscilloscope probes having appropriate voltage rating and using an isolated supply to the oscilloscope to avoid ground currents influencing measurement results. When making such measurements, it is recommended that 50 V engineering margin is allowed below the breakdown voltage specification (for example 950 V with the 1000 V CAP200DG).

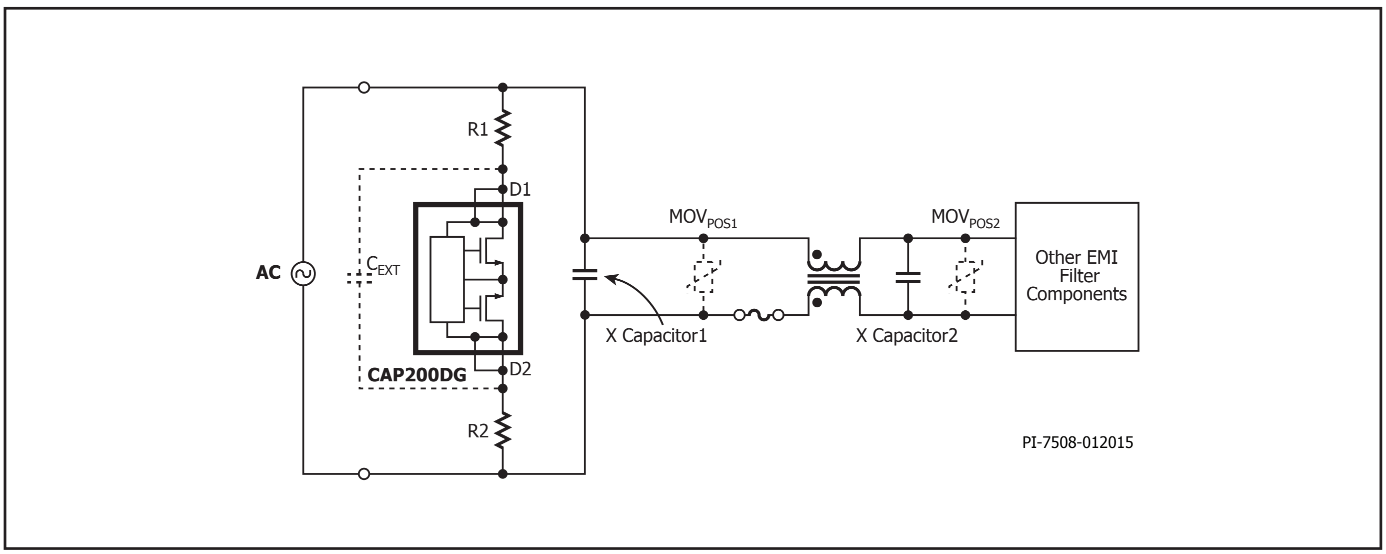


Figure 4. Placement Options of MOV and C_{EXT}.

If the measured peak Drain voltage exceeds 950 V, an external 1 kV ceramic capacitor of value up to 47 pF can also be placed between D1 and D2 terminals to attenuate the voltage applied between the CAP200DG terminals during surge. This optional external capacitor placement is shown as C_{EXT} in Figure 4. It should be noted that use of an external capacitor in this way will increase power consumption slightly due to the C_{EXT} charge/discharge currents flowing in R1 and R2 while AC is connected. A C_{EXT} value of 33 pF will add approximately 0.5 mW at 230 VAC, 50 Hz.

PCB Layout and External Resistor Selection

Figure 5 shows a typical PCB layout configuration for CAP200DG. The external resistors in this case are divided into two separate surface mount resistors to distribute loss under fault conditions – for example where a short-circuit exists between CAP200DG terminals D1 and D2. R1 and R2 values are selected according to Table 1.

Under a fault condition where CAP200DG terminals D1 and D2 are shorted together, each resistor will dissipate a power that can be calculated from the applied AC voltage and the R1 and R2 values. For example, in an application with R1=R2=75 kΩ. If CAP200DG is shorted out at 265 VAC then R1 and R2 will each dissipate 234 mW.

Resistors R1 and R2 should also be rated for 50% of the system input voltage again to allow for the short-circuitry of CAP200DG D1 to D2 pins during single point fault testing.

If lower dissipation or lower voltage across each resistor is required during fault tests, the total external resistance can be divided into more discrete resistors, however the total resistance must be equal to or greater than 150 kΩ.

Safety

CAP200DG meets safety requirements even if placed before the system input fuse. If a short-circuit is placed between D1 and D2 terminals of CAP200DG, the system is identical to existing systems where CAP200DG is not used.

With regard to open circuit tests, it is not possible to create a fault condition through a single pin fault (for example lifted pin test) since there are two pins connected to each of D1 and D2. If several pins are lifted to create an open circuit, the condition is identical to an open circuit X capacitor discharge resistor in existing systems where CAP200DG is not used. If redundancy against open circuit faults is required, two CAP200DG and R1 / R2 configurations can be placed in parallel.

Discharge Operation

To meet the safety regulations, when the AC supply is disconnected, CAP200DG will discharge the X capacitor to the safety extra low voltage (SELV) levels according to the above functional description. Although there are no specific safety requirements below SELV, CAP200DG still continues the discharge until the X capacitor is fully discharged. As such CAP200DG can be safely used at low input voltages such as the common industrial 18 VAC and 24 VAC supply rails while retaining X capacitor discharge when the AC source is disconnected.

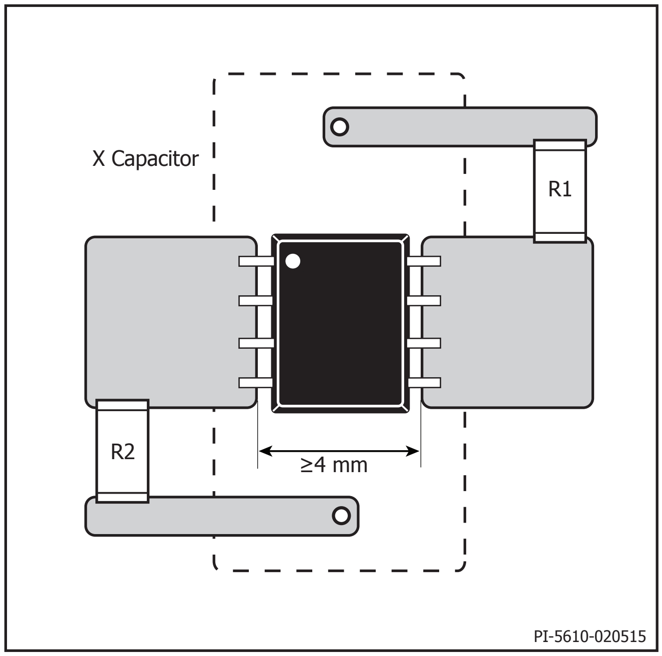


Figure 5. Typical PCB Layout.

Absolute Maximum Ratings[4]

DRAIN Pin Voltage[1] ....1000 V
DRAIN Peak Current[2] ....5.333 mA
Storage Temperature ....-65 °C to 150 °C
Lead Temperature[3] ....260 °C
Operating Ambient Temperature.............................. -10 °C to 105 °C
Maximum Junction Temperature .... -10 °C to 110 °C

Notes:
1. Voltage of D1 pin relative to D2 pin in either polarity.
2. The peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.
3. 1/16 in. from case for 5 seconds.
4. The Absolute Maximum Ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

Thermal Resistance

Thermal Resistance: D Package[1]:
(θ_{JA})................160 °C/W (Single layer JEDEC PCB)
(θ_{JC})...40 °C/W (Bottom)
(θ_{JC})... 75 °C/W (Top)

Notes:
1. Reference thermal resistance test conditions: JEDEC JESD51-3, SEMI Test Method #G43-87, and MIL-STD-883 Method 10121.1.

Parameter	Symbol	Conditions T_A = -10 to 105 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions						
AC Removal Detection Time	t_{DETECT}	Line Cycle Frequency 47-63 Hz		22	31.4	ms
Drain Saturation Current[A,B]	I_{DSAT}	CAP200DG	2.5			mA
Supply Current	I_{SUPPLY}	T_A = 25 °C			21.7	μA

Notes
A. Saturation current specifications ensure a natural RC discharge characteristic at all voltages up to 265 VAC peak with the external resistor values specified in Component Selection Table 1.
B. Specifications are guaranteed by characterization and design.

Typical Performance Characteristics

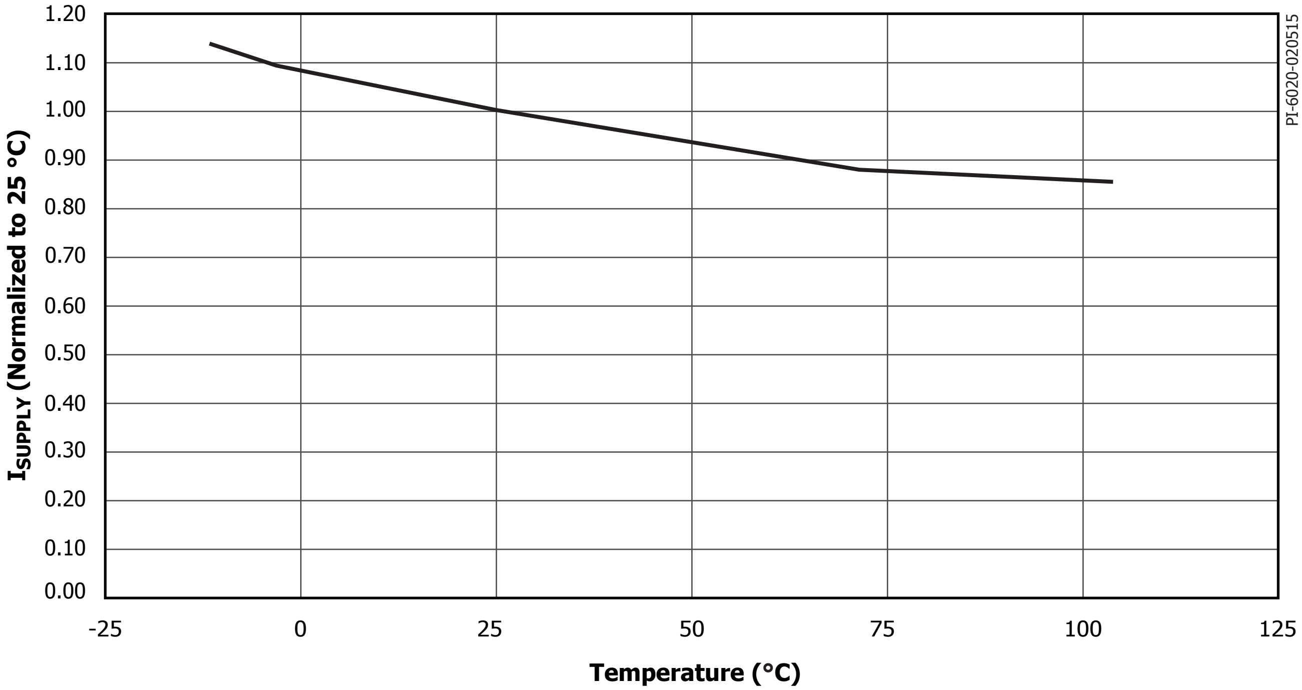
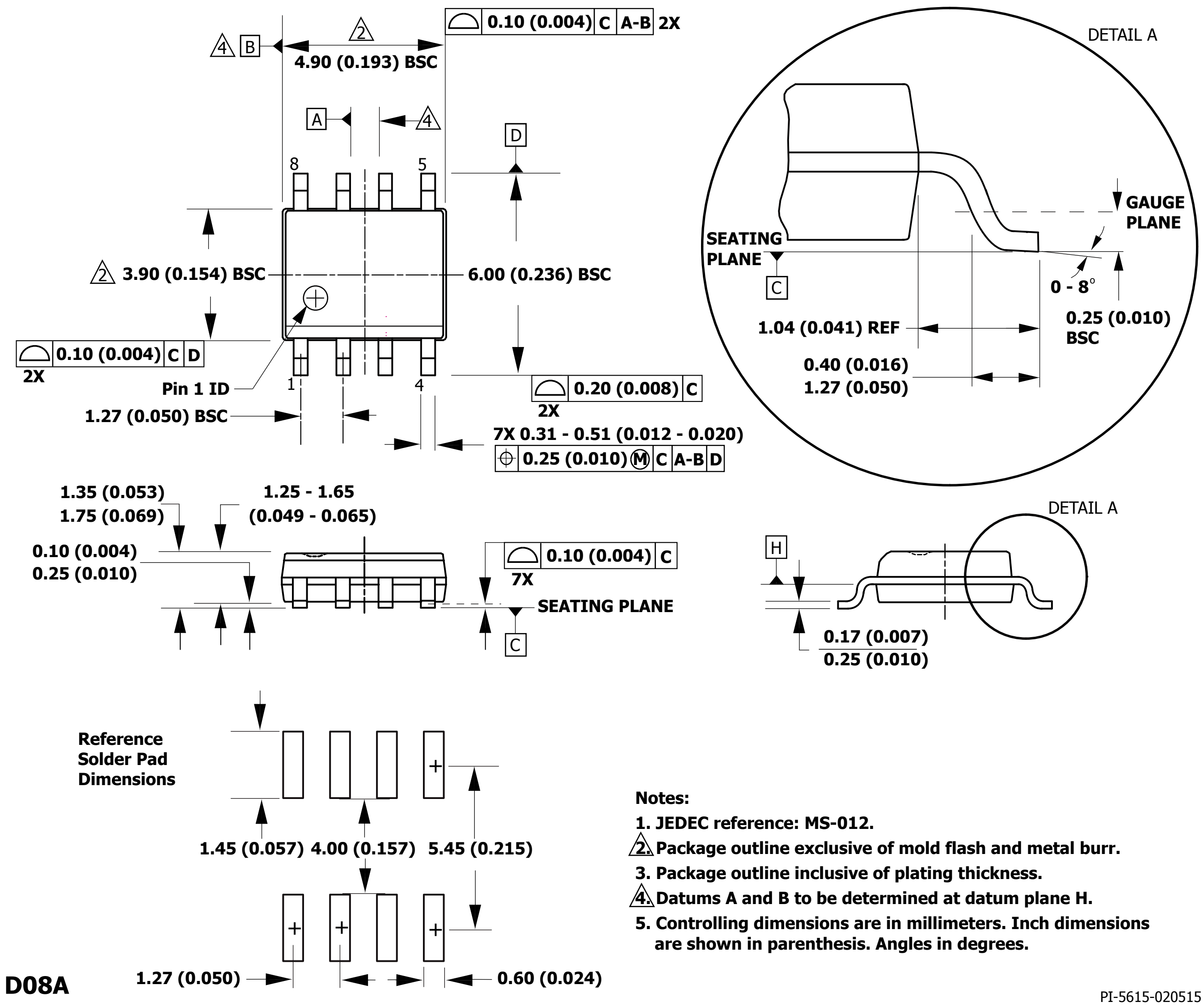


Figure 6. I_{SUPPLY} vs. Temperature.

SO-8 (D Package)



Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D08A

PI-5615-020515

Part Ordering Information

- **CAP200DG**
- **Series Number**
- **Package Identifier**

D	Plastic SO-8

- **Package Material**

G	GREEN: Halogen Free and RoHS Compliant

- **Tape & Reel and Other Options**

Blank	Standard Configurations
TL	Tape & Reel, 2.5 k pcs.

CAP 200 D G - TL

Revision	Notes	Date
A	Initial release.	02/15
B	Added Thermal Resistance section.	05/15

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