

# BLS2933-100

Microwave power LDMOS transistor

Rev. 01 — 1 August 2006

Product data sheet

## 1. Product profile

### 1.1 General description

100 W LDMOS power transistor (at a supply voltage of 32 V) for S-band radar applications in the 2.9 GHz to 3.3 GHz frequency range.

**Table 1: Typical performance**

$t_p = 200 \mu\text{s}$ ;  $\delta = 12 \%$ ;  $T_{case} = 25^\circ\text{C}$ ; in a class-AB production test circuit.

| Mode of operation | f<br>(GHz) | V <sub>DS</sub><br>(V) | P <sub>L</sub><br>(W) | G <sub>p</sub><br>(dB) | $\eta_D$<br>(%) | I <sub>Dq</sub><br>(mA) |
|-------------------|------------|------------------------|-----------------------|------------------------|-----------------|-------------------------|
| class AB          | 2.9 to 3.3 | 32                     | 100                   | 8                      | 40              | 20                      |

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

### 1.2 Features

- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- Excellent thermal stability
- Designed for broadband operation (2.9 GHz to 3.3 GHz)
- Internally matched for ease of use

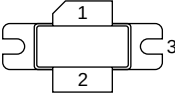
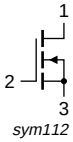
### 1.3 Applications

- S-band radar applications

# PHILIPS

2. Pinning information

Table 2. Pinning

| Pin | Description | Simplified outline                                                                  | Symbol                                                                              |
|-----|-------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 1   | drain       |  |  |
| 2   | gate        |                                                                                     |                                                                                     |
| 3   | source      |                                                                                     |                                                                                     |

[1] connected to flange

3. Ordering information

Table 3. Ordering information

| Type number | Package |                                                           |         |
|-------------|---------|-----------------------------------------------------------|---------|
|             | Name    | Description                                               | Version |
| BLS2933-100 | -       | flanged LDMOST ceramic package; 2 mounting holes; 2 leads | SOT502A |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol    | Parameter            | Conditions | Min | Max  | Unit |
|-----------|----------------------|------------|-----|------|------|
| $V_{DS}$  | drain-source voltage |            | -   | 65   | V    |
| $V_{GS}$  | gate-source voltage  |            | -   | 15   | V    |
| $I_D$     | drain current        |            | -   | 12   | A    |
| $T_{stg}$ | storage temperature  |            | -65 | +150 | °C   |
| $T_j$     | junction temperature |            | -   | 200  | °C   |

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol        | Parameter                                             | Conditions                                                                        | Typ | Unit |
|---------------|-------------------------------------------------------|-----------------------------------------------------------------------------------|-----|------|
| $Z_{th(j-h)}$ | transient thermal impedance from junction to heatsink | $T_h = 25\text{ °C}$ ;<br>$t_p = 200\text{ }\mu\text{s}$ ; $\delta = 12\text{ %}$ | 0.4 | K/W  |

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

| Symbol        | Parameter                        | Conditions                                                    | Min | Typ  | Max | Unit          |
|---------------|----------------------------------|---------------------------------------------------------------|-----|------|-----|---------------|
| $V_{(BR)DSS}$ | drain-source breakdown voltage   | $V_{GS} = 0\text{ V}; I_D = 2.1\text{ mA}$                    | 65  | -    | -   | V             |
| $V_{GS(th)}$  | gate-source threshold voltage    | $V_{DS} = 10\text{ V}; I_D = 180\text{ mA}$                   | 2.5 | 3.1  | 3.5 | V             |
| $V_{GSq}$     | gate-source quiescent voltage    | $V_{DS} = 28\text{ V}; I_{DS} = 900\text{ mA}$                | -   | 3.3  | 4.5 | V             |
| $I_{DSS}$     | drain leakage current            | $V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$                   | -   | -    | 2   | $\mu\text{A}$ |
| $I_{DSX}$     | drain cut-off current            | $V_{GS} = V_{GS(th)} + 9\text{ V}; V_{DS} = 10\text{ V}$      | 27  | 30   | -   | A             |
| $I_{GSS}$     | gate leakage current             | $V_{GS} = 15\text{ V}; V_{DS} = 0\text{ V}$                   | -   | -    | 200 | nA            |
| $g_{fs}$      | forward transconductance         | $V_{DS} = 10\text{ V}; I_D = 10\text{ A}$                     | -   | 9.0  | -   | S             |
| $R_{DS(on)}$  | drain-source on-state resistance | $V_{GS} = V_{GS(th)} + 6\text{ V}; I_D = 6\text{ A}$          | -   | 0.09 | -   | $\Omega$      |
| $C_{rs}$      | feedback capacitance             | $V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$ | -   | 2.5  | -   | pF            |

## 7. Application information

**Table 7. Application information**

RF performance in common source class-AB circuit;  $T_h = 25\text{ }^{\circ}\text{C}$ ;  $t_p = 200\text{ }\mu\text{s}$ ;  $\delta = 12\text{ }\%$ ;  $Z_{th(mb-h)} = 0.15\text{ K/W}$ ; unless otherwise specified.

| Symbol             | Parameter                             | Conditions | Min    | Typ | Max | Unit          |
|--------------------|---------------------------------------|------------|--------|-----|-----|---------------|
| $f_{oper}$         | operating frequency                   |            | 2.9    | -   | 3.3 | GHz           |
| $V_{CC}$           | supply voltage                        |            | -      | -   | 32  | V             |
| $t_p$              | pulse duration                        |            | -      | 200 | -   | $\mu\text{s}$ |
| $\delta$           | duty cycle                            |            | -      | 12  | -   | %             |
| $P_L$              | output power                          |            | 100    | -   | -   | W             |
| $P_{L(1dB)}$       | output power at 1 dB gain compression |            | -      | 120 | -   | W             |
| $G_p$              | power gain                            |            | 6      | 8   | -   | dB            |
| $\eta_D$           | drain efficiency                      |            | 33     | 40  | -   | %             |
| $P_{droop(pulse)}$ | pulse droop power                     |            | -      | 0.1 | 0.5 | dB            |
| $t_r$              | rise time                             |            | -      | 20  | 50  | ns            |
| $t_f$              | fall time                             |            | -      | 6   | 50  | ns            |
| $VSWR_{load}$      | load voltage standing wave ratio      |            | 10 : 1 | -   | -   |               |
| IRL                | input return loss                     |            | -      | -10 | -   | dB            |

Table 8. Typical impedance

| f<br>GHz | Z <sub>S</sub><br>Ω | Z <sub>L</sub><br>Ω |
|----------|---------------------|---------------------|
| 2.9      | 3.3 – j5.6          | 3.5 – j3.3          |
| 3.0      | 3.7 – j5.3          | 3.1 – j3.6          |
| 3.1      | 5.9 – j5.8          | 3.3 – j3.3          |
| 3.2      | 6.8 – j3.4          | 3.2 – j3.5          |
| 3.3      | 6.6 – j2.7          | 3.1 – j3.6          |

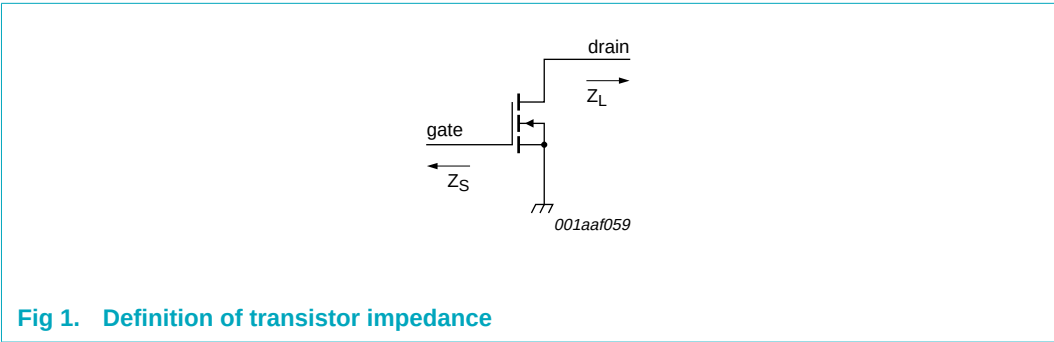
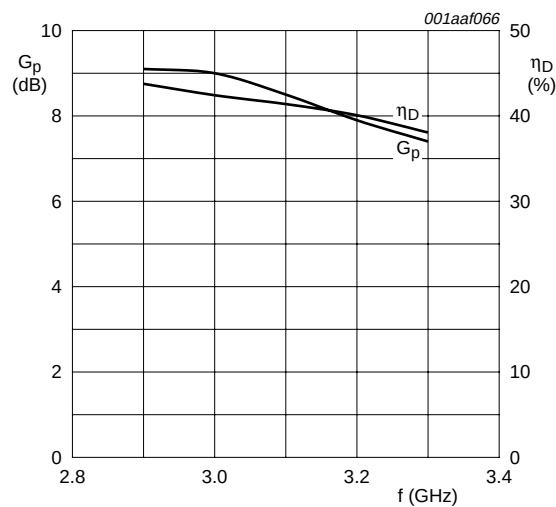


Fig 1. Definition of transistor impedance

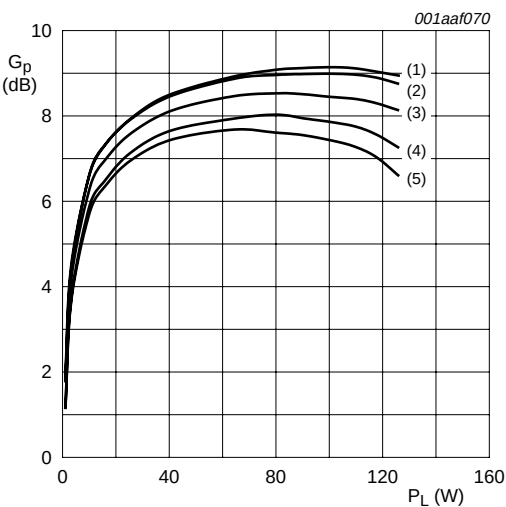
7.1 Ruggedness in class-AB operation

The BLS2933-100 is capable of withstanding a load mismatch corresponding to  $V_{SWR} > 10 : 1$  through all phases under the following conditions:  $V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 20\text{ mA}$ ;  $P_L = 100\text{ W}$  pulsed,  $t_p = 200\text{ }\mu\text{s}$ ;  $\delta = 12\text{ }\%$ .



$V_{DS} = 32$  V;  $I_{Dq} = 20$  mA;  $t_p = 200$   $\mu$ s;  $\delta = 12$  %;  
 $P_L = 100$  W.

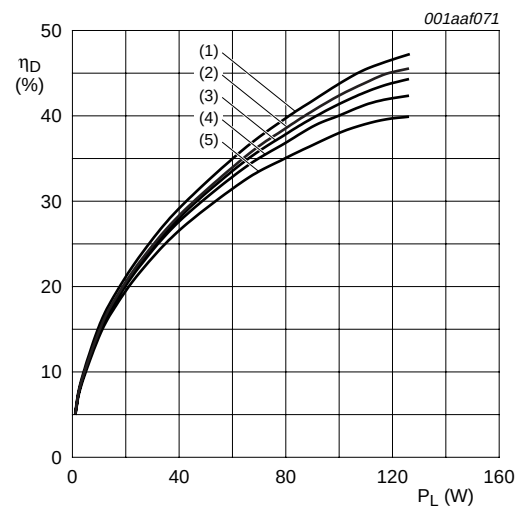
Fig 2. Power gain and drain efficiency as functions of frequency; typical values



- (1)  $f = 2.9$  MHz.
- (2)  $f = 3.0$  MHz.
- (3)  $f = 3.1$  MHz.
- (4)  $f = 3.2$  MHz.
- (5)  $f = 3.3$  MHz.

$V_{DS} = 32$  V;  $I_{Dq} = 20$  mA;  $t_p = 200$   $\mu$ s;  $\delta = 12$  %.

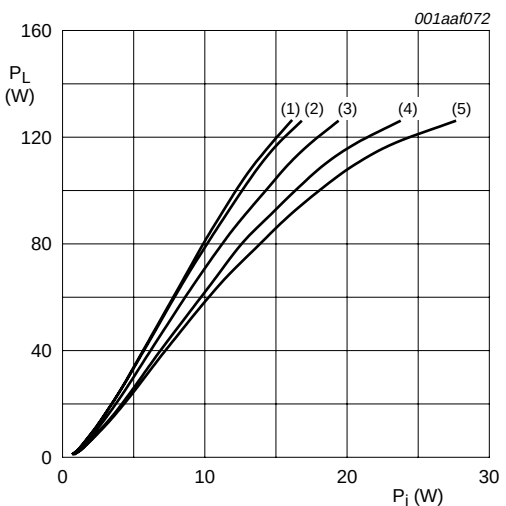
Fig 3. Power gain as a function of load power; typical values



- (1)  $f = 2.9$  MHz.
- (2)  $f = 3.0$  MHz.
- (3)  $f = 3.1$  MHz.
- (4)  $f = 3.2$  MHz.
- (5)  $f = 3.3$  MHz.

$V_{DS} = 32$  V;  $I_{Dq} = 20$  mA;  $t_p = 200$   $\mu$ s;  $\delta = 12$  %.

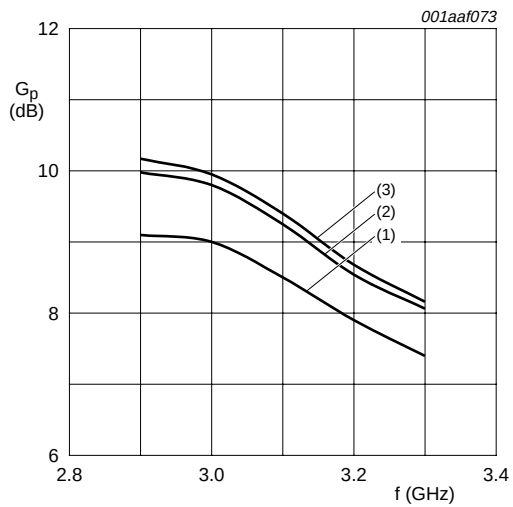
Fig 4. Efficiency as a function of power load; typical values



- (1)  $f = 2.9$  MHz.
- (2)  $f = 3.0$  MHz.
- (3)  $f = 3.1$  MHz.
- (4)  $f = 3.2$  MHz.
- (5)  $f = 3.3$  MHz.

$V_{DS} = 32$  V;  $I_{Dq} = 20$  mA;  $t_p = 200$   $\mu$ s;  $\delta = 12$  %.

Fig 5. Load power as a function of input power; typical values



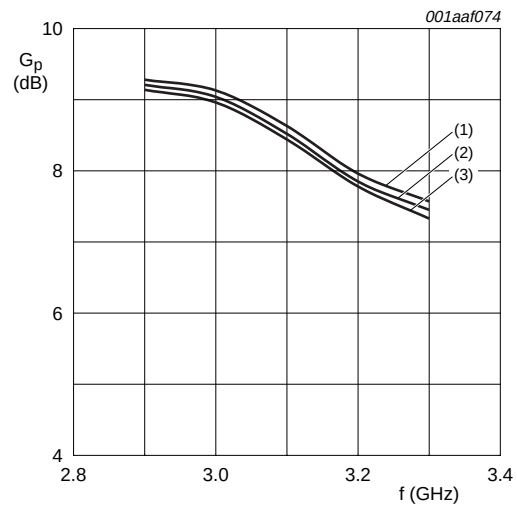
(1)  $I_{Dq} = 20 \text{ mA}$ .

(2)  $I_{Dq} = 150 \text{ mA}$ .

(3)  $I_{Dq} = 500 \text{ mA}$ .

$V_{DS} = 32 \text{ V}$ ;  $I_{Dq} = 20 \text{ mA}$ ;  $t_p = 200 \text{ }\mu\text{s}$ ;  $\delta = 12 \text{ }\%$ ;  
 $P_L = 100 \text{ W}$ .

**Fig 6. Power gain as a function of frequency and  $I_{Dq}$ ; typical values**



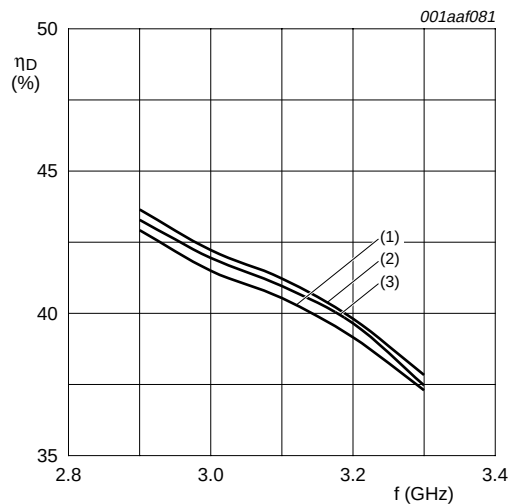
(1)  $t_p = 100 \text{ }\mu\text{s}$ .

(2)  $t_p = 300 \text{ }\mu\text{s}$ .

(3)  $t_p = 500 \text{ }\mu\text{s}$ .

$V_{DS} = 32 \text{ V}$ ;  $I_{Dq} = 20 \text{ mA}$ ;  $t_p = 100 \text{ }\mu\text{s}$ ,  $200 \text{ }\mu\text{s}$  and  
 $500 \text{ }\mu\text{s}$ ;  $\delta = 10 \text{ }\%$ ;  $P_L = 100 \text{ W}$ .

**Fig 7. Power gain as a function of frequency; typical values**



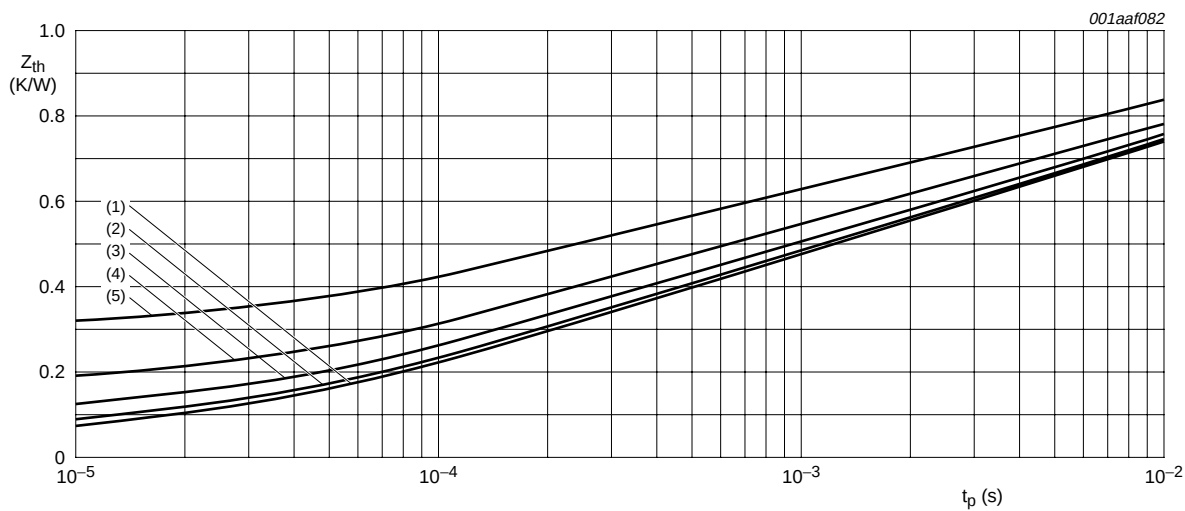
(1)  $t_p = 100 \text{ }\mu\text{s}$ .

(2)  $t_p = 300 \text{ }\mu\text{s}$ .

(3)  $t_p = 500 \text{ }\mu\text{s}$ .

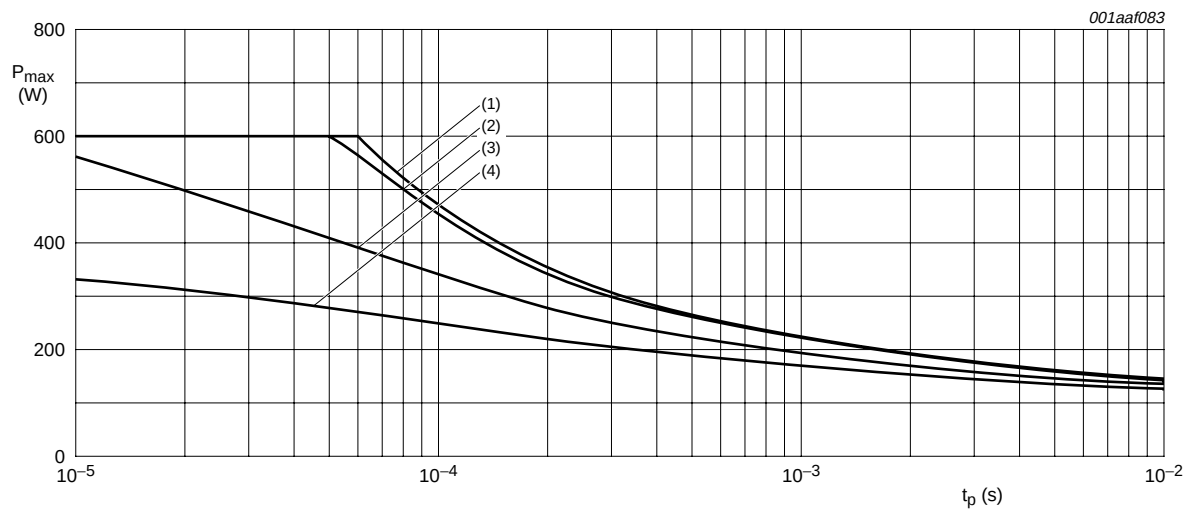
$V_{DS} = 32 \text{ V}$ ;  $I_{Dq} = 20 \text{ mA}$ ;  $\delta = 10 \text{ }\%$ ;  $P_L = 100 \text{ W}$ .

**Fig 8. Efficiency as a function of frequency; typical values**



- (1) 1 % duty cycle
- (2) 2 % duty cycle
- (3) 5 % duty cycle
- (4) 10 % duty cycle
- (5) 20 % duty cycle

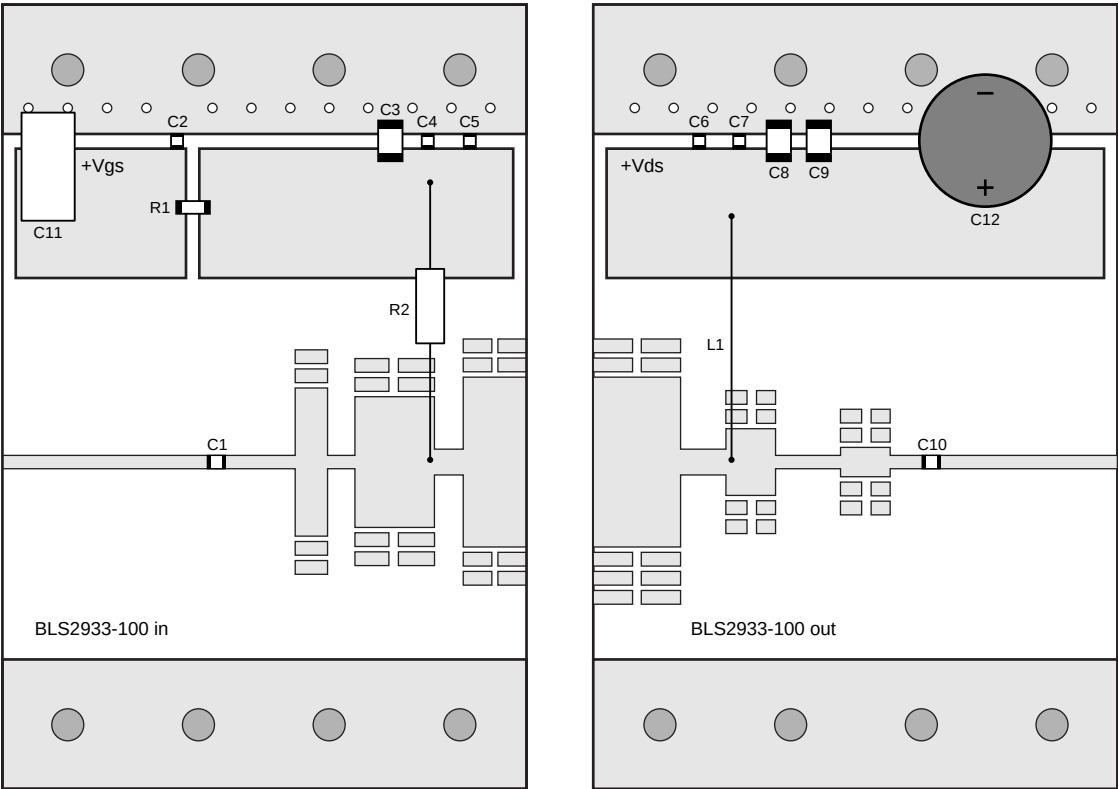
Fig 9. Thermal resistance as function of pulse duration and duty cycle; typical values



- $T_h = 70\text{ }^{\circ}\text{C}$
- (1) 1 % duty cycle
  - (2) 2 % duty cycle
  - (3) 10 % duty cycle
  - (4) 20 % duty cycle

Fig 10. Maximum allowable dissipated power as function of pulse duration and duty cycle for reaching 200 °C junction temperature

8. Test information



001aaf084

The components are situated on one side of the copper-clad Duroid 6006 Printed-Circuit Board (PCB). Both the input and output PCB are 40 mm × 60 mm with  $\epsilon_r = 6.15$  and thickness 0.64 mm.

See [Table 9](#) for list of components

Fig 11. Component layout for test circuit

Table 9. List of components (see [Figure 11](#))

| Component                   | Description                                           | Value                 | Dimensions                                        | Catalogue number     |
|-----------------------------|-------------------------------------------------------|-----------------------|---------------------------------------------------|----------------------|
| C1, C2, C4, C5, C6, C7, C10 | multilayer ceramic chip capacitor <a href="#">[1]</a> | 22 pF                 |                                                   |                      |
| C3, C8, C9                  | multilayer ceramic chip capacitor <a href="#">[2]</a> | 470 pF                |                                                   |                      |
| C11                         | tantalum capacitor                                    | 4.7 $\mu$ F; 50 V     |                                                   | Kemet T491D475K050AS |
| C12                         | electrolytic capacitor                                | 220 $\mu$ F; 63 V     |                                                   |                      |
| R1                          | resistor                                              | 560 $\Omega$          | SMD 0805                                          |                      |
| R2                          | metafilm resistor                                     | 49.9 $\Omega$ ; 0.6 W |                                                   |                      |
| L1                          | copper wire 1 mm diameter                             |                       | length of loop = 20 mm;<br>height of loop = 10 mm |                      |
| N1                          | N-connector male                                      |                       |                                                   | Suhner 13N-50-057/1  |
| N2                          | N-connector female                                    |                       |                                                   | Suhner 23N-50-057/1  |

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.



9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

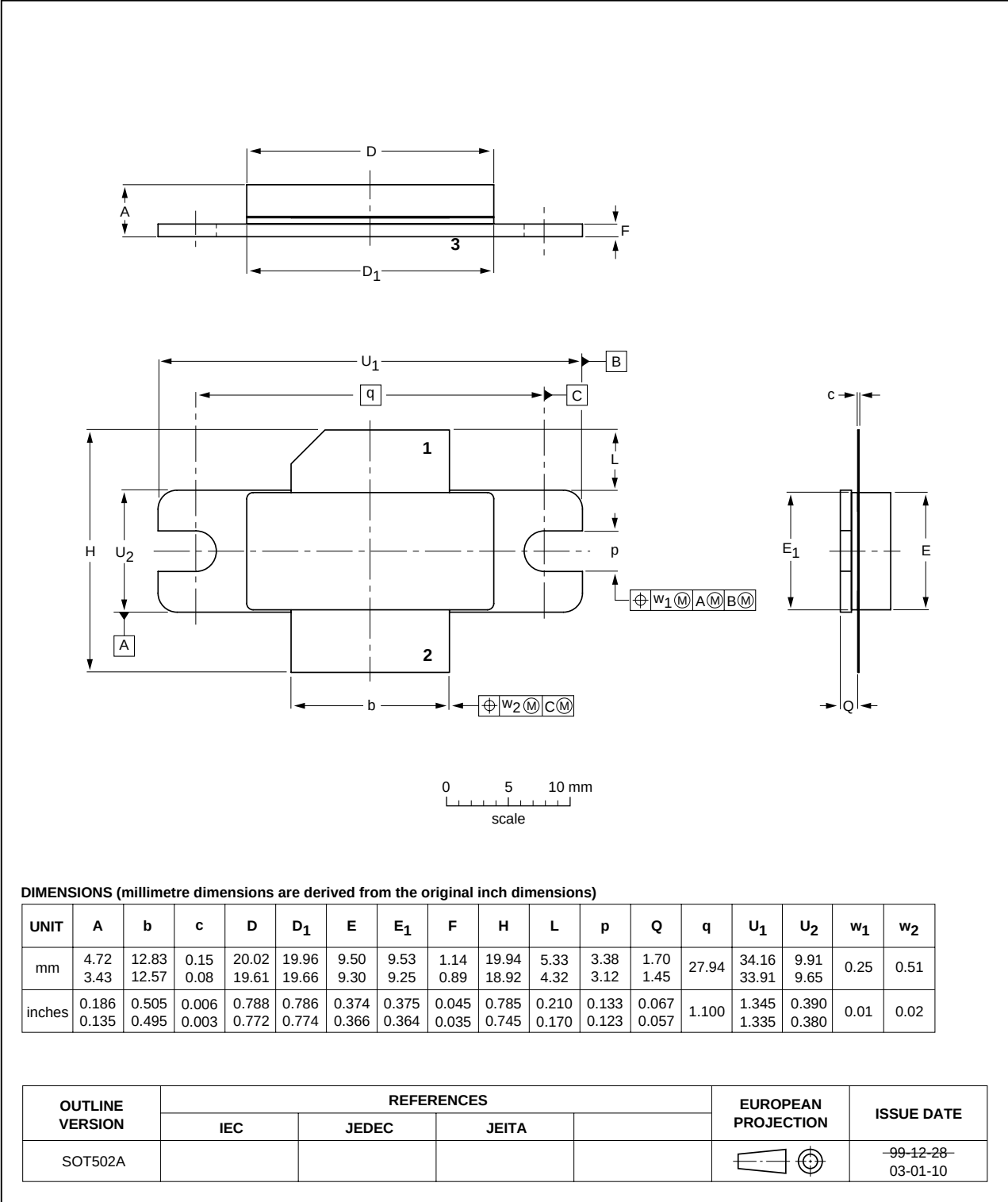


Fig 12. Package outline SOT502A

10. Revision history

Table 10. Revision history

| Document ID   | Release date | Data sheet status  | Change notice | Supersedes |
|---------------|--------------|--------------------|---------------|------------|
| BLS2933-100_1 | 20060801     | Product data sheet | -             | -          |

## 11. Legal information

### 11.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

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