

The RF MOSFET Line

RF Power Field Effect Transistors

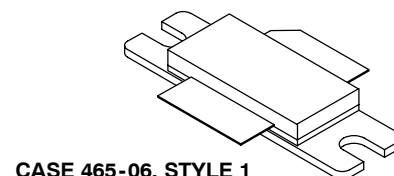
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications. Specified for GSM1805 - 1880 MHz.

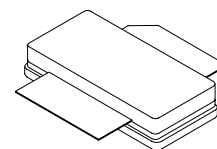
- Typical GSM Performance, Full Frequency Band (1805 - 1880 MHz)
Power Gain — 13 dB (Typ) @ 60 Watts
Efficiency — 45% (Typ) @ 60 Watts
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 60 Watts CW Output Power
- Excellent Thermal Stability
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ" Nominal.
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 Inch Reel.

MRF18060AR3
MRF18060ASR3
MRF18060ALSR3

1.80 - 1.88 GHz, 60 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF18060AR3



CASE 465A-06, STYLE 1
NI-780S
MRF18060ASR3, MRF18060ALSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C \geq 25^\circ\text{C}$ Derate above 25°C	P_D	180 1.03	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	$^\circ\text{C}/\text{W}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

NOTE - CAUTION - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 10 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	6	μAdc
Gate-Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2	—	4	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 500 mAdc)	V _{GS(Q)}	2.5	3.9	4.5	Vdc
Drain-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.27	—	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.7	—	S

DYNAMIC CHARACTERISTICS

Input Capacitance (Including Input Matching Capacitor in Package) (1) (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{iss}	—	160	—	pF
Output Capacitance (1) (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{oss}	—	740	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	2.7	—	pF

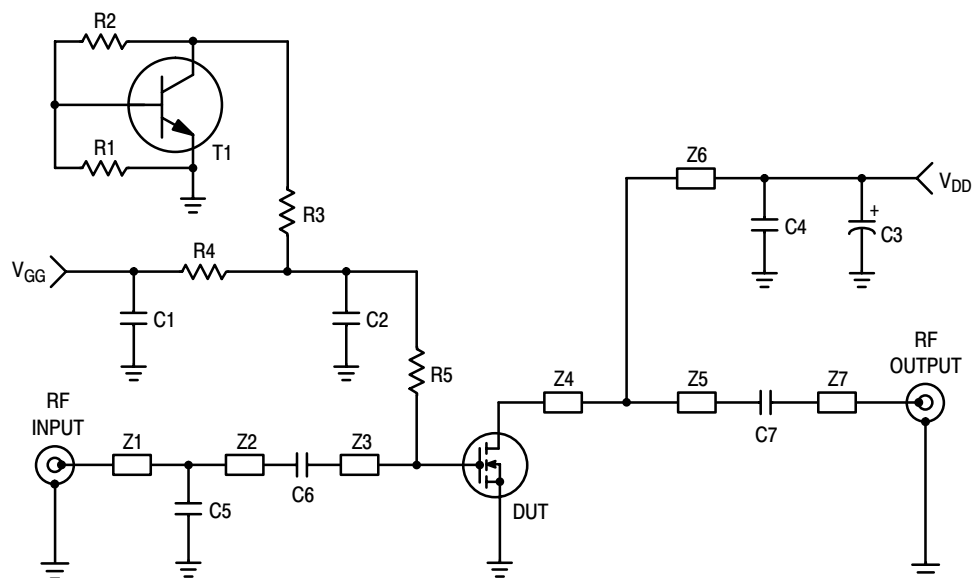
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Common-Source Amplifier Power Gain @ 60 W (2) (V _{DD} = 26 Vdc, I _{DQ} = 500 mA, f = 1805 - 1880 MHz)	G _{ps}	11.5	13	—	dB
Drain Efficiency @ 60 W (2) (V _{DD} = 26 Vdc, I _{DQ} = 500 mA, f = 1805 - 1880 MHz)	η	43	45	—	%
Input Return Loss (2) (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 500 mA, f = 1805 - 1880 MHz)	IRL	—	—	- 10	dB
Output Mismatch Stress (V _{DD} = 26 Vdc, P _{out} = 60 W CW, I _{DQ} = 500 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch-to-batch consistency.

Freescale Semiconductor, Inc.



C1	100 nF Chip Capacitor (1203)	Z1	0.47" x 0.09" Microstrip
C2, C4, C7	10 pF Chip Capacitors	Z2	1.16" x 0.09" Microstrip
C3	10 μ F, 35 V Electrolytic Tantalum Capacitor	Z3	0.57" x 0.95" Microstrip
C5	1.2 pF Chip Capacitor	Z4	0.59" x 1.18" Microstrip
C6	1.0 pF Chip Capacitor	Z5	1.26" x 0.15" Microstrip
R1, R3	2.2 k Ω Chip Resistors (0805)	Z6	1.15" x 0.09" Microstrip
R2, R4	2.7 k Ω Chip Resistors (0805)	Z7	0.37" x 0.09" Microstrip
R5	1.1 k Ω Chip Resistor (0805)		
T1	BC847 Transistor SOT-23		

Figure 1. 1805 - 1880 MHz Test Fixture Schematic

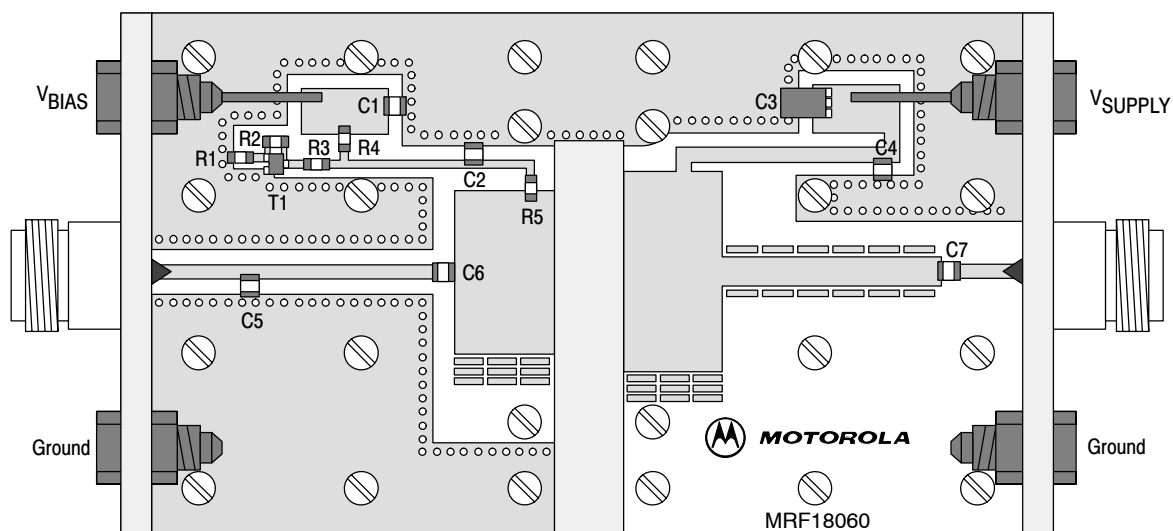


Figure 2. 1805 - 1880 MHz Test Fixture Component Layout

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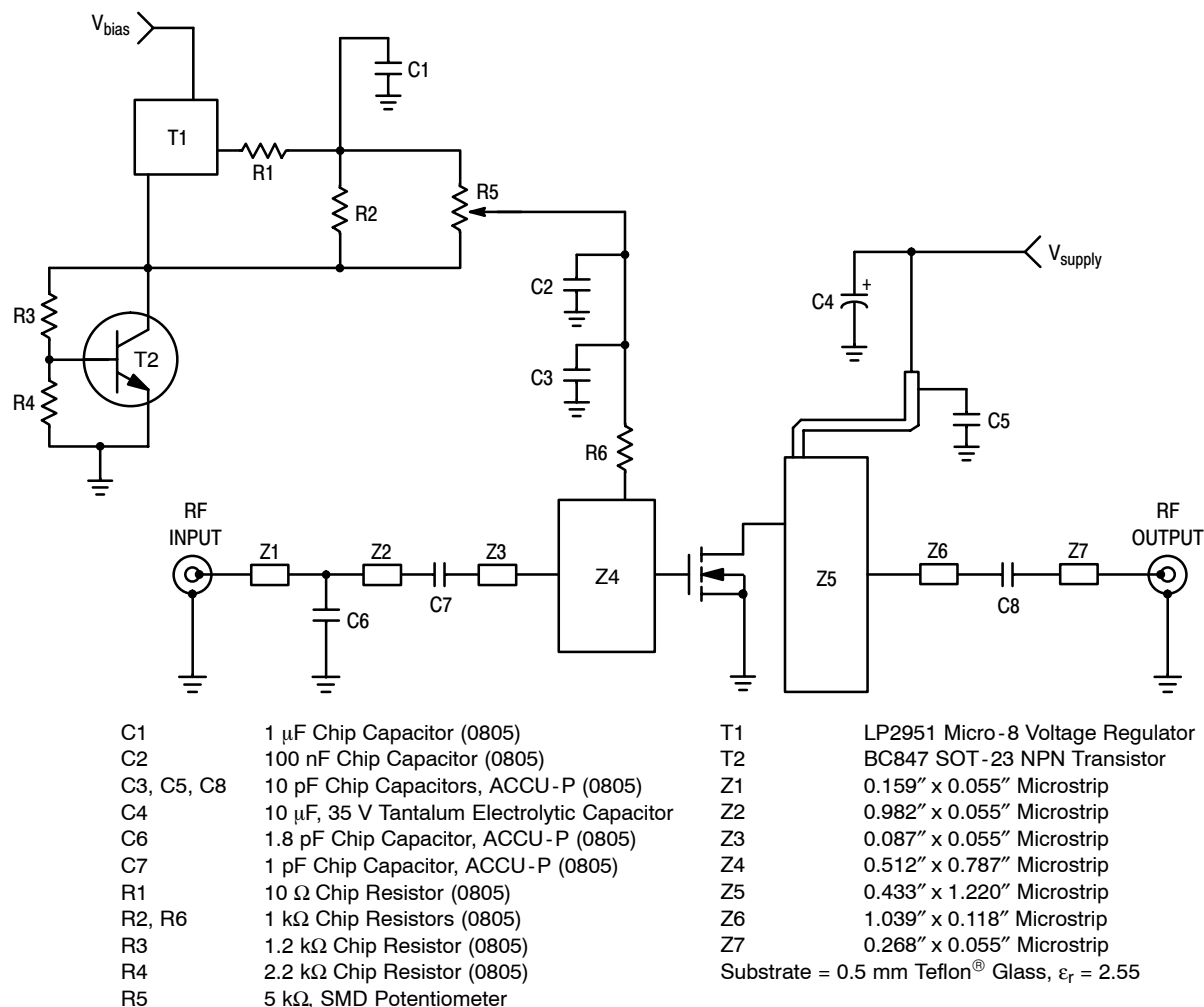


Figure 3. 1800 - 2000 MHz Demo Board Schematic

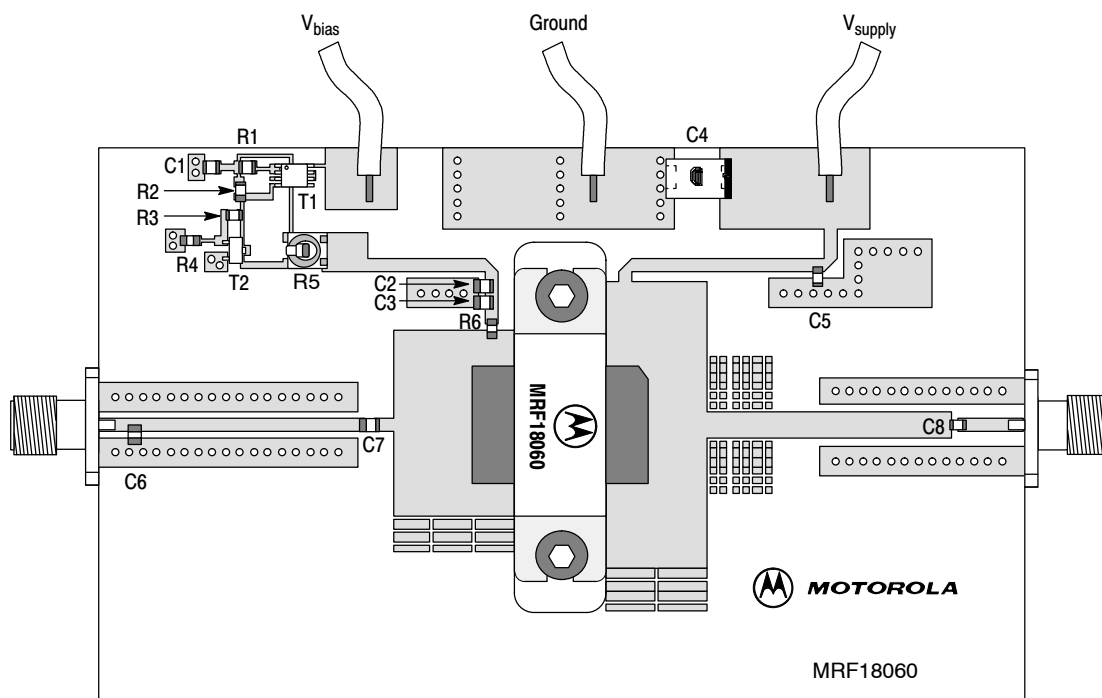


Figure 4. 1800 - 2000 MHz Demo Board Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS (DATA TAKEN USING WIDEBAND DEMONSTRATION BOARD)

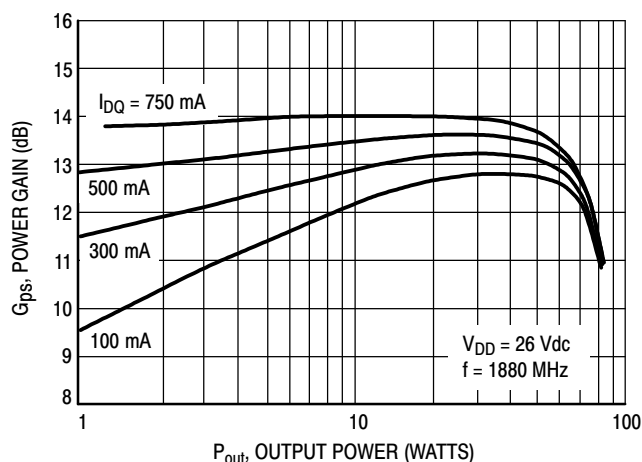


Figure 5. Power Gain versus Output Power

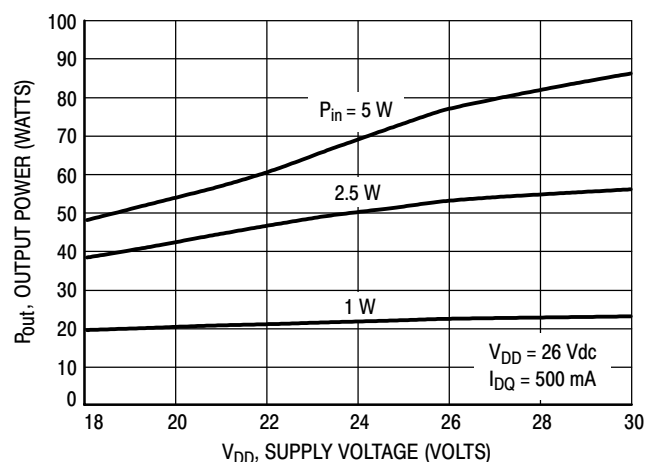


Figure 6. Output Power versus Supply Voltage

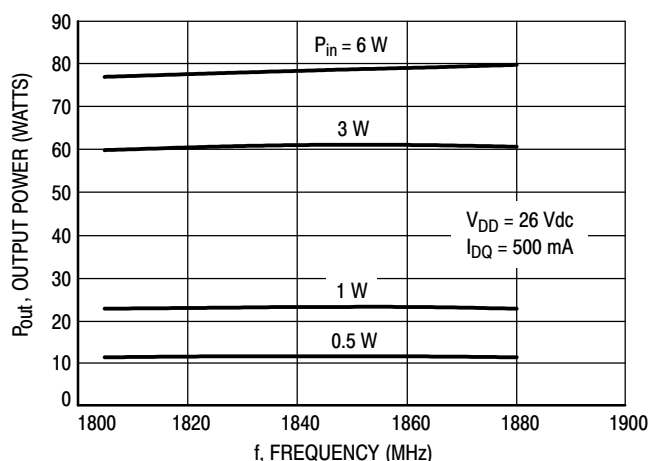


Figure 7. Output Power versus Frequency

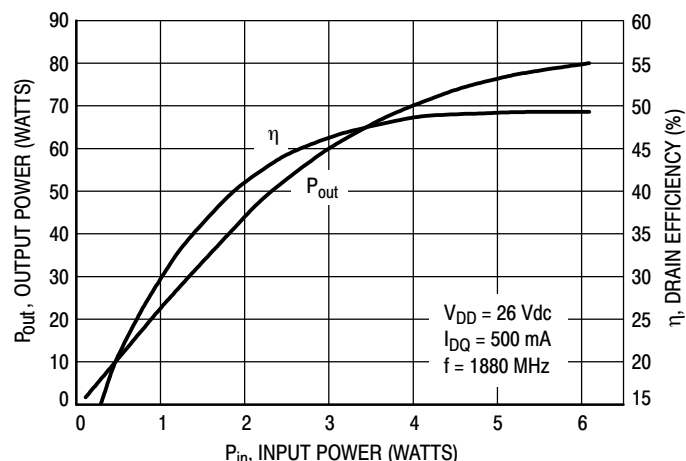


Figure 8. Output Power and Efficiency versus Input Power

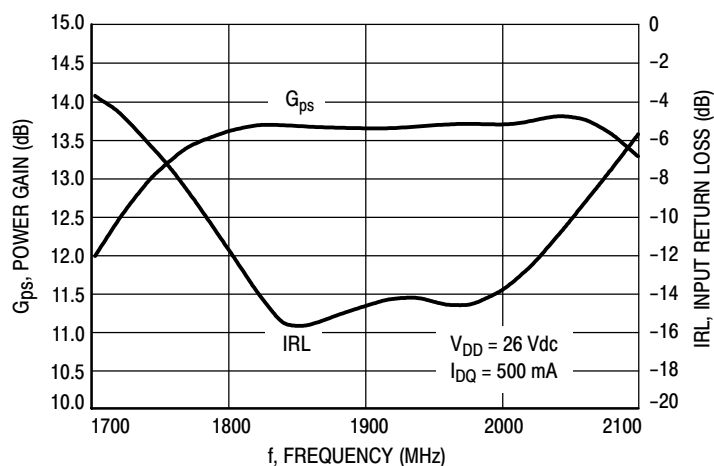
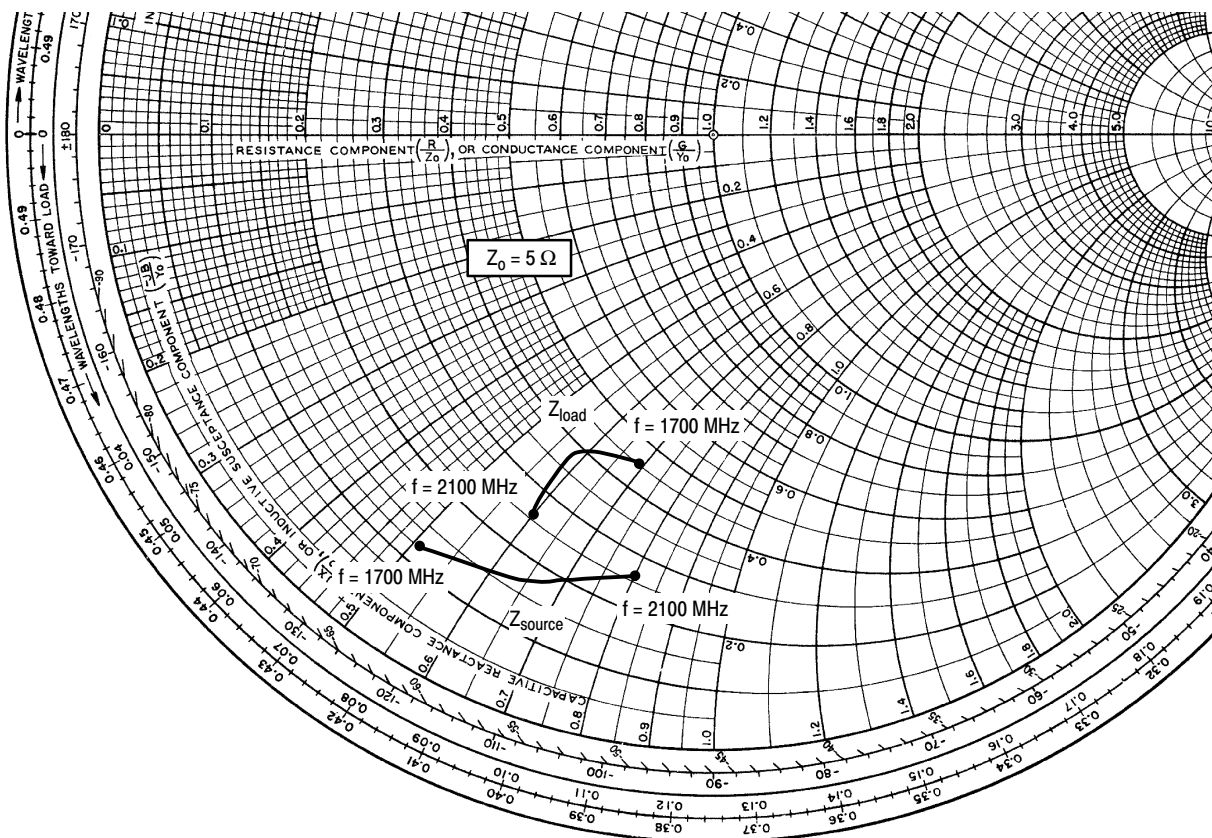


Figure 9. Wideband Gain and IRL (at Small Signal)



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 60 \text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
1700	$0.60 - j2.53$	$2.27 - j3.44$
1800	$0.80 - j3.20$	$2.05 - j3.05$
1900	$0.92 - j3.42$	$1.90 - j2.90$
2000	$1.07 - j3.59$	$1.64 - j2.88$
2100	$1.31 - j4.00$	$1.29 - j2.99$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

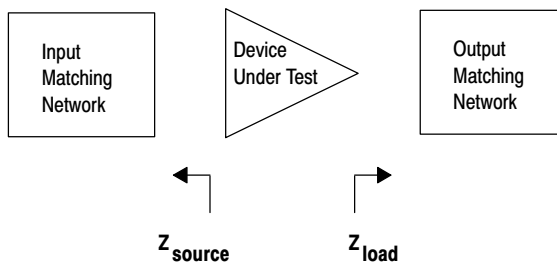
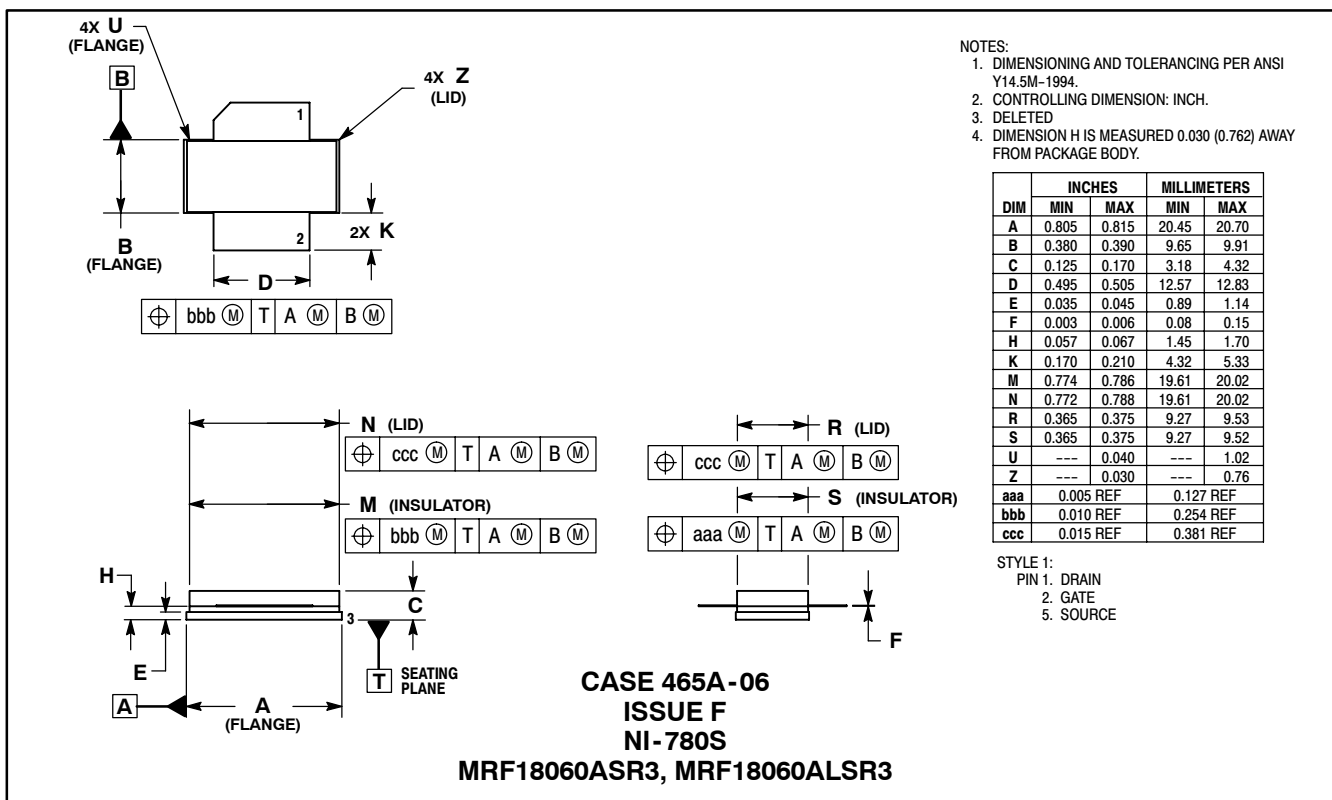
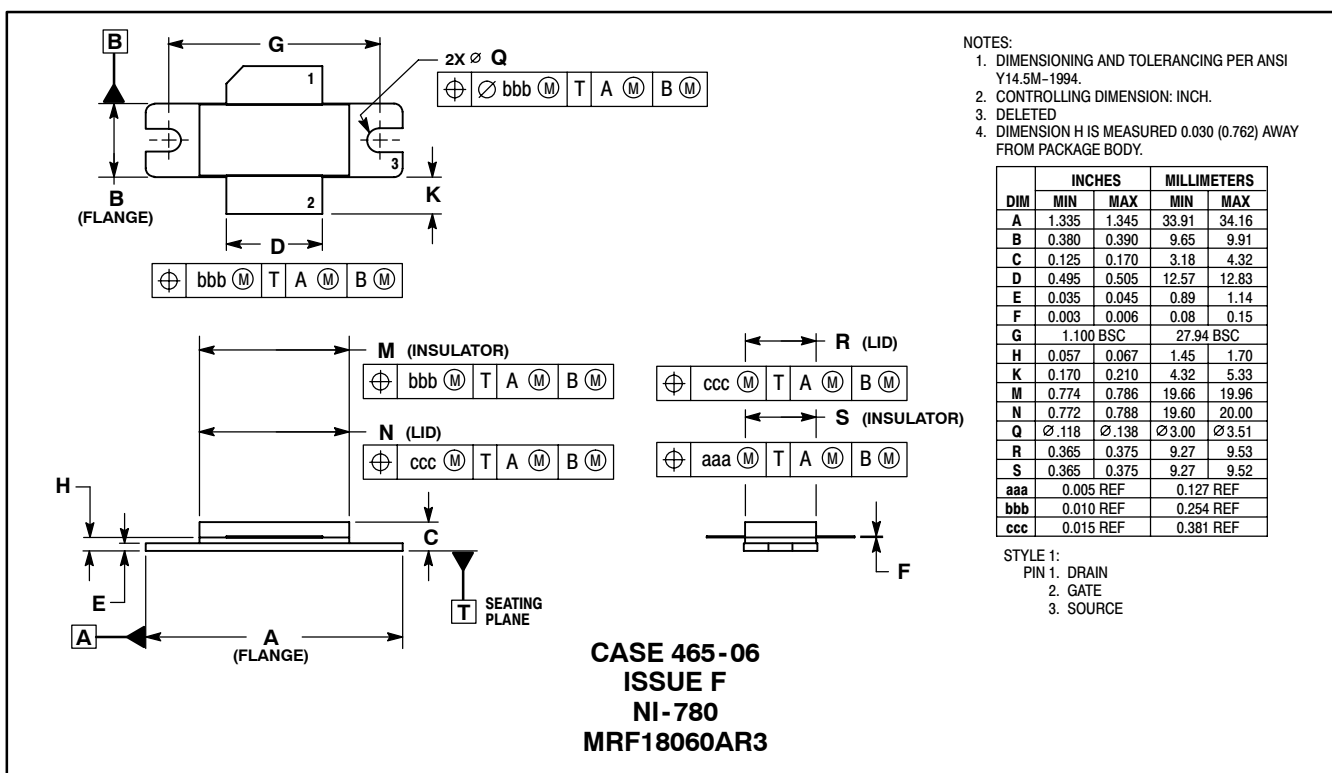


Figure 10. Series Equivalent Source and Load Impedance

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PACKAGE DIMENSIONS



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