

74F377

Octal D-Type Flip-Flop with Clock Enable

General Description

The 74F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The CE input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

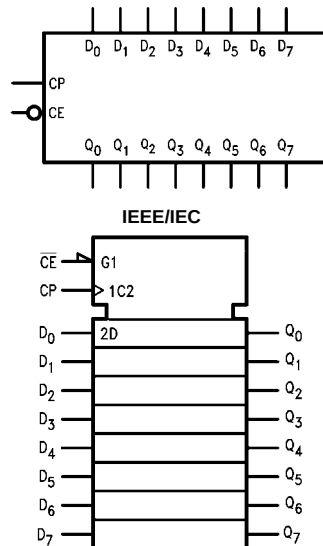
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- See 74F273 for master reset version
- See 74F373 for transparent latch version
- See 74F374 for 3-STATE version

Ordering Code:

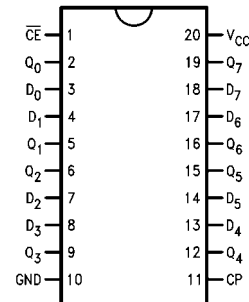
Order Number	Package Number	Package Description
74F377SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F377SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F377PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

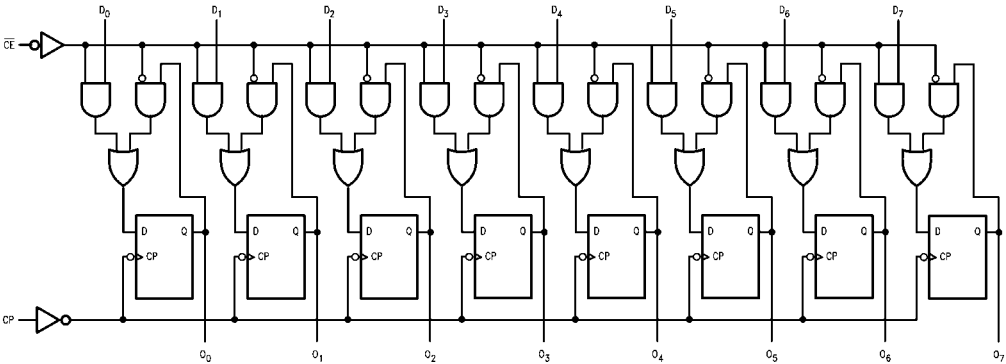
Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0-D_7	Data Inputs	1.0/1.0	$20\ \mu A/-0.6\ mA$
$\overline{CE}$	Clock Enable (Active LOW)	1.0/1.0	$20\ \mu A/-0.6\ mA$
CP	Clock Pulse Input	1.0/1.0	$20\ \mu A/-0.6\ mA$
Q_0-Q_7	Data Outputs	50/33.3	$-1\ mA/20\ mA$

Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↗	L	h	H
Load "0"	↗	L	L	L
Hold	↗	h	X	No Change
(Do Nothing)	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↗ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

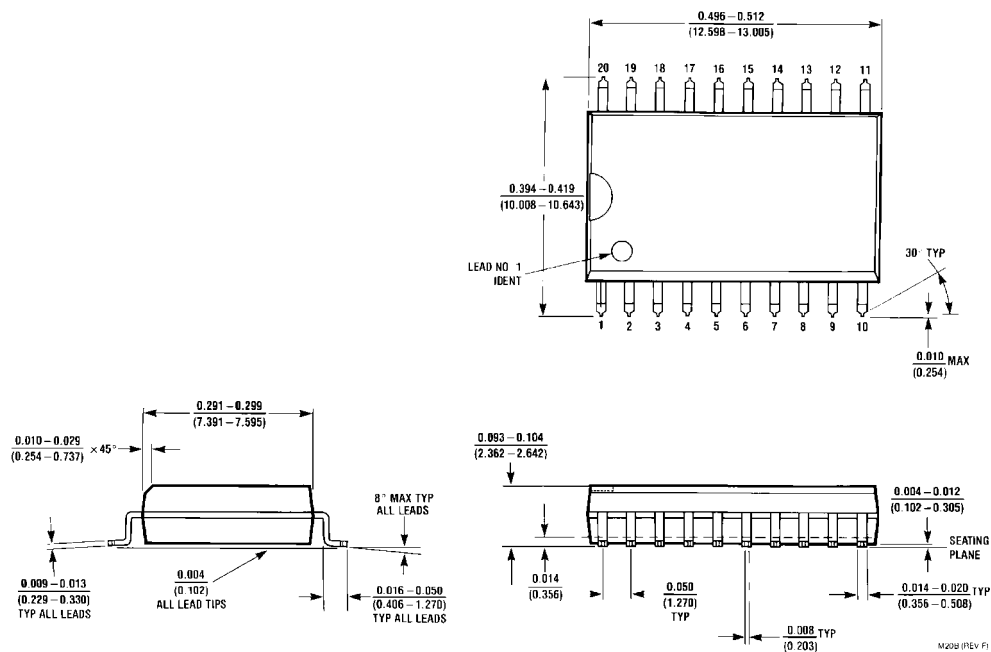
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.5 2.7		V	Min	I _{OH} = −1 mA I _{OH} = −1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			−0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V _{OUT} = 0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{ID} = 150 mV All Other Pins Grounded
I _{CCH}	Power Supply Current		35	46	mA	Max	CP = 
I _{CCL}			44	56			D _n = MR = HIGH

AC Electrical Characteristics

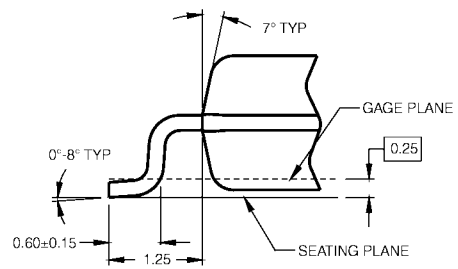
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	130			85		105		MHz
t _{PLH}	Propagation Delay	3.0		7.0	2.0	8.5	2.5	7.5	ns
t _{PHL}	CP to Q _n	4.0		9.0	3.0	10.5	3.5	9.0	

AC Operating Requirements

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	3.0		3.5		3.0		ns
t _S (L)	D _n to CP	3.5		4.0		3.5		
t _H (H)	Hold Time, HIGH or LOW	0.5		1.0		0.5		ns
t _H (L)	D _n to CP	1.0		1.0		1.0		
t _S (H)	Setup Time, HIGH or LOW	4.1		4.0		4.1		ns
t _S (L)	$\overline{\text{CE}}$ to CP	3.5		5.0		4.0		
t _H (H)	Hold Time, HIGH to LOW	0.5		1.5		0.5		ns
t _H (L)	$\overline{\text{CE}}$ to CP	2.0		2.5		2.0		
t _W (H)	Clock Pulse Width,	6.0		5.0		6.0		ns
t _W (L)	HIGH or LOW	6.0		5.0		6.0		



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**



DETAIL A

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.

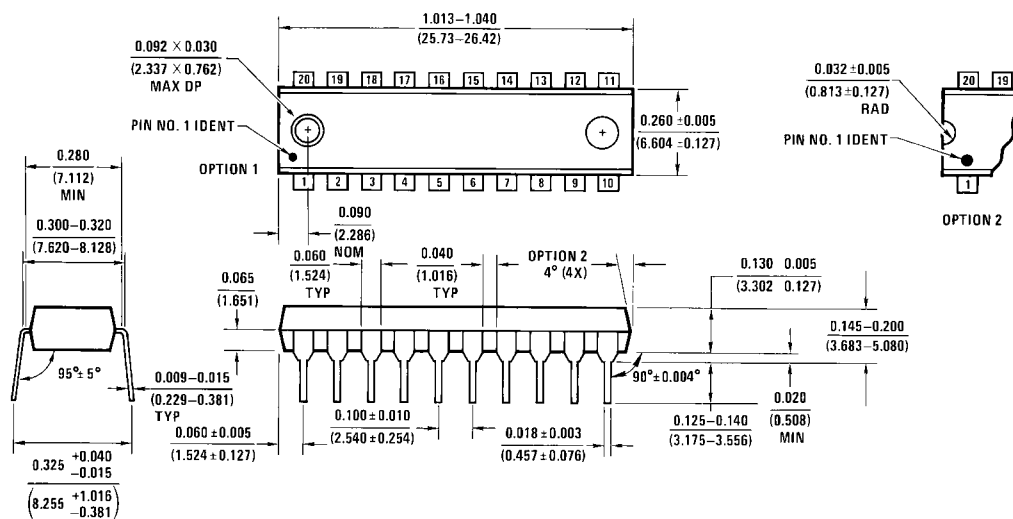
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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