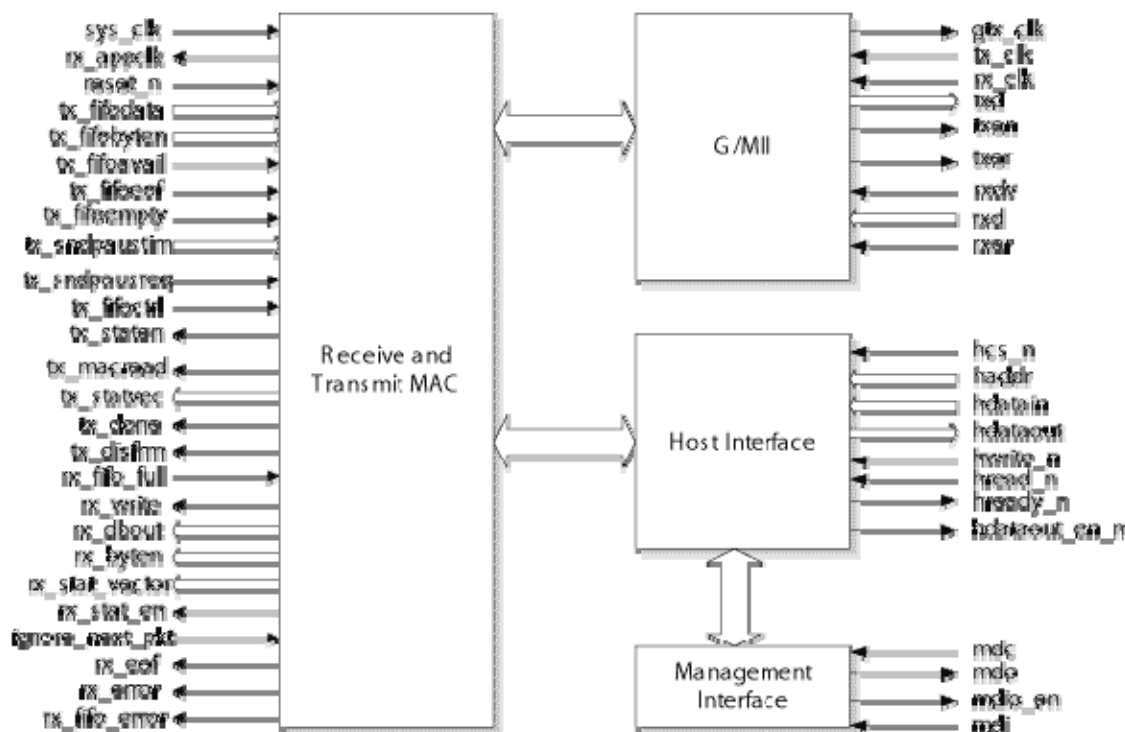


## Ethernet MAC Cores

### Overview

The Ethernet Media Access Controller (MAC) core can be configured to operate in either the Gigabit mode (1000 Mbits/sec data rate) or the Fast Ethernet mode (10/100 Mbits/sec data rate). Netlist configurations of this core operate only in either the Gigabit mode or Fast Ethernet mode. The netlist cannot auto-negotiate between the two different modes.

The Ethernet MAC transmits and receives data between a host processor and an Ethernet network. The main function of the Ethernet MAC is to ensure that the Media Access rules specified in the 802.3 IEEE standard are met while transmitting a frame of data over Ethernet. Figure 2 shows the transmission of data on the Ethernet network using the frame format. On the receiving side, the Ethernet MAC extracts the different components of a frame and transfers them to higher applications through the FIFO interface.



### Features

- Compliant to IEEE 802.3z Standard
- Generic Host Interface
- Configurable 8-bit or 16-bit and Greater Data Bus
- 16-bit Wide Internal Data Path
- Full-duplex Operation in Gigabit Mode
- Full and Half Duplex in 10/100 Mode
- Transmit and Receive Statistics Vector
- Programmable Inter Packet Gap (IPG)
- Multicast Address Filtering
- Supports:
  - Full-duplex Control Using PAUSE Frames
  - VLAN Tagged Frames
  - Automatic Re-transmission on Collision

Automatic Padding of Short Frames  
 Optional FCS Transmission and Reception  
 Optional MII Management Interface Module

Supports Jumbo Frames up to 8192 kbytes

Reference Design for GMII to RGMII Bridge

Reduced pincount Gigabit Media Independent Interface

## Evaluation Configurations

Evaluation Configurations Available for Series 4 ORCA FPGAs and FPSCs<sup>1</sup>

| Name of Parameter File | <a href="#">ether_fast_o4_3_002.lpc</a>                | <a href="#">ether_1gig_o4_3_001.lpc</a> |
|------------------------|--------------------------------------------------------|-----------------------------------------|
| Mode (Mbps)            | 10/100                                                 | 1000                                    |
| CPU Data Width         | 16                                                     | 16                                      |
| MIIM Module            | Yes                                                    | No                                      |
| LUTs                   | 2581                                                   | 1747                                    |
| ORCA 4 PFUs            | 548                                                    | 364                                     |
| Registers              | 1850                                                   | 1313                                    |
| External Pins          | 198                                                    | 201                                     |
| System EBRs (RAM512)   | 2                                                      | 1                                       |
| fMAX (MHz)             | 62.5 MHz sys_clk,<br>25MHz MII host clks<br>(PHY side) | 125MHz (GMII)                           |

<sup>1</sup> Performance and utilization characteristics using ispLEVER™ software and targeting the ORCA4E04-2BA352C. When using this IP Core in a different density, package, speed or grade within the ORCA 4 family, performance may vary.

Evaluation Configurations Available for ispXPGA<sup>1</sup>

| Name of Parameter File | <a href="#">ether_1gig_xp_1_001.lpc</a> | <a href="#">ether_fast_xp_1_002.lpc</a>                |
|------------------------|-----------------------------------------|--------------------------------------------------------|
| Mode (Mbps)            | 1000                                    | 10/100                                                 |
| CPU Data Width         | 16                                      | 16                                                     |
| MIIM Module            | No                                      | Yes                                                    |
| LUTs                   | 2084                                    | 3545                                                   |
| PFUs                   | 744                                     | 1156                                                   |
| Registers              | 1502                                    | 2179                                                   |
| External Pins          | 201                                     | 198                                                    |
| System EBRs            | 4                                       | 2                                                      |
| fMAX                   | 125 MHz (GMII)                          | 62.5 MHz sys_clk,<br>25MHz MII host clks<br>(PHY side) |

<sup>1</sup> Performance and utilization characteristics using ispLEVER™ software and targeting the LFX500B-04FH516C device. The evaluation version of this IP core only works on this specific device density, package, and speed grade.

Evaluation Configurations Available for LatticeECP and LatticeEC<sup>1</sup>

| Name of Parameter File | <a href="#">ether_1gig_e2_3_001.lpc</a> | <a href="#">ether_fast_e2_3_006.lpc</a>                |
|------------------------|-----------------------------------------|--------------------------------------------------------|
| Mode (Mbps)            | 1000                                    | 10/100                                                 |
| CPU Data Width         | 16                                      | 16                                                     |
| MIIM Module            | No                                      | Yes                                                    |
| LUT4s                  | 1681                                    | 2712                                                   |
| SLICEs                 | 1318                                    | 1892                                                   |
| Registers              | 1339                                    | 1792                                                   |
| I/Os                   | 201                                     | 198                                                    |
| System EBRs            | 2                                       | 4                                                      |
| fMAX                   | 125 MHz (GMII)                          | 62.5 MHz sys_clk,<br>25MHz MII host clks<br>(PHY side) |

<sup>1</sup> Performance and utilization characteristics are generated using LFEC20E-4F672C in Lattice ispLEVER v.4.1 software. When using this IP core in a different density, package, or speed grade, performance may vary.

Evaluation Configurations Available for LatticeXP<sup>1</sup>

| Name of Parameter File | <a href="#">ether_1gig_xm_3_001.lpc</a> | <a href="#">ether_fast_xm_3_006.lpc</a>                |
|------------------------|-----------------------------------------|--------------------------------------------------------|
| Mode (Mbps)            | 1000                                    | 10/100                                                 |
| CPU Data Width         | 16                                      | 16                                                     |
| MIIM Module            | No                                      | Yes                                                    |
| LUT4s                  | 1730                                    | 3008                                                   |
| SLICEs                 | 1328                                    | 1892                                                   |
| Registers              | 1340                                    | 1839                                                   |
| I/Os                   | 201                                     | 198                                                    |
| System EBRs            | 2                                       | 4                                                      |
| fMAX                   | 125 MHz (GMII)                          | 62.5 MHz sys_clk,<br>25MHz MII host clks<br>(PHY side) |

<sup>1</sup> Performance and utilization characteristics are generated using LFXP10C-4F388C in Lattice ispLEVER 5.0 software. When using this IP core in a different density, package, or speed grade, performance may vary.

Evaluation Configurations Available for LatticeSC<sup>1</sup>

| Name of Parameter File | <a href="#">ether_1gig_sc_3_001.lpc</a> | <a href="#">ether_fast_sc_3_006.lpc</a> |
|------------------------|-----------------------------------------|-----------------------------------------|
| Mode (Mbps)            | 1000                                    | 10/100                                  |
| CPU Data Width         | 16                                      | 16                                      |
| MIIM Module            | No                                      | Yes                                     |

| Name of Parameter File | <a href="#">ether_1gig_sc_3_001.lpc</a> | <a href="#">ether_fast_sc_3_006.lpc</a>                |
|------------------------|-----------------------------------------|--------------------------------------------------------|
| <b>LUT4s</b>           | 1929                                    | 2856                                                   |
| <b>SLICES</b>          | 1301                                    | 1910                                                   |
| <b>Registers</b>       | 1333                                    | 1831                                                   |
| <b>I/Os</b>            | 201                                     | 198                                                    |
| <b>System EBRs</b>     | 1                                       | 2                                                      |
| <b>fMAX</b>            | 125 MHz (GMII)                          | 62.5 MHz sys_clk,<br>25MHz MII host clks<br>(PHY side) |

## Ordering Information

### Part Numbers:

For ORCA 4 Fast Ethernet : ETHER-FAST-O4-N3

For ORCA 4 Gigabit: ETHER-1GIG-O4-N3

For ispXPGA Fast Ethernet: ETHER-FAST-XP-N3

For ispXPGA Gigabit: ETHER-1GIG-XP-N3

For LatticeECP/EC Fast Ethernet: ETHER-FAST-E2-N3

For LatticeECP/EC Gigabit: ETHER-1GIG-E2-N3

For LatticeXP Fast Ethernet: ETHER-FAST-XM-N3

For LatticeXP Gigabit: ETHER-1GIG-XM-N3

For LatticeSC Fast Ethernet: ETHER-FAST-SC-N3

For LatticeSC Gigabit: ETHER-1GIG-SC-N3

To find out how to purchase the Ethernet MAC IP Cores, please contact your **local Lattice Sales Office**.