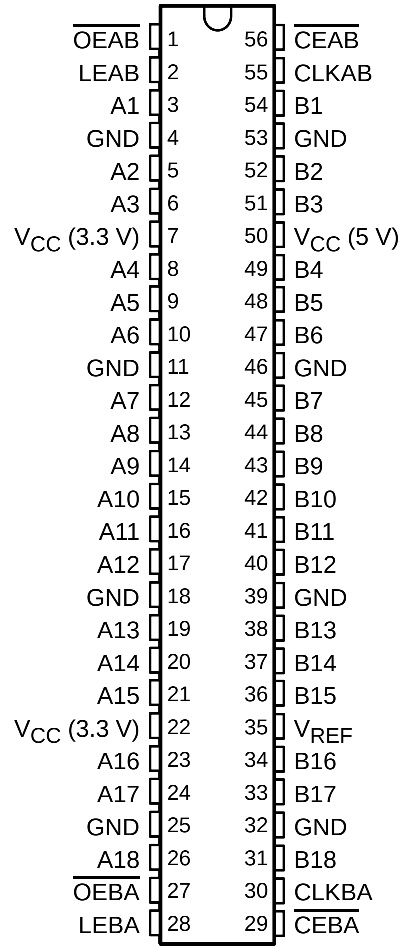
- **Member of Texas Instruments' Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (34 mA)**
- **LVTTL Outputs (–32 mA/64 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on A-Port Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG OR DL PACKAGE
(TOP VIEW)



description

The SN74GTLPH16612 is a medium-drive, 18-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It allows for transparent, latched, clocked, or clock-enabled modes of data transfer. This device provides a high-speed interface between cards operating at LVTTL logic levels and backplanes operating at GTLP signal levels. High-speed (about two times faster than standard LVTTL or TTL) backplane operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and OEC™ circuitry. These improvements minimize bus-settling time and have been designed and tested using several backplane models.

GTLP is a TI™ derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH16612 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels.

The B port normally operates at GTLP levels, while the A-port and control inputs are compatible with LVTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port.

To improve signal integrity, the SN74GTLPH16612 B-port output transition time is optimized for distributed backplane loads.

description (continued)

V_{CC} (5 V) supplies the internal and GTLP circuitry, while V_{CC} (3.3 V) supplies the LVTTL output buffers.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74GTLPH16612DL	GTLPH16612
		Tape and reel	SN74GTLPH16612DLR	
	TSSOP – DGG	Tape and reel	SN74GTLPH16612GR	GTLPH16612

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional description

The SN74GTLPH16612 is a medium-drive (34 mA), 18-bit UBT transceiver, containing D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH16612 UBT Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	’245, ’623, ’645	’863	’861	’16245, ’16623	’16863
Buffer/driver	’241, ’244, ’541		’827	’16241, ’16244, ’16541	’16825
Latched transceiver	’543			’16543	’16472
Latch	’373, ’573	’843	’841	’16373	’16843
Registered transceiver	’646, ’652			’16646, ’16652	’16474
Flip-flop	’374, ’574		’821	’16374	
Standard UBT					’16500, ’16501
Universal bus driver					’16835
Registered transceiver with clock enable	’2952			’16470, ’16952	
Flip-flop with clock enable	’377	’823			’16823
Standard UBT with clock enable					’16600, ’16601
SN74GTLPH16612 UBT transceiver replaces all above functions					

Data flow in each direction is controlled by the clock enables ($\overline{CEAB}$ and $\overline{CEBA}$), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA), and output enables ($\overline{OEAB}$ and $\overline{OEBA}$).

For A-to-B data flow, when $\overline{CEAB}$ is low, the device operates on the low-to-high transition of CLKAB for the flip-flop and on the high-to-low transition of LEAB for the latch path, i.e., if $\overline{CEAB}$ and LEAB are low, the A data is latched, regardless of the state of CLKAB (high or low) and if LEAB is high, the device is in transparent mode. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state.

The data flow for B-to-A is similar to that of A-to-B, except that $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA are used.

FUNCTION TABLE†

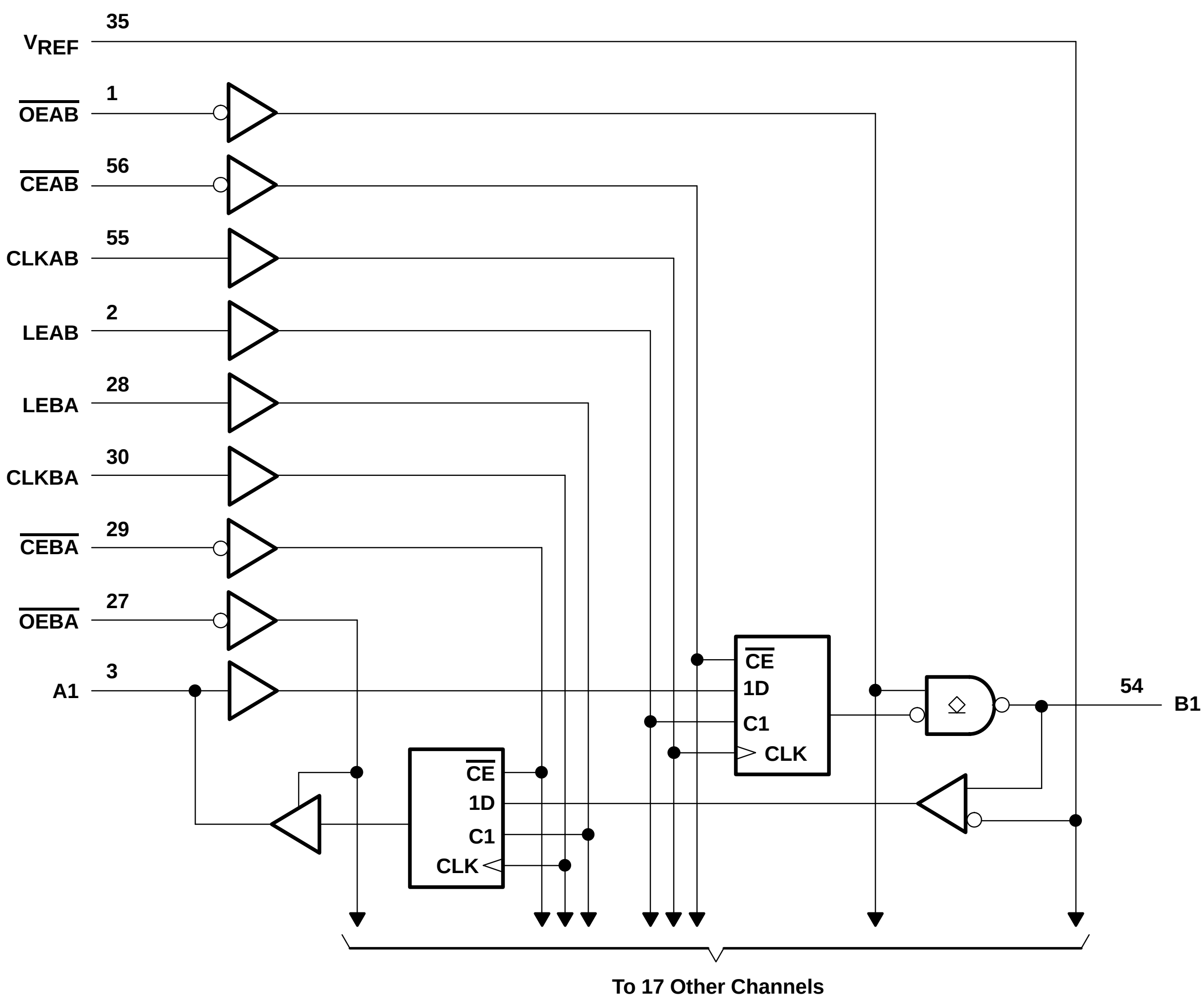
INPUTS					OUTPUT	MODE
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Isolation
L	L	L	H	X	B_0‡	Latched storage of A data
L	L	L	L	X	B_0§	
X	L	H	X	L	L	True transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0§	Clock inhibit

† A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA. The condition when $\overline{OEAB}$ and $\overline{OEBA}$ are both low at the same time is not recommended.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: 3.3 V . . . . –0.5 V to 4.6 V
5 V . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1): A port and control inputs . . . . –0.5 V to 7 V
B port and V_{REF} . . . . –0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1): A port . . . . –0.5 V to 7 V
B port . . . . –0.5 V to 4.6 V
Current into any output in the low state, I_O: A port . . . . 128 mA
B port . . . . 80 mA
Current into any A port output in the high state, I_O (see Note 2) . . . . 64 mA
Continuous current through each V_{CC} or GND . . . . ±100 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . 64°C/W
DL package . . . . 56°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 7)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3.3 V	3.15	3.3	3.45	V
		5 V	4.75	5	5.25	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port	V_{REF}+50 mV			V
		Except B port	2			
V_{IL}	Low-level input voltage	B port			V_{REF}–50 mV	V
		Except B port			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port			–32	mA
I_{OL}	Low-level output current	A port			64	mA
		B port			34	
T_A	Operating free-air temperature		–40		85	°C

NOTES: 4. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first, V_{CC} = 5 V second, and V_{CC} = 3.3 V, I/O, control inputs, V_{TT}, and V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
7. V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port	V_{CC} (3.3 V) = 3.15 V to 3.45 V, V_{CC} (5 V) = 4.75 V to 5.25 V		I_{OH} = –100 μA	V_{CC} (3.3 V) –0.2			V
		V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	I_{OH} = –8 mA	2.4			
				I_{OH} = –32 mA	2			
V_{OL}	A port	V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	I_{OL} = 100 μA			0.2	V
				I_{OL} = 16 mA			0.4	
				I_{OL} = 32 mA			0.5	
				I_{OL} = 64 mA			0.55	
	B port	V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V,	I_{OL} = 34 mA			0.65	
I_I	Control inputs	V_{CC} (3.3 V) = 0 or 3.45 V,	V_{CC} (5 V) = 0 or 5.25 V,	V_I = 5.5 V			10	μA
	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V	V_I = 5.5 V			20	
				V_I = V_{CC} (3.3 V)			1	
				V_I = 0			–30	
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V	V_I = V_{CC} (3.3 V)			5	
				V_I = 0			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				100	μA
$I_{I(hold)}$	A port	V_{CC} (3.3 V) = 3.15 V,	V_{CC} (5 V) = 4.75 V	V_I = 0.8 V	75			μA
				V_I = 2 V	–75			
				V_I = 0 to V_{CC} (3.3 V)‡			±500	
I_{OZH}	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = V_{CC} (3.3 V)			1	μA
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 1.5 V			10	
I_{OZL}	A port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 0			–1	μA
	B port	V_{CC} (3.3 V) = 3.45 V,	V_{CC} (5 V) = 5.25 V,	V_O = 0.65 V			–10	
I_{CC} (3.3 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND§, V_I = V_{TT} or GND¶		Outputs high			1	mA
				Outputs low			5	
				Outputs disabled			1	
I_{CC} (5 V)	A or B port	V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, I_O = 0, V_I = V_{CC} (3.3 V) or GND§, V_I = V_{TT} or GND¶		Outputs high			120	mA
				Outputs low			120	
				Outputs disabled			120	
ΔI_{CC} (3.3 V)#		V_{CC} (3.3 V) = 3.45 V, V_{CC} (5 V) = 5.25 V, One A-port or control input at 2.7 V, Other A-port or control inputs at V_{CC} (3.3 V) or GND					1	mA
C_i	Control inputs	V_I = 3.15 V or 0				4		pF
C_{io}	A port	V_O = 3.15 V or 0				8.5		pF
	B port	V_O = 1.5 V or 0				8		

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ This is the V_I for A-port or control inputs.
¶ This is the V_I for B port.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted) (see Figure 1)

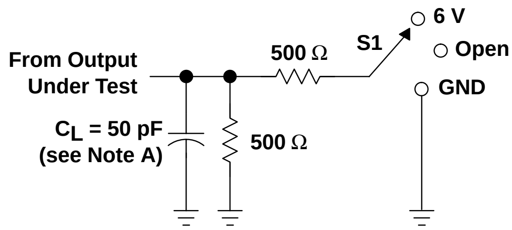
			MIN	MAX	UNIT
f_{clock}	Clock frequency			85	MHz
t_w	Pulse duration	LEAB or LEBA high	3.3		ns
		CLKAB or CLKBA high or low	5.7		
t_{su}	Setup time	A before CLKAB↑	1		ns
		B before CLKBA↑	1.8		
		A before LEAB↓	0.5		
		B before LEBA↓	1.2		
		$\overline{CEAB}$ before CLKAB↑	1.2		
		$\overline{CEBA}$ before CLKBA↑	1.4		
t_h	Hold time	A after CLKAB↑	1.9		ns
		B after CLKBA↑	0.5		
		A after LEAB↓	2.7		
		B after LEBA↓	3.5		
		$\overline{CEAB}$ after CLKAB↑	1.2		
		$\overline{CEBA}$ after CLKBA↑	1.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			85			MHz
t_{PLH}	A	B	2.5		6.9	ns
t_{PHL}			2.5		6.9	
t_{PLH}	LEAB	B	3.2		7.3	ns
t_{PHL}			3.2		7.3	
t_{PLH}	CLKAB	B	3.4		7.8	ns
t_{PHL}			3.4		7.8	
t_{en}	$\overline{OEAB}$	B	2.8		7	ns
t_{dis}			2.8		7	
t_r	Transition time, B outputs (20% to 80%)			2.6		ns
t_f	Transition time, B outputs (80% to 20%)			2.6		ns
t_{PLH}	B	A	1.5		5.7	ns
t_{PHL}			1.5		5.7	
t_{PLH}	LEBA	A	1.8		5.7	ns
t_{PHL}			1.8		5.7	
t_{PLH}	CLKBA	A	2.3		5.5	ns
t_{PHL}			2.3		5.5	
t_{en}	$\overline{OEBA}$	A	1.8		6.1	ns
t_{dis}			1.8		6.1	

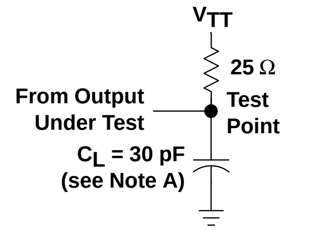
† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

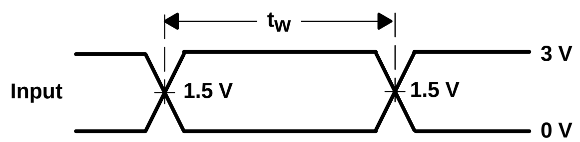


LOAD CIRCUIT FOR A OUTPUTS

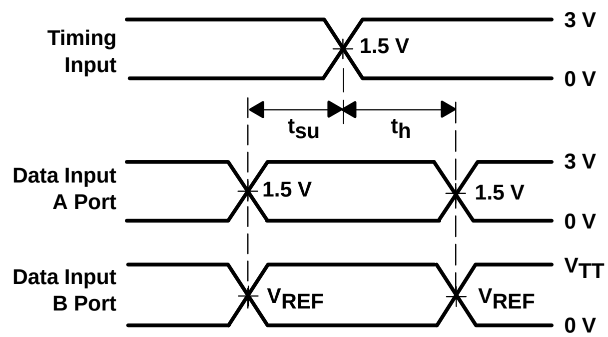
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



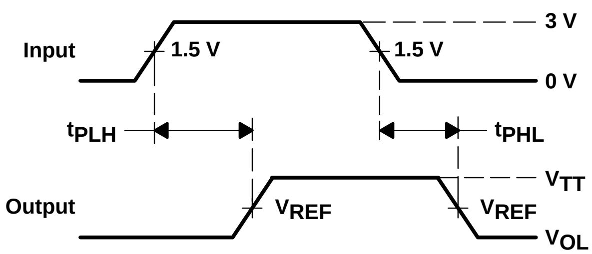
LOAD CIRCUIT FOR B OUTPUTS



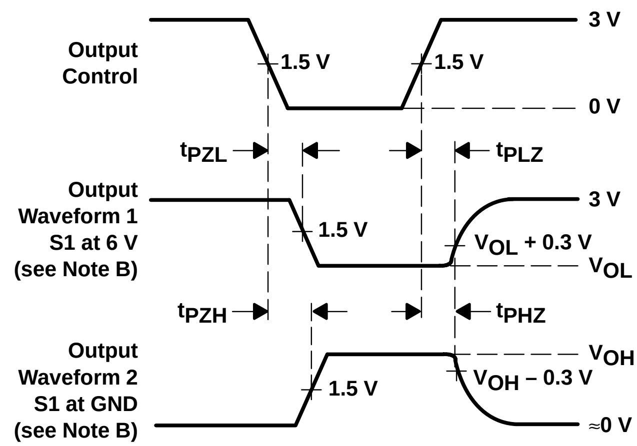
VOLTAGE WAVEFORMS
PULSE DURATION



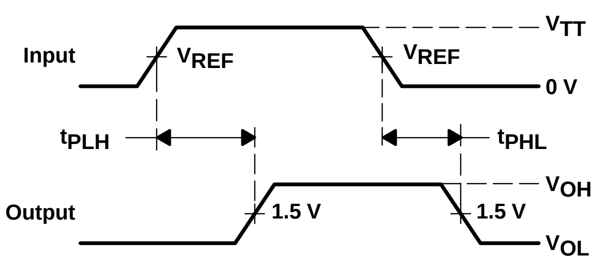
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The previous switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to an RLC circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

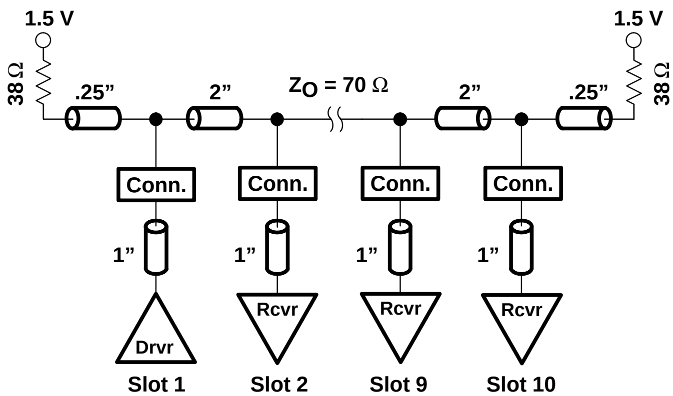


Figure 2. Medium-Drive Test Backplane

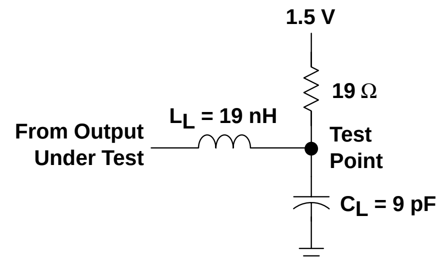


Figure 3. Medium-Drive RLC Network

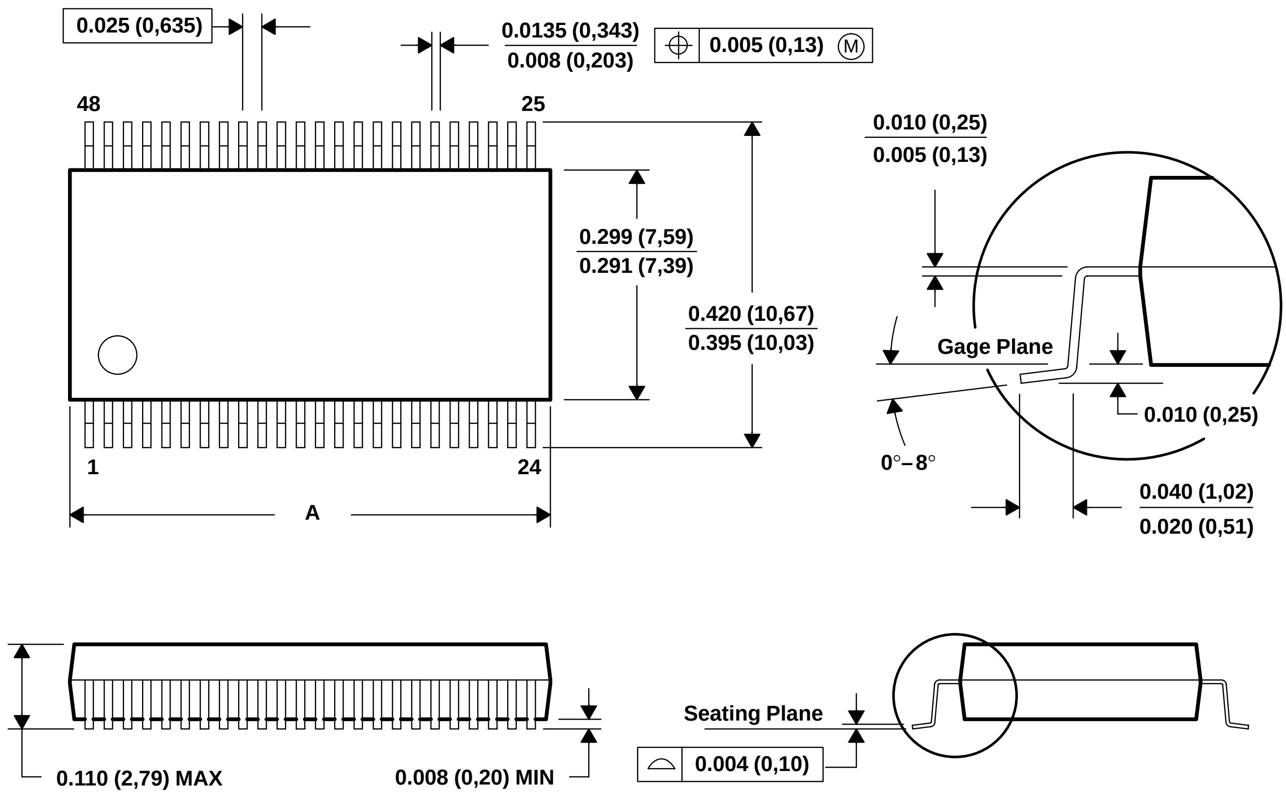
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	UNIT
f_{max}			85		MHz
t_{PLH}	A	B		3.6	ns
t_{PHL}				3.6	
t_{PLH}	LEAB	B		4.3	ns
t_{PHL}				4.3	
t_{PLH}	CLKAB	B		4.4	ns
t_{PHL}				4.4	
t_{en}	$\overline{OEAB}$	B		4.1	ns
t_{dis}				4.3	
t_r	Rise time, B outputs (20% to 80%)			1.4	ns
t_f	Fall time, B outputs (80% to 20%)			2.1	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI SPICE models.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



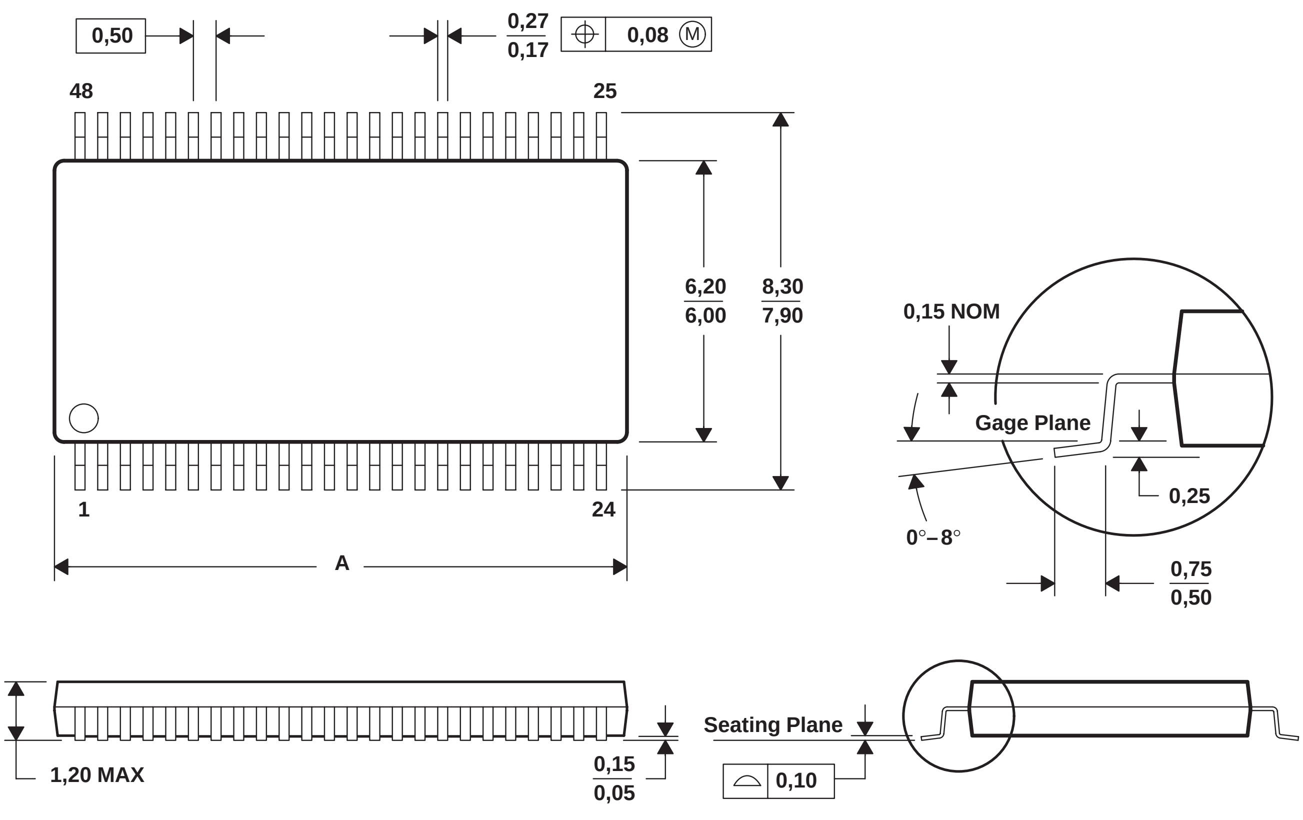
PINS ** / DIM	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

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