



74AVC20T245

20-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 9 — 25 June 2024

Product data sheet

1. General description

The 74AVC20T245 is a 20-bit, dual supply transceiver that enables bi-directional voltage level translation. The device can be used as two 10-bit transceivers or as a single 20-bit transceiver. It features four 10-bit input-output ports (1An, 1Bn and 2An, 2Bn), two output enable inputs (nOE), two direction inputs (nDIR) and dual supplies ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ and $V_{CC(B)}$ can be independently supplied at any voltage between 0.8 V and 3.6 V making the device suitable for bi-directional voltage level translation between any of the low voltage nodes: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V. The 1An and 2An ports, nOE and nDIR are referenced to $V_{CC(A)}$, the 1Bn and 2Bn ports are referenced to $V_{CC(B)}$. A HIGH on a 1DIR allows transmission from 1An to 1Bn and a LOW on 1DIR allows transmission from 1Bn to 1An. A HIGH on nOE causes the outputs to assume a HIGH impedance OFF-state.

The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, all output ports will assume a high impedance OFF-state.

2. Features and benefits

- Wide supply voltage range:
 - $V_{CC(A)}$: 0.8 V to 3.6 V
 - $V_{CC(B)}$: 0.8 V to 3.6 V
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-B (2.7 V to 3.6 V)
- Maximum data rates:
 - 380 Mbit/s (≥ 1.8 V to 3.3 V translation)
 - 260 Mbit/s (≥ 1.1 V to 3.3 V translation)
 - 260 Mbit/s (≥ 1.1 V to 2.5 V translation)
 - 210 Mbit/s (≥ 1.1 V to 1.8 V translation)
 - 120 Mbit/s (≥ 1.1 V to 1.5 V translation)
 - 100 Mbit/s (≥ 1.1 V to 1.2 V translation)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3B exceeds 8000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC20T245DGG	-40 °C to +125 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4. Functional diagram

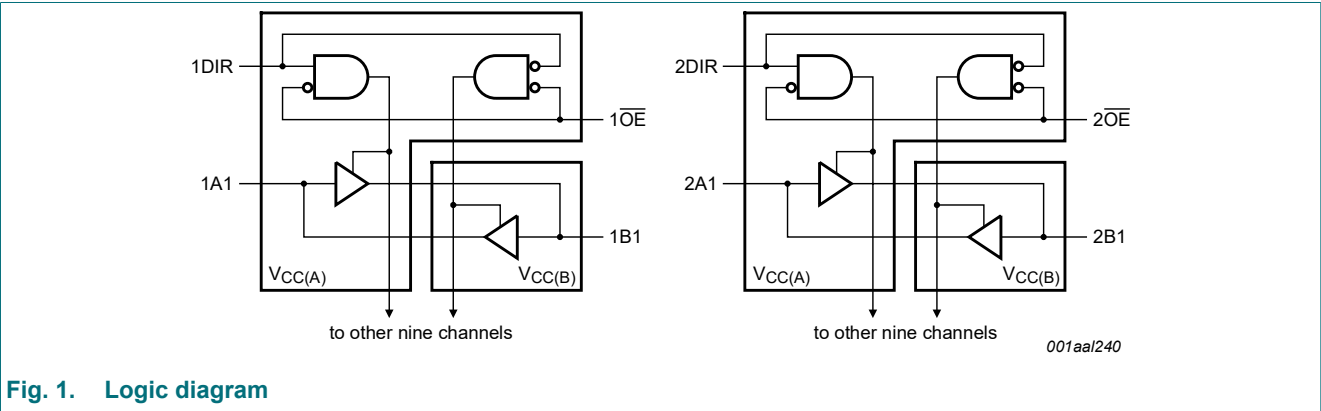


Fig. 1. Logic diagram

20-bit dual supply translating transceiver with configurable voltage translation; 3-state

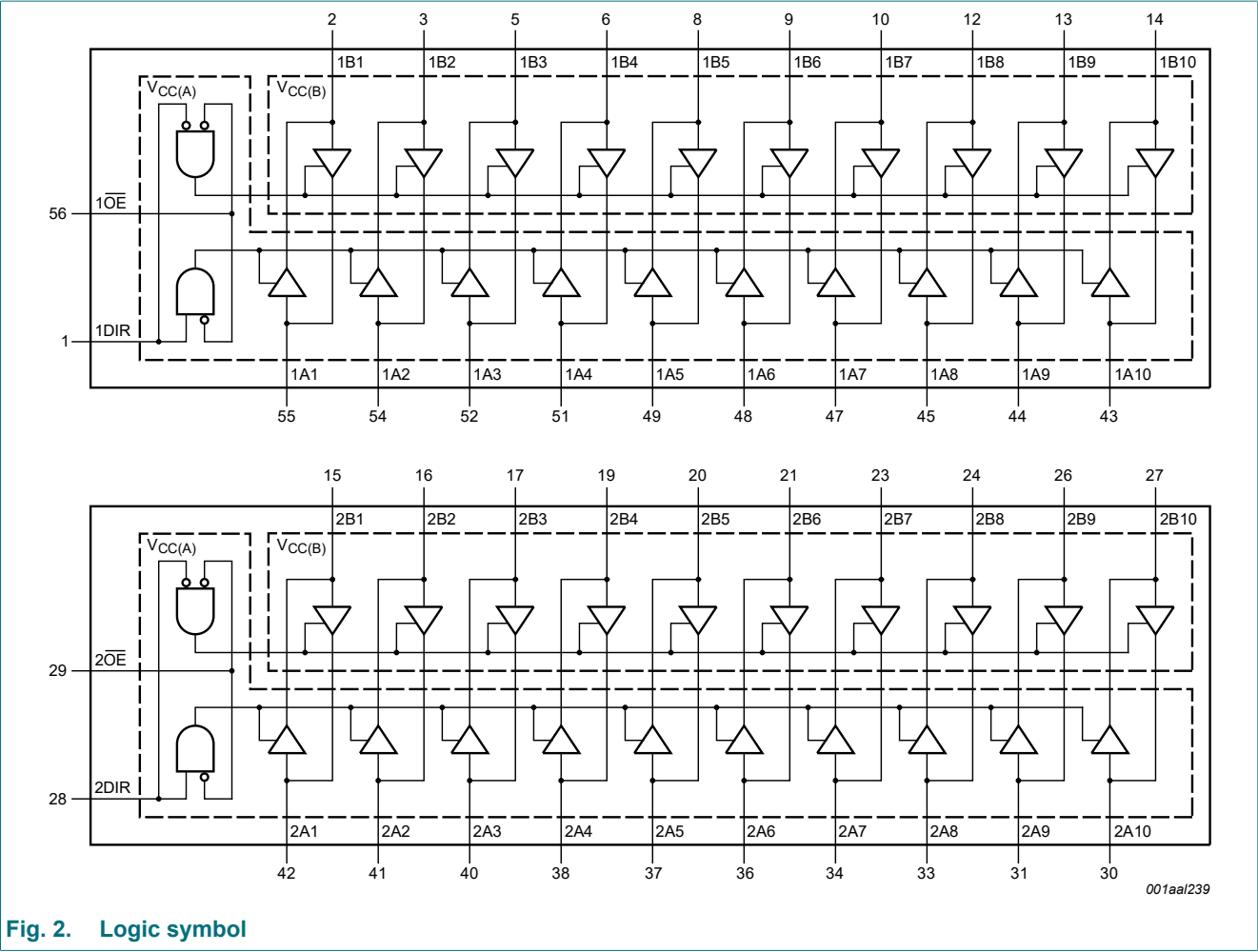
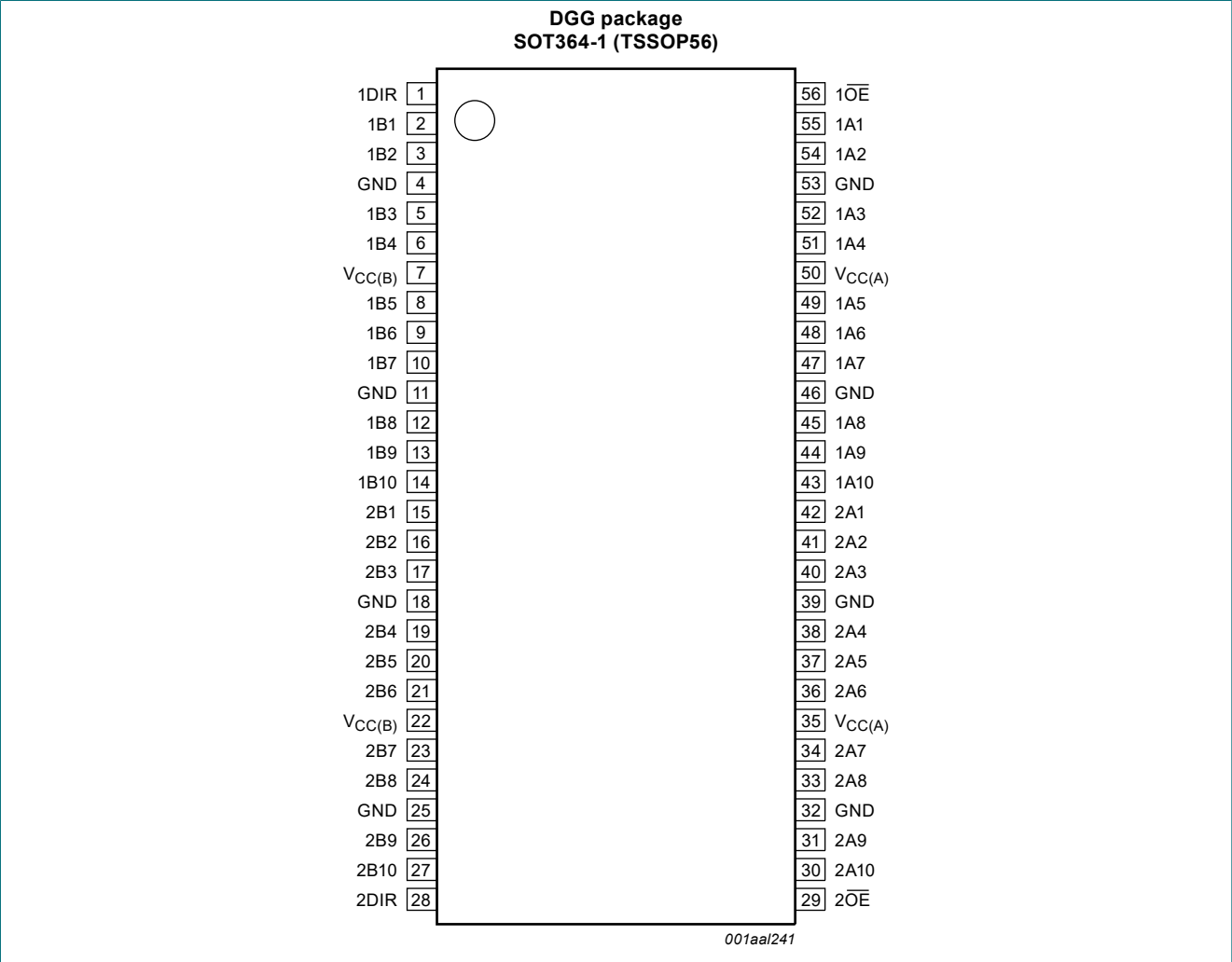


Fig. 2. Logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 28	direction control
1B1 to 1B10	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data input or output
2B1 to 2B10	15, 16, 17, 19, 20, 21, 23, 24,26, 27	data input or output
GND[1]	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V _{CC(B)}	7, 22	supply voltage B (nBn inputs are referenced to V _{CC(B)})
1OE, 2OE	56, 29	output enable input (active LOW)
1A1 to 1A10	55, 54, 52, 51, 49, 48, 47, 45,44, 43	data input or output
2A1 to 2A10	42, 41, 40, 38, 37, 36, 34, 33,31, 30	data input or output
V _{CC(A)}	35, 50	supply voltage A (nAn, nOE and nDIR inputs are referenced to V _{CC(A)})

[1] All GND pins must be connected to ground (0 V).

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage	Input		Input/output[1]	
V _{CC(A)} , V _{CC(B)}	nOE [2]	nDIR[2]	nAn[2]	nBn[2]
0.8 V to 3.6 V	L	L	nAn = nBn	input
0.8 V to 3.6 V	L	H	input	nBn = nAn
0.8 V to 3.6 V	H	X	Z	Z
GND[1]	X	X	Z	Z

[1] If at least one of V_{CC(A)} or V_{CC(B)} is at GND level, the device goes into suspend mode.
[2] The nAn, nDIR and nOE input circuit is referenced to V_{CC(A)}; The nBn input circuit is referenced to V_{CC(B)}.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(A)}	supply voltage A		-0.5	+4.6	V
V _{CC(B)}	supply voltage B		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
V _O	output voltage	Active mode [1] [2] [3]	-0.5	V _{CCO} + 0.5	V
		Suspend or 3-state mode [1]	-0.5	+4.6	V
I _O	output current	V _O = 0 V to V _{CCO} [2]	-	±50	mA
I _{CC}	supply current	I _{CC(A)} or I _{CC(B)}	-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [4]	-	500	mW

- [1] The minimum input and minimum output voltage ratings may be exceeded if the input and output clamping current ratings are observed.
- [2] V_{CCO} is the supply voltage associated with the output port.
- [3] V_{CCO} + 0.5 V should not exceed 4.6 V.
- [4] For SOT364-1 (TSSOP56) packages: P_{tot} derates linearly with 12.2 mW/K above 109 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(A)}	supply voltage A		0.8	3.6	V
V _{CC(B)}	supply voltage B		0.8	3.6	V
V _I	input voltage		0	3.6	V
V _O	output voltage	Active mode [1]	0	V _{CCO}	V
		Suspend or 3-state mode	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CCI} = 0.8 V to 3.6 V [2]	-	5	ns/V

- [1] V_{CCO} is the supply voltage associated with the output port.
- [2] V_{CCI} is the supply voltage associated with the input port.

9. Static characteristics

Table 6. Typical static characteristics at T_{amb} = 25 °C

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).[1] [2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -1.5 mA; V _{CC(A)} = V _{CC(B)} = 0.8 V	-	0.69	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 1.5 mA; V _{CC(A)} = V _{CC(B)} = 0.8 V	-	0.07	-	V
I _I	input leakage current	nDIR, nOE input; V _I = 0 V or 3.6 V; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	±0.025	±0.25	µA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = V _{CC(B)} = 3.6 V [3]	-	±0.5	±2.5	µA
		suspend mode A port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V [3]	-	±0.5	±2.5	µA
		suspend mode B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V [3]	-	±0.5	±2.5	µA
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 3.6 V; V _{CC(A)} = 0 V; V _{CC(B)} = 0.8 V to 3.6 V	-	±0.1	±1	µA
		B port; V _I or V _O = 0 V to 3.6 V; V _{CC(B)} = 0 V; V _{CC(A)} = 0.8 V to 3.6 V	-	±0.1	±1	µA
C _I	input capacitance	nDIR, nOE input; V _I = 0 V or 3.3 V; V _{CC(A)} = V _{CC(B)} = 3.3 V	-	2.0	-	pF
C _{I/O}	input/output capacitance	A and B port; V _O = 3.3 V or 0 V; V _{CC(A)} = V _{CC(B)} = 3.3 V	-	4.0	-	pF

- [1] V_{CCO} is the supply voltage associated with the output port.
- [2] V_{CCI} is the supply voltage associated with the data input port.
- [3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).[1] [2]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	data input					
		V _{CCI} = 0.8 V	0.70V _{CCI}	-	0.70V _{CCI}	-	V
		V _{CCI} = 1.1 V to 1.95 V	0.65V _{CCI}	-	0.65V _{CCI}	-	V
		V _{CCI} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V _{CCI} = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, nOE input					
		V _{CC(A)} = 0.8 V	0.70V _{CC(A)}	-	0.70V _{CC(A)}	-	V
		V _{CC(A)} = 1.1 V to 1.95 V	0.65V _{CC(A)}	-	0.65V _{CC(A)}	-	V
		V _{CC(A)} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V _{CC(A)} = 3.0 V to 3.6 V	2	-	2	-	V

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Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{IL}	LOW-level input voltage	data input					
		V _{CCI} = 0.8 V	-	0.30V _{CCI}	-	0.30V _{CCI}	V
		V _{CCI} = 1.1 V to 1.95 V	-	0.35V _{CCI}	-	0.35V _{CCI}	V
		V _{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, n $\overline{\text{OE}}$ input					
		V _{CC(A)} = 0.8 V	-	0.30V _{CC(A)}	-	0.30V _{CC(A)}	V
		V _{CC(A)} = 1.1 V to 1.95 V	-	0.35V _{CC(A)}	-	0.35V _{CC(A)}	V
		V _{CC(A)} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V _{CC(A)} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = -100 μ A; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	V _{CCO} - 0.1	-	V _{CCO} - 0.1	-	V
		I _O = -3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	0.85	-	0.85	-	V
		I _O = -6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	1.05	-	1.05	-	V
		I _O = -8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	1.2	-	1.2	-	V
		I _O = -9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	1.75	-	1.75	-	V
		I _O = -12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	2.3	-	2.3	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 100 μ A; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I _O = 3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	-	0.25	-	0.25	V
		I _O = 6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	-	0.35	-	0.35	V
		I _O = 8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	-	0.45	-	0.45	V
		I _O = 9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	-	0.55	-	0.55	V
		I _O = 12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	-	0.7	-	0.7	V
I _I	input leakage current	nDIR, n $\overline{\text{OE}}$ input; V _I = 0 V or 3.6 V; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	± 1	-	± 5	μ A
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = V _{CC(B)} = 3.6 V [3]	-	± 5	-	± 30	μ A
		suspend mode A port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V [3]	-	± 5	-	± 30	μ A
		suspend mode B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V [3]	-	± 5	-	± 30	μ A
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 3.6 V; V _{CC(A)} = 0 V; V _{CC(B)} = 0.8 V to 3.6 V	-	± 5	-	± 30	μ A
		B port; V _I or V _O = 0 V to 3.6 V; V _{CC(B)} = 0 V; V _{CC(A)} = 0.8 V to 3.6 V	-	± 5	-	± 30	μ A

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Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I _{CC}	supply current	A port; V _I = 0 V or V _{CCI} ; I _O = 0 A					
		V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	45	-	190	µA
		V _{CC(A)} = 1.1 V to 3.6 V; V _{CC(B)} = 1.1 V to 3.6 V	-	35	-	140	µA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-	35	-	140	µA
		V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V	-5	-	-20	-	µA
		B port; V _I = 0 V or V _{CCI} ; I _O = 0 A					
		V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	45	-	190	µA
		V _{CC(A)} = 1.1 V to 3.6 V; V _{CC(B)} = 1.1 V to 3.6 V	-	35	-	140	µA
		V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	-5	-	-20	-	µA
		V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V	-	35	-	140	µA
		A plus B port (I _{CC(A)} + I _{CC(B)}); I _O = 0 A; V _I = 0 V or V _{CCI} ; V _{CC(A)} = 0.8 V to 3.6 V; V _{CC(B)} = 0.8 V to 3.6 V	-	80	-	270	µA
		A plus B port (I _{CC(A)} + I _{CC(B)}); I _O = 0 A; V _I = 0 V or V _{CCI} ; V _{CC(A)} = 1.1 V to 3.6 V; V _{CC(B)} = 1.1 V to 3.6 V	-	65	-	220	µA

- [1] V_{CCO} is the supply voltage associated with the output port.
- [2] V_{CCI} is the supply voltage associated with the data input port.
- [3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 8. Typical total supply current (I_{CC(A)} + I_{CC(B)})

V _{CC(A)}	V _{CC(B)}							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	µA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	µA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	µA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	µA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	µA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	µA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	µA

10. Dynamic characteristics

Table 9. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$

Voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C_{PD}	power dissipation capacitance	A port: (direction A to B); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction A to B); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction B to A); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction B to A); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction A to B); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction A to B); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction B to A); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction B to A); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] $f_i = 10\text{ MHz}$; $V_i = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\text{ }\Omega$.

Table 10. Typical dynamic characteristics at $V_{CC(A)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		nBn to nAn	14.4	12.4	12.1	11.9	11.8	11.8	ns
t_{dis}	disable time	n $\overline{OE}$ to nAn	16.2	16.2	16.2	16.2	16.2	16.2	ns
		n $\overline{OE}$ to nBn	17.6	10.0	9.0	9.1	8.7	9.3	ns
t_{en}	enable time	n $\overline{OE}$ to nAn	21.9	21.9	21.9	21.9	21.9	21.9	ns
		n $\overline{OE}$ to nBn	22.2	11.1	9.8	9.4	9.4	9.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Table 11. Typical dynamic characteristics at $V_{CC(B)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4 [1]

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		nBn to nAn	14.4	7.0	6.2	6.0	5.9	6.0	ns
t_{dis}	disable time	n $\overline{OE}$ to nAn	16.2	5.9	4.4	4.2	3.1	3.5	ns
		n $\overline{OE}$ to nBn	17.6	14.2	13.7	13.6	13.3	13.1	ns
t_{en}	enable time	n $\overline{OE}$ to nAn	21.9	6.4	4.4	3.5	2.6	2.3	ns
		n $\overline{OE}$ to nBn	22.2	17.7	17.2	17.0	16.8	16.7	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

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Table 12. Dynamic characteristics for temperature range -40 °C to +85 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4.[1]

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.4	0.5	7.1	0.5	6.2	0.5	5.2	0.5	5.1	ns
		nBn to nAn	0.5	9.4	0.5	8.9	0.5	8.7	0.5	8.4	0.5	8.2	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	2.0	11.9	2.0	11.9	2.0	11.9	2.0	11.9	2.0	11.9	ns
		n $\overline{OE}$ to nBn	1.5	12.7	1.5	9.8	1.5	9.6	1.0	8.1	1.0	9.0	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	1.5	15.3	1.5	15.3	1.5	15.3	1.5	15.3	1.5	15.3	ns
		n $\overline{OE}$ to nBn	1.0	15.6	1.0	11.5	1.0	10.0	0.5	8.4	0.5	8.0	ns
V _{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.9	0.5	6.4	0.5	5.4	0.5	4.3	0.5	3.9	ns
		nBn to nAn	0.5	7.1	0.5	6.4	0.5	6.1	0.5	5.8	0.5	5.7	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	2.0	9.0	2.0	9.0	2.0	9.0	2.0	9.0	2.0	9.0	ns
		n $\overline{OE}$ to nBn	1.5	11.7	1.5	9.0	1.5	7.8	1.0	6.4	1.0	6.0	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	1.5	10.3	1.5	10.3	1.5	10.3	1.5	10.2	1.5	10.2	ns
		n $\overline{OE}$ to nBn	1.0	14.3	1.0	10.3	1.0	8.4	0.5	6.1	0.5	5.3	ns
V _{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.7	0.5	6.1	0.5	5.0	0.5	3.9	0.5	3.5	ns
		nBn to nAn	0.5	6.2	0.5	5.4	0.5	5.0	0.5	4.7	0.5	4.6	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	2.0	7.4	2.0	7.4	2.0	7.4	2.0	7.4	2.0	7.4	ns
		n $\overline{OE}$ to nBn	1.5	11.3	1.5	8.7	1.5	7.4	1.0	5.8	1.0	5.6	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	1.0	8.1	1.0	8.1	1.0	7.9	1.0	7.9	1.0	7.9	ns
		n $\overline{OE}$ to nBn	0.5	13.8	0.5	10.0	0.5	7.9	0.5	5.7	0.5	4.8	ns
V _{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.4	0.5	5.8	0.5	4.7	0.5	3.5	0.5	3.0	ns
		nBn to nAn	0.5	5.2	0.5	4.3	0.5	3.9	0.5	3.5	0.5	3.4	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	ns
		n $\overline{OE}$ to nBn	1.2	10.8	1.2	8.2	1.2	6.9	1.0	5.3	1.0	5.2	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	0.5	5.4	0.5	5.4	0.5	5.3	0.5	5.2	0.5	5.2	ns
		n $\overline{OE}$ to nBn	0.5	13.3	0.5	9.6	0.5	7.6	0.5	5.3	0.5	4.3	ns
V _{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	8.2	0.5	5.7	0.5	4.6	0.5	3.4	0.5	2.9	ns
		nBn to nAn	0.5	5.1	0.5	3.9	0.5	3.5	0.5	3.0	0.5	2.9	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	0.8	5.0	0.8	5.0	0.8	5.0	0.8	5.0	0.8	5.0	ns
		n $\overline{OE}$ to nBn	1.2	10.5	1.2	8.1	1.2	6.7	1.0	5.1	0.8	5.0	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	0.5	4.4	0.5	4.4	0.5	4.3	0.5	4.2	0.5	4.1	ns
		n $\overline{OE}$ to nBn	1.0	13.1	1.0	9.6	0.5	7.5	0.5	5.1	0.5	4.1	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

20-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 13. Dynamic characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4 [1]

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	nAn to nBn	0.5	10.4	0.5	7.9	0.5	6.9	0.5	5.8	0.5	5.7	ns
		nBn to nAn	0.5	10.4	0.5	9.8	0.5	9.6	0.5	9.3	0.5	9.1	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	2.0	13.1	2.0	13.1	2.0	13.1	2.0	13.1	2.0	13.1	ns
		n $\overline{OE}$ to nBn	1.5	14.0	1.5	10.8	1.5	10.6	1.0	9.0	1.0	9.9	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	1.5	16.9	1.5	16.9	1.5	16.9	1.5	16.9	1.5	16.9	ns
		n $\overline{OE}$ to nBn	1.0	17.2	1.0	12.7	1.0	11.0	0.5	9.3	0.5	8.8	ns
V _{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.8	0.5	7.1	0.5	6.0	0.5	4.8	0.5	4.3	ns
		nBn to nAn	0.5	7.9	0.5	7.1	0.5	6.8	0.5	6.4	0.5	6.3	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	2.0	9.9	2.0	9.9	2.0	9.9	2.0	9.9	2.0	9.9	ns
		n $\overline{OE}$ to nBn	1.5	12.9	1.5	9.9	1.5	8.6	1.0	7.1	1.0	6.6	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	1.5	11.4	1.5	11.4	1.5	11.4	1.5	11.3	1.5	11.3	ns
		n $\overline{OE}$ to nBn	1.0	15.8	1.0	11.4	1.0	9.3	0.5	6.8	0.5	5.9	ns
V _{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.6	0.5	6.8	0.5	5.5	0.5	4.3	0.5	3.9	ns
		nBn to nAn	0.5	6.9	0.5	6.0	0.5	5.5	0.5	5.2	0.5	5.1	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	2.0	8.2	2.0	8.2	2.0	8.2	2.0	8.2	2.0	8.2	ns
		n $\overline{OE}$ to nBn	1.5	12.5	1.5	9.6	1.5	8.2	1.0	6.4	1.0	6.2	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	1.0	9.0	1.0	9.0	1.0	8.7	1.0	8.7	1.0	8.7	ns
		n $\overline{OE}$ to nBn	0.5	15.2	0.5	11.0	0.5	8.7	0.5	6.3	0.5	5.3	ns
V _{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.3	0.5	6.4	0.5	5.2	0.5	3.9	0.5	3.3	ns
		nBn to nAn	0.5	5.8	0.5	4.8	0.5	4.3	0.5	3.9	0.5	3.8	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	1.1	5.8	1.1	5.8	1.1	5.8	1.1	5.8	1.1	5.8	ns
		n $\overline{OE}$ to nBn	1.2	11.9	1.2	9.1	1.2	7.6	1.0	5.9	1.0	5.8	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	0.5	6.0	0.5	6.0	0.5	5.9	0.5	5.8	0.5	5.8	ns
		n $\overline{OE}$ to nBn	0.5	14.7	0.5	10.6	0.5	8.4	0.5	5.9	0.5	4.8	ns
V _{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	nAn to nBn	0.5	9.1	0.5	6.3	0.5	5.1	0.5	3.8	0.5	3.2	ns
		nBn to nAn	0.5	5.7	0.5	4.3	0.5	3.9	0.5	3.3	0.5	3.2	ns
t _{dis}	disable time	n $\overline{OE}$ to nAn	0.8	5.5	0.8	5.5	0.8	5.5	0.8	5.5	0.8	5.5	ns
		n $\overline{OE}$ to nBn	1.2	11.6	1.2	9.0	1.2	7.4	1.0	5.7	0.8	5.5	ns
t _{en}	enable time	n $\overline{OE}$ to nAn	0.5	4.9	0.5	4.9	0.5	4.8	0.5	4.7	0.5	4.6	ns
		n $\overline{OE}$ to nBn	1.0	14.5	1.0	10.6	0.5	8.3	0.5	5.7	0.5	4.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

10.1. Waveforms and test circuit

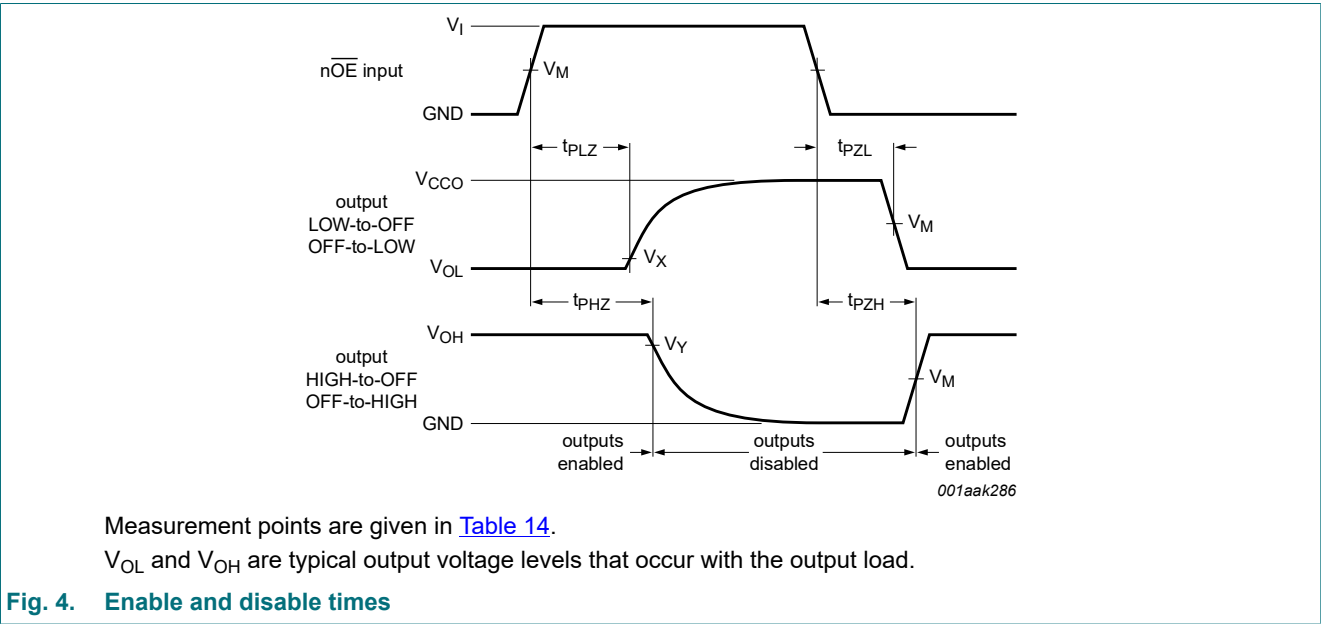
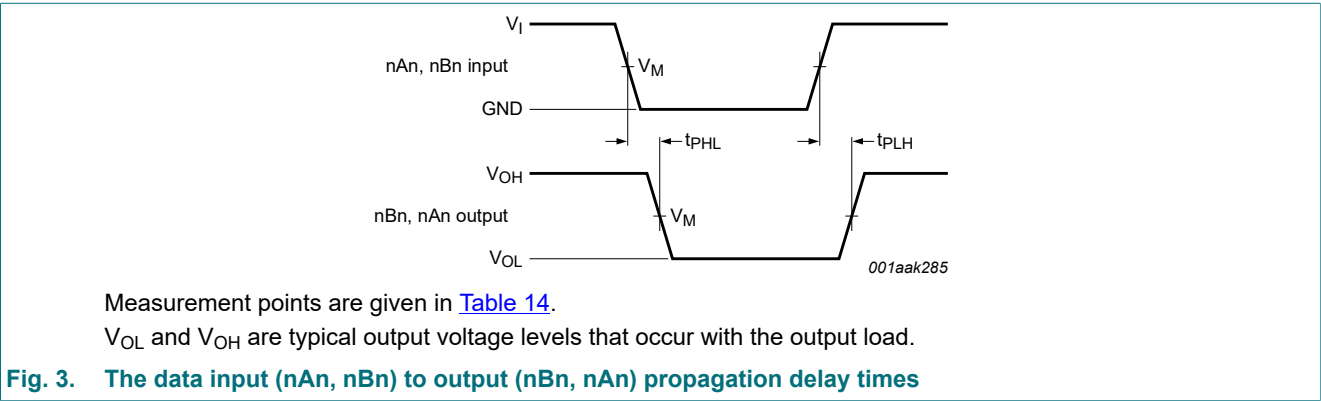
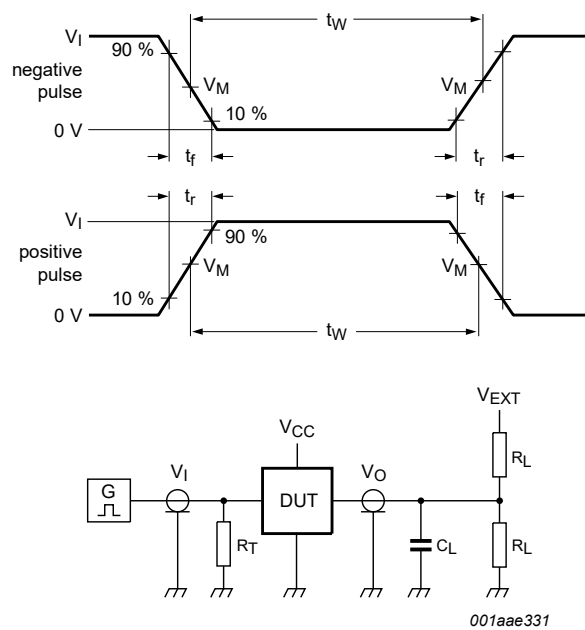


Table 14. Measurement points

Supply voltage	Input [1]	Output [2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1\text{ V}$	$V_{OH} - 0.1\text{ V}$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1] V_{CCI} is the supply voltage associated with the data input port.
[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in [Table 15](#).
Definitions test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance.
 V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

Table 15. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	V_I [1]	$\Delta t/\Delta V$ [2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
0.8 V to 1.6 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the data input port.
[2] $dV/dt \geq 1.0 \text{ V/ns}$
[3] V_{CCO} is the supply voltage associated with the output port.

11. Typical propagation delay characteristics

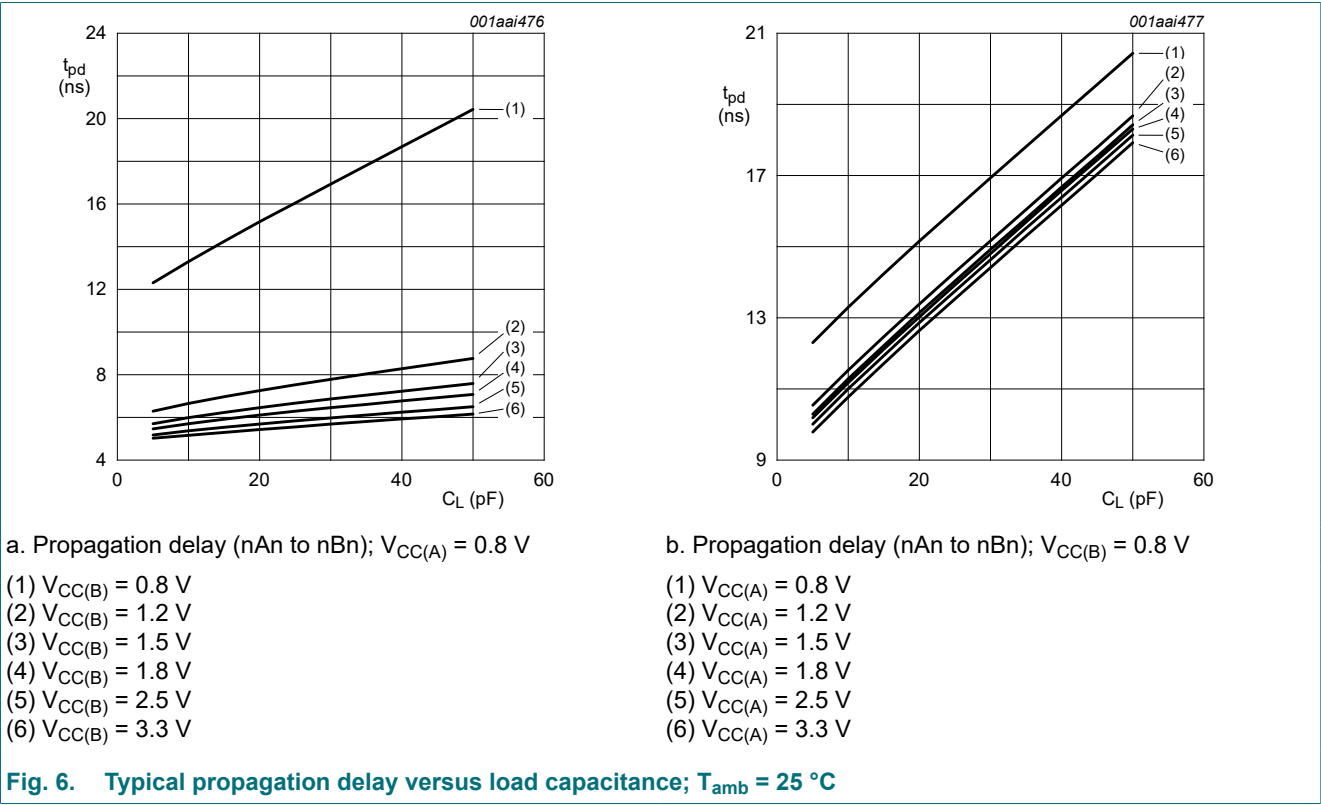
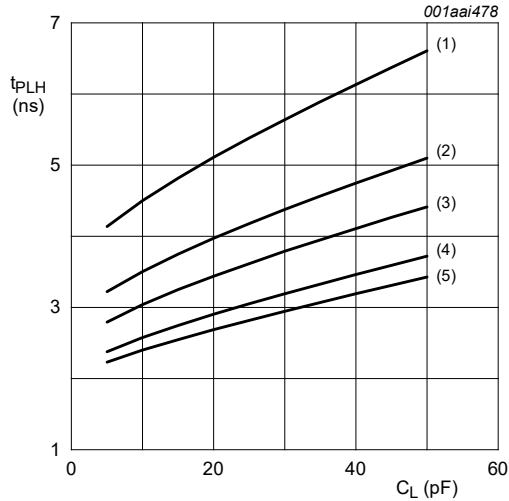
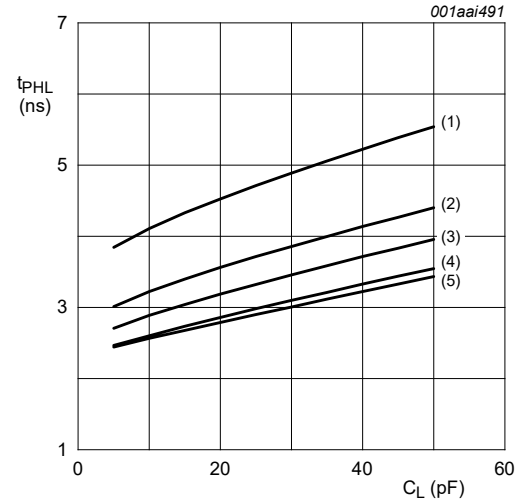


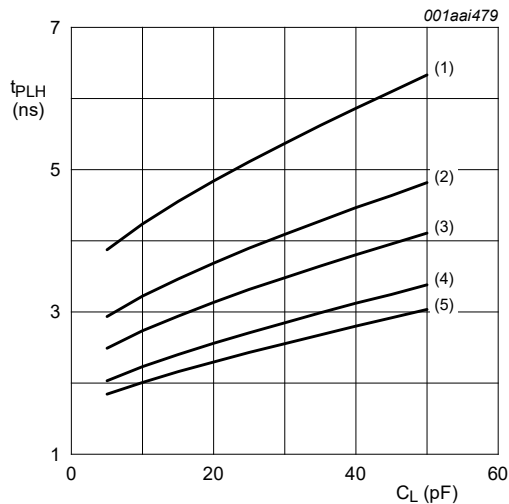
Fig. 6. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^{\circ}\text{C}$



a. LOW to HIGH propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.2 \text{ V}$

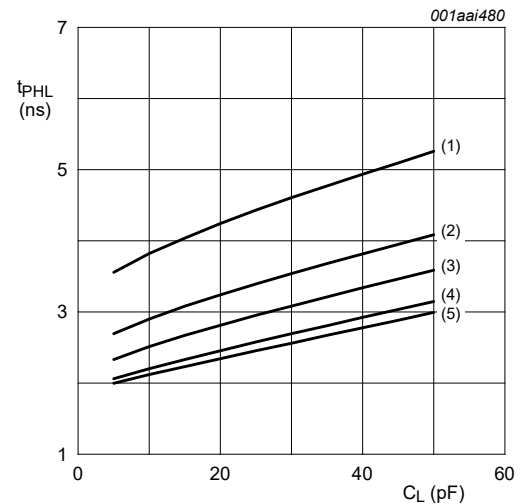


b. HIGH to LOW propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.2 \text{ V}$



c. LOW to HIGH propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.5 \text{ V}$

- (1) $V_{CC(B)} = 1.2 \text{ V}$
- (2) $V_{CC(B)} = 1.5 \text{ V}$
- (3) $V_{CC(B)} = 1.8 \text{ V}$
- (4) $V_{CC(B)} = 2.5 \text{ V}$
- (5) $V_{CC(B)} = 3.3 \text{ V}$



d. HIGH to LOW propagation delay (nAn to nBn);
 $V_{CC(A)} = 1.5 \text{ V}$

Fig. 7. Typical propagation delay versus load capacitance; $T_{amb} = 25 \text{ }^{\circ}\text{C}$

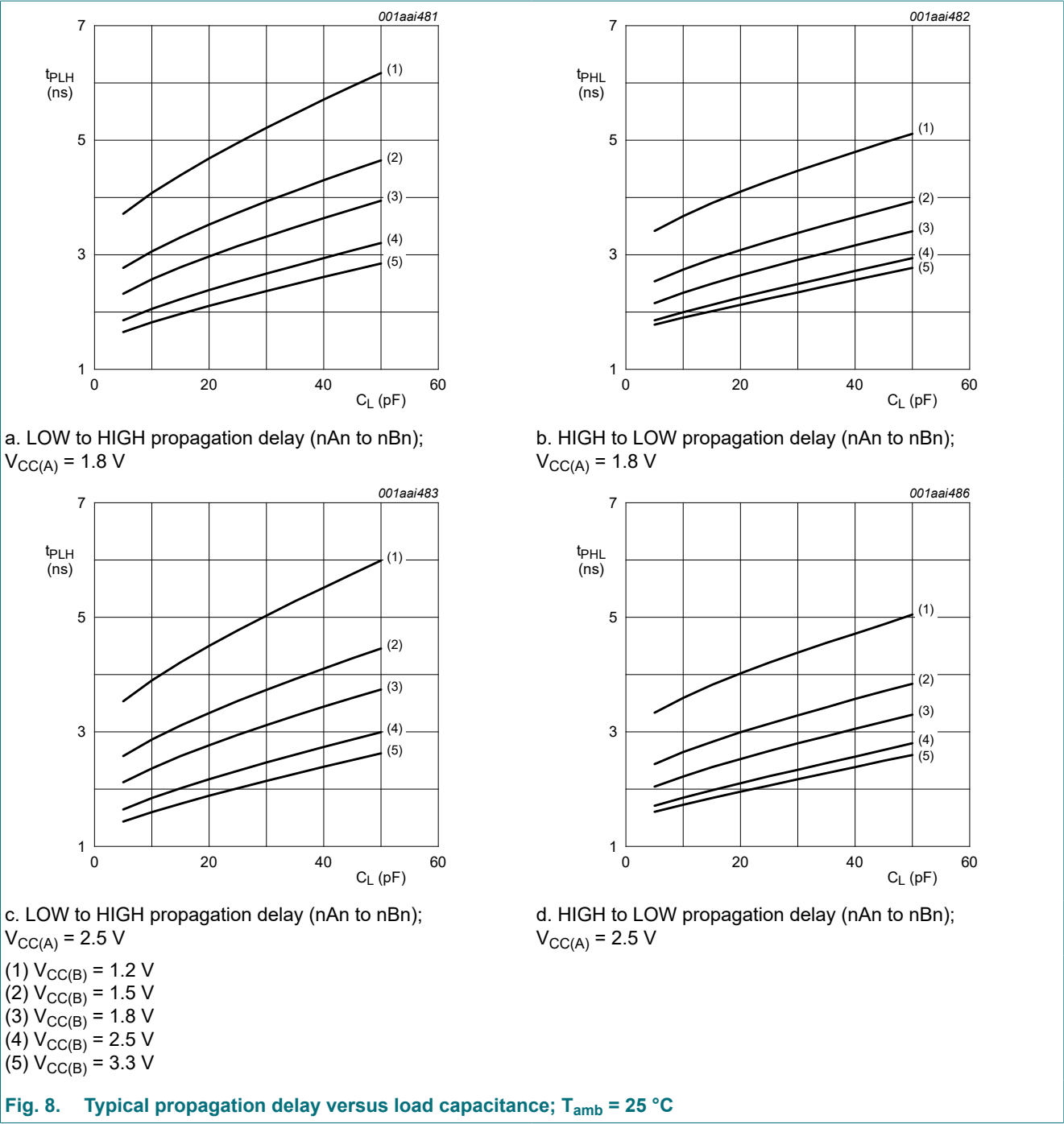
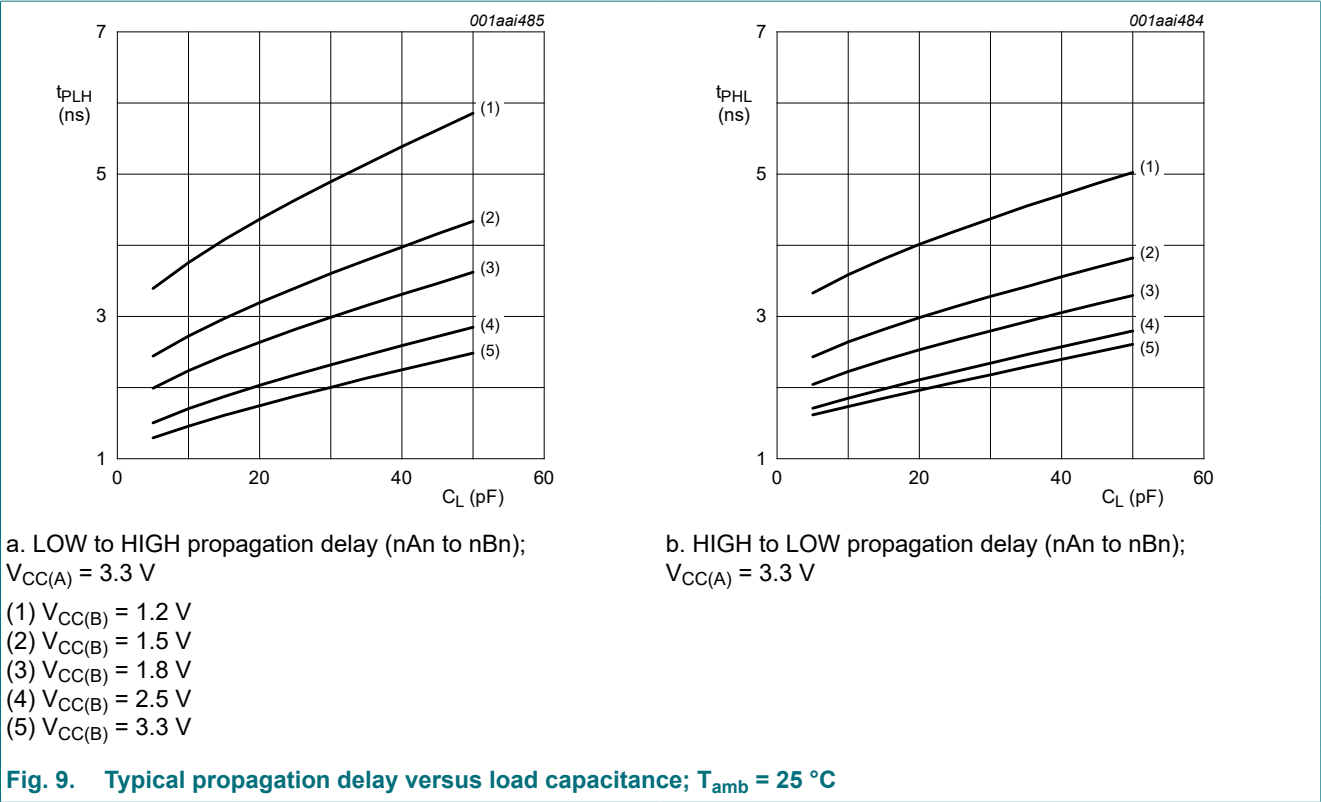


Fig. 8. Typical propagation delay versus load capacitance; $T_{amb} = 25\text{ }^{\circ}\text{C}$



12. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

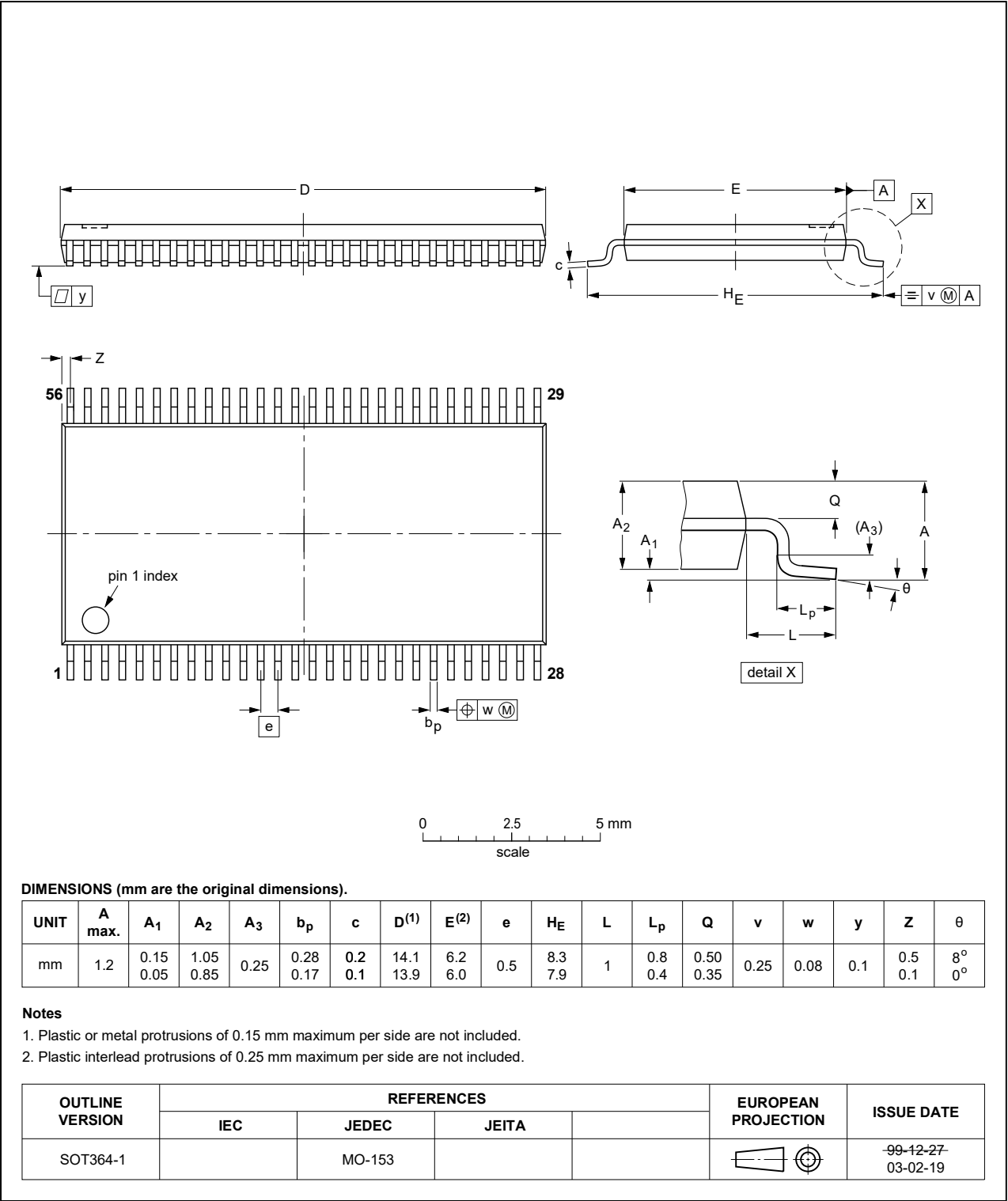


Fig. 10. Package outline SOT364-1 (TSSOP56)

13. Abbreviations

Table 16. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC20T245 v.9	20240625	Product data sheet	-	74AVC20T245 v.8
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - Section 7: P_{tot} and derating values for P_{tot} total power dissipation updated.			
74AVC20T245 v.8	20190114	Product data sheet	-	74AVC20T245 v.7
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type numbers 74AVC20T245DGV and 74AVC20T245BX removed.			
74AVC20T245 v.7	20120308	Product data sheet	-	74AVC20T245 v.6
Modifications:	For type number 74AVC20T245BX the sot code has changed to SOT1134-2.			
74AVC20T245 v.6	20111207	Product data sheet	-	74AVC20T245 v.5
Modifications:	Legal pages updated.			
74AVC20T245 v.5	20110616	Product data sheet	-	74AVC20T245 v.4
74AVC20T245 v.4	20101124	Product data sheet	-	74AVC20T245 v.3
74AVC20T245 v.3	20100622	Product data sheet	-	74AVC20T245 v.2
74AVC20T245 v.2	20100318	Product data sheet	-	74AVC20T245 v.1
74AVC20T245 v.1	20100111	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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