Configurable, Dual 3 A/Single 6 A, Synchronous, Step-Down DC-to-DC Regulator

Data Sheet

ADP2116

FEATURES

- Configurable 3 A/3 A or 3 A/2 A dual-output load combinations or 6 A combined single-output load
- High efficiency: up to 95%
- Input voltage, V_{IN}: 2.75 V to 5.5 V
- Selectable fixed output voltage of 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, or adjustable output voltage to 0.6 V minimum
- ±1.5% accurate reference voltage
- Selectable switching frequency of 300 kHz, 600 kHz, 1.2 MHz, or synchronized from 200 kHz to 2 MHz
- Optimized gate slew rate for reduced EMI
- External synchronization input or internal clock output
- Dual-phase, 180° phase-shifted PWM channels
- Current mode for fast transient response
- Pulse skip mode with light loads or forced PWM operation
- Input undervoltage lockout (UVLO)
- Independent enable inputs and power-good outputs
- Overcurrent and thermal overload protection
- Programmable soft start
- 32-lead, 5 mm × 5 mm LFCSP package
- Supported by ADIsimPower™ design tool

APPLICATIONS

- Point-of-load regulation
- Telecommunications and networking systems
- Consumer electronics
- Industrial and instrumentation
- Medical

GENERAL DESCRIPTION

The ADP2116 is a versatile, synchronous, step-down switching regulator that satisfies a wide range of customer point-of-load requirements. The two PWM channels can be configured to deliver independent outputs at 3 A and 3 A (or at 3 A and 2 A) or can be configured as a single interleaved output capable of delivering 6 A. The two PWM channels are 180° phase shifted to reduce input ripple current and input capacitance.

The ADP2116 provides high efficiency and can operate at switching frequencies of up to 2 MHz. At light loads, the ADP2116 can be set to operate in pulse skip mode for higher efficiency or in forced PWM mode for noise sensitive applications.

The ADP2116 is designed with an optimized slew rate to reduce EMI emissions, allowing the device to power sensitive, high performance signal chain circuits. The switching frequency can be set to 300 kHz, 600 kHz, or 1.2 MHz, or it can be synchronized to an external clock that minimizes the system noise. The bidirectional synchronization pin is also configurable as a 90° out-of-phase output clock, providing the possibility for a stackable multiphase power solution.

The ADP2116 input voltage range is from 2.75 V to 5.5 V and can convert to a fixed output of 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V that can be set independently for each channel using external resistors. If a resistor divider is used, the output voltage can be set as low as 0.6 V. The ADP2116 operates over the −40°C to +125°C junction temperature range.

TYPICAL APPLICATION CIRCUIT

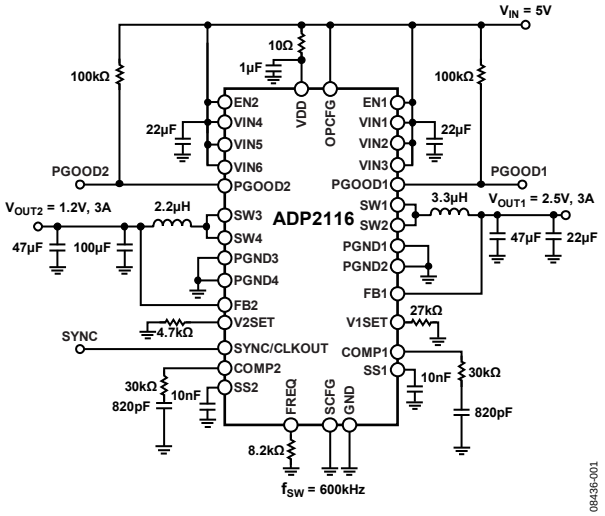

Figure 1.

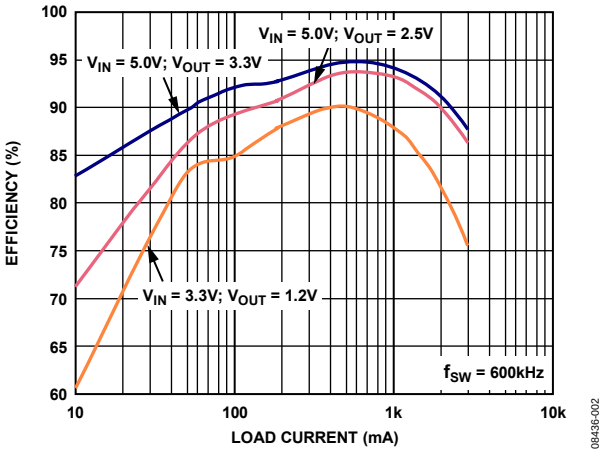

Figure 2. Typical Efficiency vs. Load Current

Rev. B

Document Feedback

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Changed CP-32-2 to CP-32-7 ... Throughout
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6/12—Rev. 0 to Rev. A

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Updated Outline Dimensions ... 36

10/09—Revision 0: Initial Version

SPECIFICATIONS

If unspecified, VDD = VINx = EN1 = EN2 = 5.0 V. The minimum and maximum specifications are valid for T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_J = 25°C. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
VDD Bias Voltage	V_{DD}		2.75		5.5	V
Undervoltage Lockout Threshold	UVLO	V_{DD} rising		2.65	2.75	V
		V_{DD} falling	2.35	2.47		
Undervoltage Lockout Hysteresis				0.18		V
Quiescent Current	$I_{DD,CH1}$	EN1 = VDD = 5 V, EN2 = GND, V_{FB1} = VDD, OPCFG = GND		1.7	2.5	mA
	$I_{DD,CH2}$	EN2 = VDD = 5 V, EN1 = GND, V_{FB2} = VDD, OPCFG = GND		1.7	2.5	mA
	$I_{DD,CH1 + CH2}$	EN1 = EN2 = VDD = 5 V, V_{FB2} = V_{FB1} = VDD, OPCFG = GND		3.0	4.0	mA
Shutdown Current	$I_{DD,SD}$	EN1 = EN2 = GND, VDD = VINx = 2.75 V to 5.5 V, T_J = −40°C to +115°C		1.0	10	µA
ERROR INTEGRATOR (OPERATIONAL TRANSCONDUCTANCE AMPLIFIER)						
FB1, FB2 Input Bias Current	I_{FB}	Adjustable output, V_{FBx} = 0.6 V, V1SET, V2SET = VDD or via 82 kΩ to GND		1	65	nA
		Fixed output, V_{FBx} = 1.2 V, V1SET, V2SET via 4.7 kΩ to GND		11	15	µA
Transconductance	g_m			550		µA/V
COMPx VOLTAGE RANGE						
COMPx Zero-Current Threshold	$V_{COMP, ZCT}$	Guaranteed by design		1.12		V
COMPx Clamp High Voltage	$V_{COMP, HI}$	VDD = VINx = 2.75 V to 5.5 V		2.36	2.45	V
COMPx Clamp Low Voltage	$V_{COMP, LO}$	VDD = VINx = 2.75 V to 5.5 V	0.65	0.70		V
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	V_{FB}	Adjustable output, T_J = 25°C, V1SET, V2SET = VDD or via 82 kΩ to GND	0.597	0.600	0.603	V
		Adjustable output, T_J = −40°C to +125°C, V1SET, V2SET = VDD or via 82 kΩ to GND	0.594	0.600	0.606	V
	$V_{FB\ ERROR}$	Fixed output, T_J = 25°C, V1SET, V2SET = GND or via 4.7 kΩ, 8.2 kΩ, 15 kΩ, 27 kΩ, 47 kΩ to GND	−1.0		+1.0	%
		Fixed output, T_J = −40°C to +125°C, V1SET, V2SET = GND or via 4.7 kΩ, 8.2 kΩ, 15 kΩ, 27 kΩ, 47 kΩ to GND	−1.5		+1.5	%
Line Regulation		VDD = VINx = 2.75 V to 5.5 V		0.05		%/V
Load Regulation		VDD = VINx = 2.75 V to 5.5 V		0.03		%/A
OSCILLATOR		All oscillator parameters provided for VDD = 2.75 V to 5.5 V				
Switching Frequency	f_{SW}	FREQ tied to GND	255	300	345	kHz
		FREQ via 8.2 kΩ to GND	510	600	690	kHz
		FREQ via 27 kΩ to GND	1020	1200	1380	kHz
SYNC Frequency Range	f_{SYNC}	$f_{SYNC} = 2 \times f_{SW}$				
		FREQ tied to GND	400		1000	kHz
		FREQ via 8.2 kΩ to GND	800		2000	kHz
		FREQ via 27 kΩ to GND	1600		4000	kHz
SYNC Input Pulse Width			100			ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SYNC Pin Capacitance to GND	C_{SYNC}			5		pF
SYNC Input Logic Low	V_{IL_SYNC}				0.8	V
SYNC Input Logic High	V_{IH_SYNC}		2.0			V
Phase Shift Between Channels				180		Degrees
CLKOUT Frequency	f_{CLKOUT}	$f_{CLKOUT} = 2 \times f_{SW}$				
		FREQ tied to GND	510	600	690	kHz
		FREQ via 8.2 kΩ to GND	1020	1200	1380	kHz
		FREQ via 27 kΩ to GND	2040	2400	2760	kHz
CLKOUT Positive Pulse Time	t_{CLKOUT}		100			ns
CLKOUT Rise or Fall Time		C_{CLKOUT} = 20 pF		10		ns
CURRENT LIMIT		All current-limit parameters provided for VDD = VINx = 2.75 V to 5.5 V				
Peak Output Current Limit, Channel 1	I_{LIMIT1}	OPCFG tied to VDD or via 82 kΩ to GND	3.5	4.5	5.3	A
Peak Output Current Limit, Channel 2	I_{LIMIT2}	OPCFG tied to VDD or via 82 kΩ to GND	3.5	4.5	5.3	A
		OPCFG via 47 kΩ or 27 kΩ to GND	2.4	3.3	4.0	A
Current-Sense Amplifier Gain	G_{CS}			4		A/V
Hiccup Time		f_{SW} = 300 kHz	10	13.6	17	ms
Number of Cumulative Current-Limit Cycles to Go into Hiccup Mode				8		Cycles
SWITCH NODE CHARACTERISTICS						
High-Side, P-Channel R_{DSON}[1]		VDD = VINx = 3.3 V		68		mΩ
		VDD = VINx = 5.0 V		52		mΩ
Low-Side, N-Channel R_{DSON}[1]		VDD = VINx = 3.3 V		32		mΩ
		VDD = VINx = 5.0 V		27		mΩ
SWx Minimum On Time	$SW_{ON\ MIN}$	VDD = VINx = 2.75 V to 5.5 V		107		ns
SWx Minimum Off Time	$SW_{OFF\ MIN}$	VDD = VINx = 5.5 V		192		ns
		VDD = VINx = 2.75 V		255		ns
SWx Maximum Leakage Current		VDD = VINx = 2.75 V to 5.5 V, ENx = GND, T_J = −40°C to +115°C		0.1	15	µA
ENABLE INPUTS						
EN1, EN2 Logic Low Level	EN_{LO}	VDD = VINx = 2.75 V to 5.5 V			0.8	V
EN1, EN2 Logic High Level	EN_{HI}	VDD = VINx = 2.75 V to 5.5 V	2.0			V
EN1, EN2 Input Leakage Current	I_{EN_LEAK}	VDD = VINx = ENx = 2.75 V to 5.5 V, T_J = −40°C to +115°C		0.1	1	µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{TMSD}			150		°C
Thermal Shutdown Hysteresis				25		°C
SOFT START						
SS1, SS2 Pin Current	I_{SS1}, I_{SS2}	VDD = VINx = 2.75 V to 5.5 V, V_{SS} = 0 V	4.8	6.0	7.8	µA
Soft Start Threshold Voltage	V_{SS_THRESH}	VDD = VINx = 2.75 V to 5.5 V		0.65		V
Soft Start Pull-Down Current		VDD = VINx = 2.75 V to 5.5 V, EN = GND	0.5			mA
POWER GOOD		All power-good parameters provided for VDD = VINx = 2.75 V to 5.5 V				
Overvoltage PGOODx Rising Threshold[2]				116		%
Overvoltage PGOODx Falling Threshold[2]			100	108	114	%
Undervoltage PGOODx Rising Threshold[2]			85	92	97	%
Undervoltage PGOODx Falling Threshold[2]				84		%
PGOODx Delay				50		µs
PGOODx Leakage Current		V_{PGOODx} = VDD		0.1	1	µA
PGOODx Low Saturation Voltage		I_{PGOODx} = 1 mA		50	110	mV

[1] Pin-to-pin measurements.
[2] The thresholds are expressed as a percentage of the nominal output voltage.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VDD to GND	−0.3 V to +6 V
VIN1, VIN2, VIN3, VIN4, VIN5, VIN6 to PGND1, PGND2, PGND3, PGND4	−0.3 V to +6 V
EN1, EN2, SCFG, FREQ, SYNC/CLKOUT, PGOOD1, PGOOD2, V1SET, V2SET, COMP1, COMP2, SS1, SS2 to GND	−0.3 V to (VDD + 0.3 V)
FB1, FB2 to GND	−0.3 V to +3.6 V
SW1, SW2, SW3, SW4 to PGND1, PGND2, PGND3, PGND4	−0.3 V to (VDD + 0.3 V)
PGND1, PGND2, PGND3, PGND4 to GND	±0.3 V
VIN1, VIN2, VIN3, VIN4, VIN5, VIN6 to VDD	±0.3 V
θ_{JA}, JEDEC 1S2P PCB, Natural Convection	34°C/W
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Soldering Lead Temperature (10 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Absolute maximum ratings apply individually only, not in combination.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

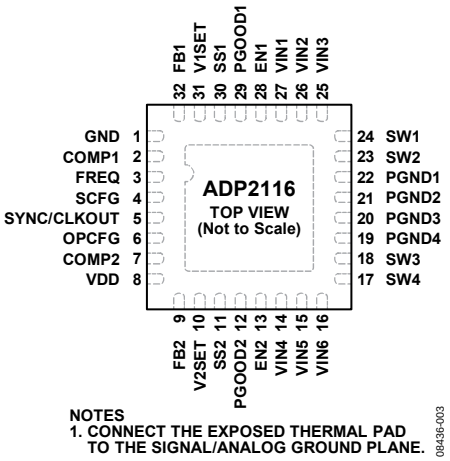


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground for the Internal Analog and Digital Circuits. Connect GND to the signal/analog ground plane before connecting to the power ground.
2	COMP1	Error Amplifier Output for Channel 1. Connect a series RC network from COMP1 to GND to compensate the control loop of Channel 1. For multiphase operation, tie COMP1 and COMP2 together.
3	FREQ	Frequency Select Input. Connect this pin through a resistor to GND to set the appropriate switching frequency (see Table 5).
4	SCFG	Synchronization Configuration Input. SCFG configures the SYNC/CLKOUT pin as an input or output. Tie this pin to VDD to configure SYNC/CLKOUT as an output. Tie this pin to GND to configure SYNC/CLKOUT as an input.
5	SYNC/CLKOUT	External Synchronization Input/Internal Clock Output. This bidirectional pin is configured with the SCFG pin (see the Pin 4 description for details). When this pin is configured as an output, a buffered clock of twice the switching frequency with a phase shift of 90° is available on this pin. When configured as an input, this pin accepts an external clock to which the converters are synchronized. The frequency select resistor, mentioned in the description of Pin 3, must be selected to be close to the expected switching frequency for stable operation (see the Setting the Oscillator Frequency section).
6	OPCFG	Operation Configuration Input. Connect this pin to VDD or through a resistor to GND to set the system mode of operation according to Table 7. This pin can be used to select a peak current limit for each power channel and to enable or disable the pulse skip mode.
7	COMP2	Error Amplifier Output for Channel 2. Connect a series RC network from COMP2 to GND to compensate the control loop of Channel 2. For multiphase operation, tie COMP1 and COMP2 together.
8	VDD	Power Supply Input. The power source for the ADP2116 internal circuitry. Connect VDD and VINx with a 10 Ω resistor as close as possible to the ADP2116. Bypass VDD to GND with a 1 µF or greater capacitor.
9	FB2	Feedback Voltage Input for Channel 2. For the fixed output voltage option, connect FB2 to V_{OUT2}. For the adjustable output voltage option, connect this pin to a resistor divider between V_{OUT2} and GND. The reference voltage for the adjustable output voltage option is 0.6 V. With multiphase configurations, the FB2 and FB1 pins should be tied together and then connected to V_{OUT}.
10	V2SET	Output Voltage Set Pin for Channel 2. To select a fixed output voltage option (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V) for V_{OUT2}, connect this pin through a resistor to GND (see Table 4 for details). To select an adjustable output voltage for V_{OUT2}, connect this pin to GND through an 82 kΩ resistor or tie this pin directly to VDD depending on the output voltage desired.
11	SS2	Soft Start Input for Channel 2. Place a capacitor from SS2 to GND to set the soft start period. A 10 nF capacitor sets a 1 ms soft start period. For multiphase configuration, connect SS2 to SS1.
12	PGOOD2	Open-Drain Power-Good Output for Channel 2. Place a 100 kΩ pull-up resistor to VDD or to any other voltage that is 5.5 V or less; PGOOD2 is held low when Channel 2 is out of regulation.
13	EN2	Enable Input for Channel 2. Drive EN2 high to turn on the Channel 2 converter; drive EN2 low to turn off the Channel 2 converter. Tie EN2 to VDD for startup with VDD. When using a multiphase configuration, connect EN2 to EN1.

Pin No.	Mnemonic	Description
14	VIN4	Power Supply Input. The source of the high-side internal power MOSFET of Channel 2.
15	VIN5	Power Supply Input. The source of the high-side internal power MOSFET of Channel 2.
16	VIN6	Power Supply Input. The source of the high-side internal power MOSFET of Channel 2.
17	SW4	Switch Node Output. The drain of the P-channel power switch and N-channel synchronous rectifier of Channel 2. Tie SW3 to SW4, and then connect the output LC filter between the switching node and the output voltage.
18	SW3	Switch Node Output. The drain of the P-channel power switch and N-channel synchronous rectifier of Channel 2. Tie SW3 to SW4, and then connect the output LC filter between the switching node and the output voltage.
19	PGND4	Power Ground. The source of the low-side internal power MOSFET of Channel 2.
20	PGND3	Power Ground. The source of the low-side internal power MOSFET of Channel 2.
21	PGND2	Power Ground. The source of the low-side internal power MOSFET of Channel 1.
22	PGND1	Power Ground. The source of the low-side internal power MOSFET of Channel 1.
23	SW2	Switch Node Output. The drain of the P-channel power switch and N-channel synchronous rectifier of Channel 1. Tie SW1 to SW2, and then connect the output LC filter between the switching node and the output voltage.
24	SW1	Switch Node Output. The drain of the P-channel power switch and N-channel synchronous rectifier of Channel 1. Tie SW1 to SW2, and then connect the output LC filter between the switching node and the output voltage.
25	VIN3	Power Supply Input. The source of the high-side internal power MOSFET of Channel 1.
26	VIN2	Power Supply Input. The source of the high-side internal power MOSFET of Channel 1.
27	VIN1	Power Supply Input. The source of the high-side internal power MOSFET of Channel 1.
28	EN1	Enable Input for Channel 1. Drive EN1 high to turn on the Channel 1 converter; drive EN1 low to turn off the Channel 1 converter. Tie EN1 to VDD for startup with VDD. When using a multiphase configuration, connect EN1 to EN2.
29	PGOOD1	Open-Drain Power-Good Output for Channel 1. Place a 100 kΩ pull-up resistor to VDD or to any other voltage that is 5.5 V or less; PGOOD1 is held low when Channel 1 is out of regulation.
30	SS1	Soft Start Input for Channel 1. Place a capacitor from SS1 to GND to set the soft start period. A 10 nF capacitor sets a 1 ms soft start period. For multiphase configuration, connect SS1 to SS2.
31	V1SET	Output Voltage Set Pin for Channel 1. To select a fixed output voltage option (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V) for V_{OUT1}, connect this pin through a resistor to GND (see Table 4 for details). To select an adjustable output voltage for V_{OUT1}, connect this pin to GND through an 82 kΩ resistor or tie this pin directly to VDD depending on the output voltage desired.
32	FB1	Feedback Voltage Input for Channel 1. For the fixed output voltage option, connect FB1 to V_{OUT1}. For the adjustable output voltage option, connect this pin to a resistor divider between V_{OUT1} and GND. With multiphase configurations, the FB1 and FB2 pins should be tied together and then connected to V_{OUT}.
	EP	Exposed Thermal Pad. Connect the exposed thermal pad to the signal/analog ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

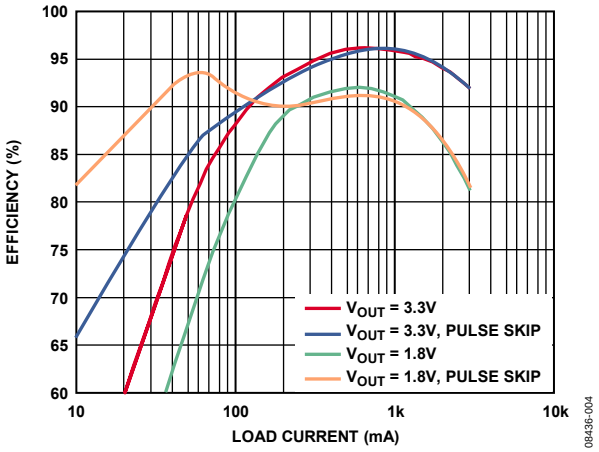


Figure 4. Efficiency vs. Load, V_{IN} = 5 V and f_{SW} = 300 kHz; V_{OUT} = 3.3 V, Inductor Cooper Bussmann DR1050-8R2-R, 8.2 µH, 15 mΩ; V_{OUT} = 1.8 V, Inductor TOKO FDV0620-4R7M, 4.7 µH, 53 mΩ

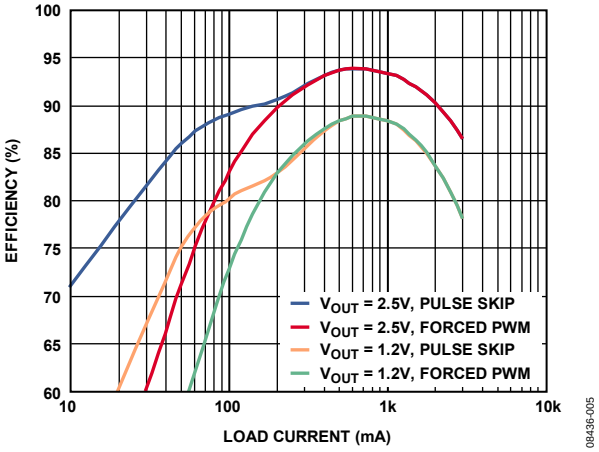


Figure 5. Efficiency vs. Load, V_{IN} = 5 V and f_{SW} = 600 kHz; V_{OUT} = 2.5 V, Inductor TOKO FDV0620-3R3M, 3.3 µH, 40 mΩ; V_{OUT} = 1.2 V, Inductor TOKO FDV0620-2R2M, 2.2 µH, 30 mΩ

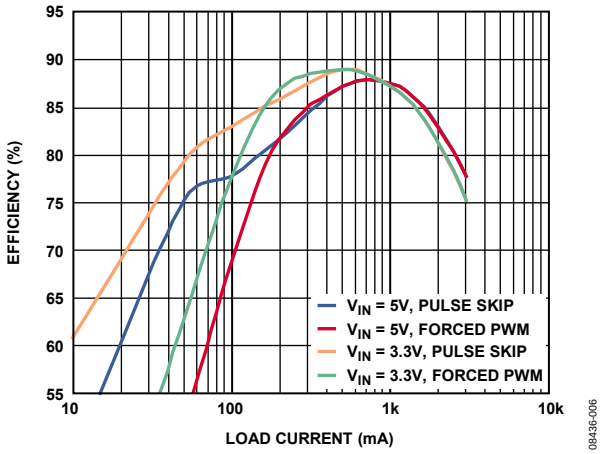


Figure 6. Efficiency vs. Load, V_{OUT} = 1.2 V and f_{SW} = 1.2 MHz; Inductor TOKO FDV0620-1R0M, 1.0 µH, 14 mΩ

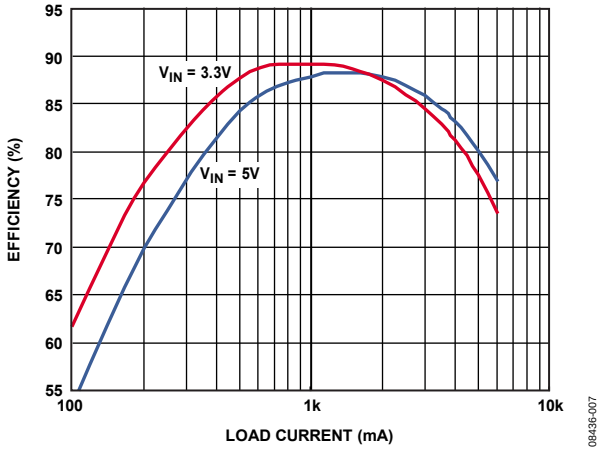


Figure 7. Efficiency, Combined Dual-Phase Output, V_{OUT} = 1.2 V and f_{SW} = 1.2 MHz; Inductor TOKO FDV0620-1R0M, 1.0 µH, 14 mΩ

LINE AND LOAD REGULATION

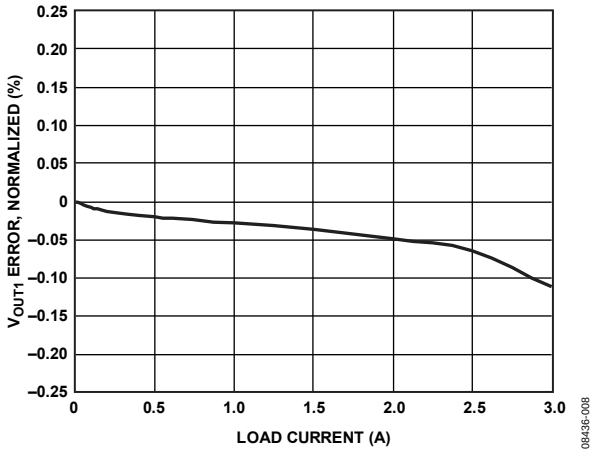


Figure 8. Load Regulation, Channel 1: V_{IN} = 5 V, f_{SW} = 600 kHz, and T_A = 25°C

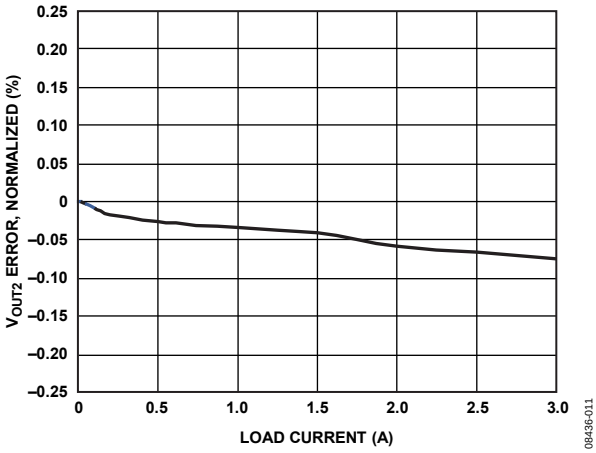


Figure 11. Load Regulation, Channel 2: V_{IN} = 5 V, f_{SW} = 600 kHz, and T_A = 25°C

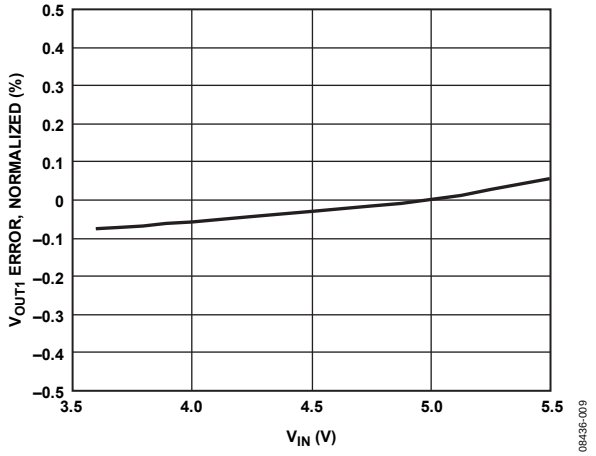


Figure 9. Line Regulation, Channel 1: Load Current = 3 A and f_{SW} = 600 kHz

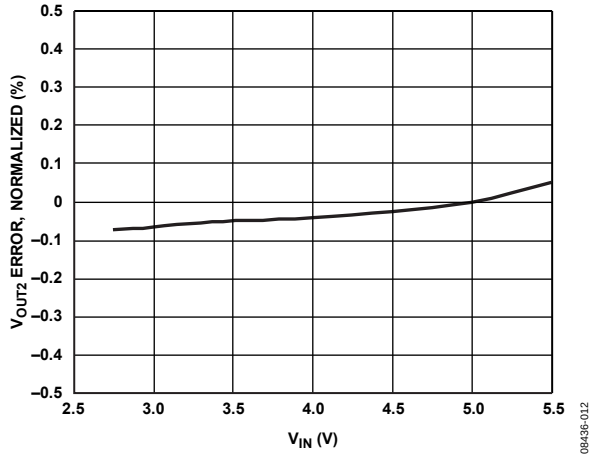


Figure 12. Line Regulation, Channel 2: Load Current = 3 A and f_{SW} = 600 kHz

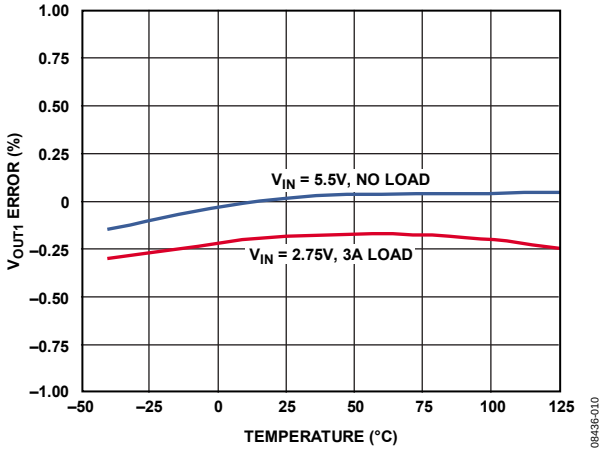


Figure 10. Output Voltage Error vs. Temperature, Channel 1: V_{OUT} = 0.6 V and f_{SW} = 600 kHz

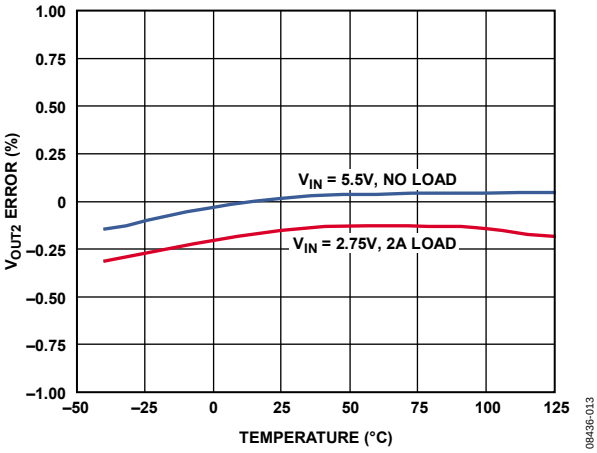


Figure 13. Output Voltage Error vs. Temperature, Channel 2: V_{OUT} = 1.5 V and f_{SW} = 600 kHz

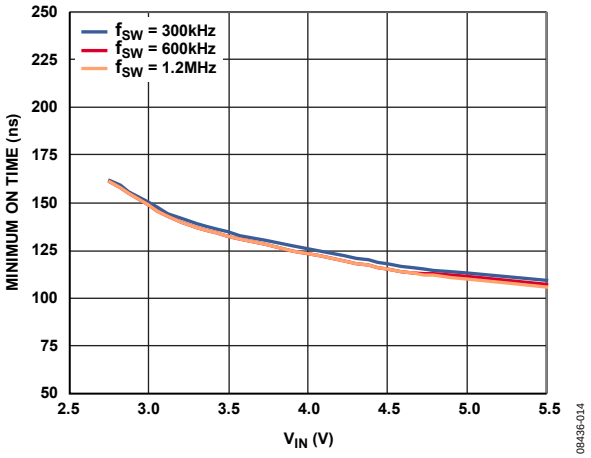


Figure 14. Minimum On Time, Open Loop, Includes Dead Time

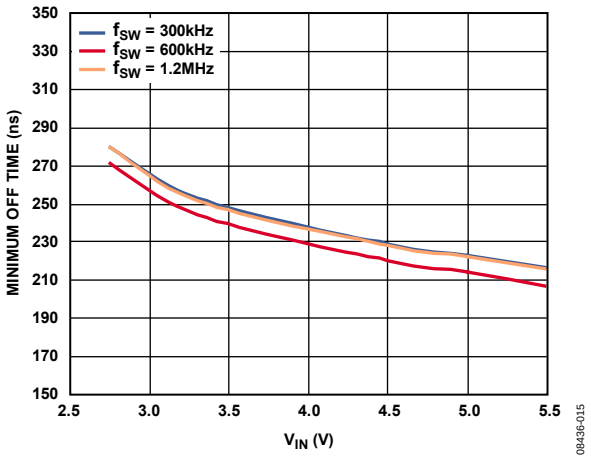


Figure 15. Minimum Off Time, Open Loop, Includes Dead Time

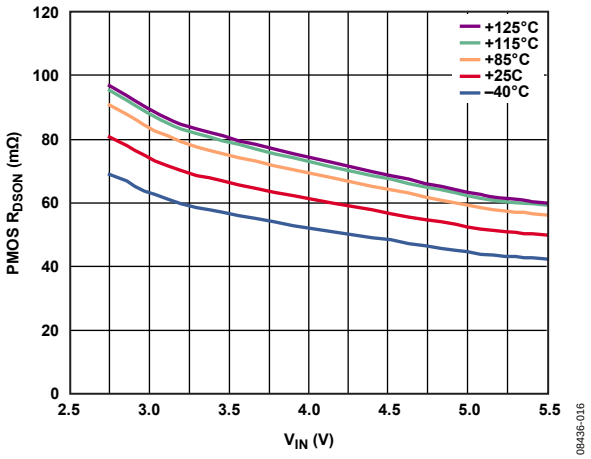


Figure 16. High-Side PMOS Resistance vs. Input Voltage, Includes Bond Wires

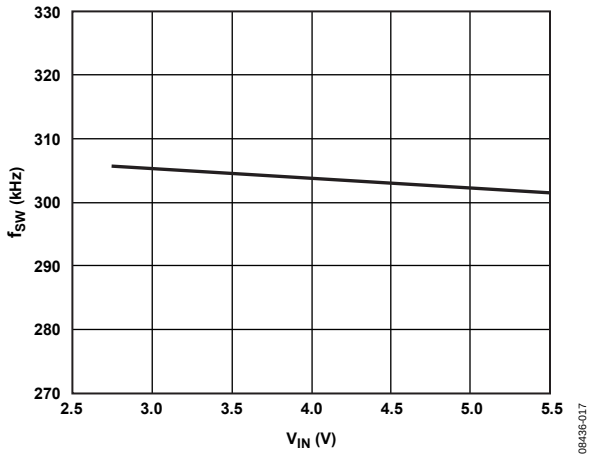


Figure 17. Switching Frequency vs. Input Voltage, f_{SW} = 300 kHz

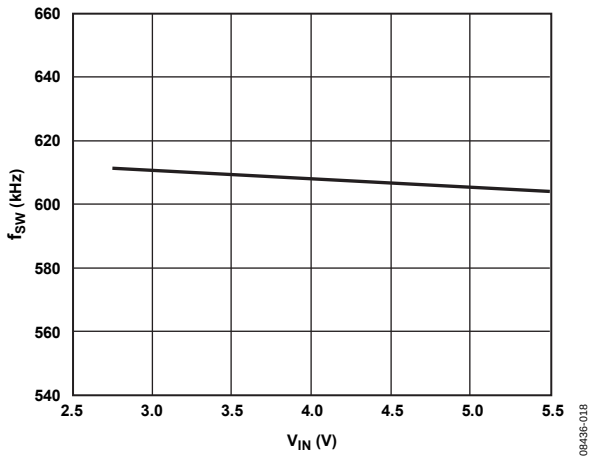


Figure 18. Switching Frequency vs. Input Voltage, f_{SW} = 600 kHz

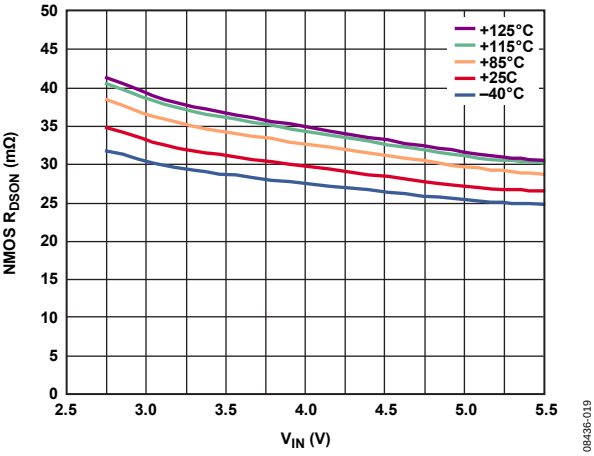


Figure 19. Low-Side NMOS Resistance vs. Input Voltage, Includes Bond Wires

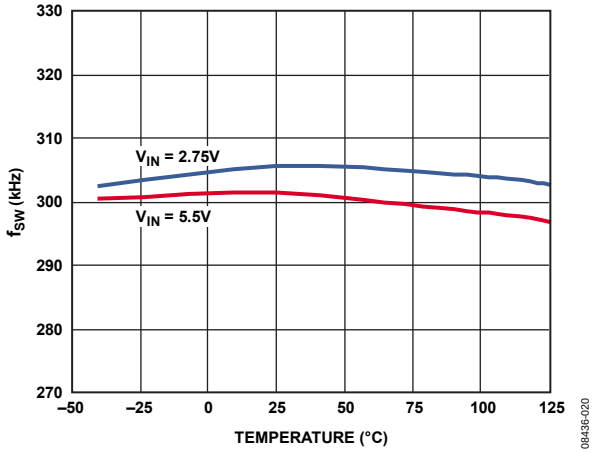


Figure 20. Switching Frequency vs. Temperature, f_{SW} = 300 kHz

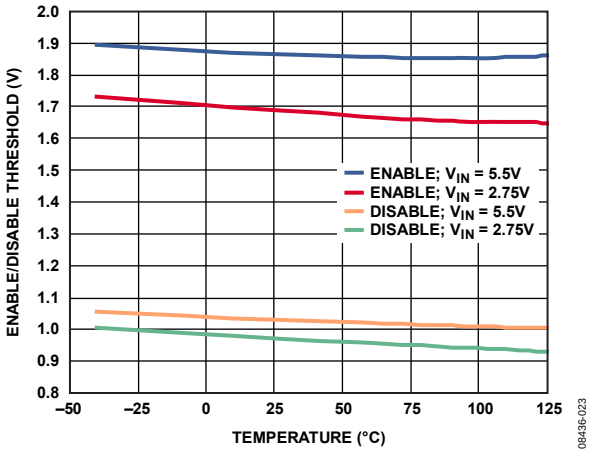


Figure 23. Enable/Disable Threshold vs. Temperature

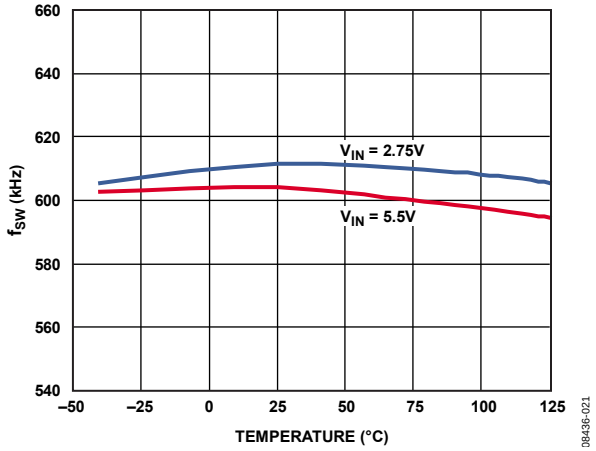


Figure 21. Switching Frequency vs. Temperature, f_{SW} = 600 kHz

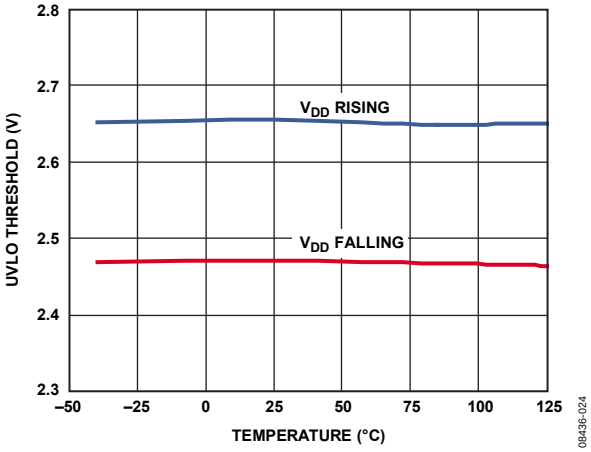


Figure 24. UVLO Threshold vs. Temperature

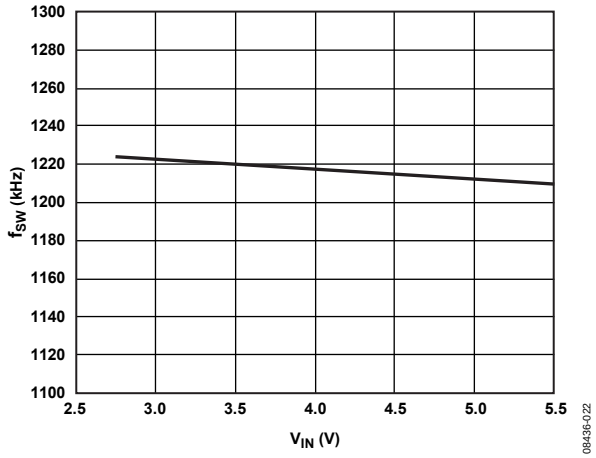


Figure 22. Switching Frequency vs. Input Voltage, f_{SW} = 1.2 MHz

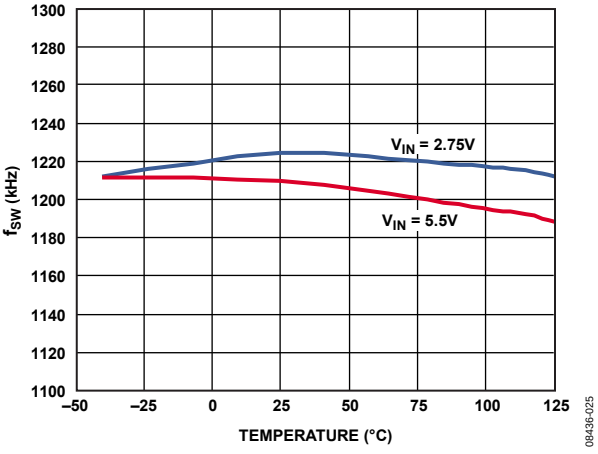


Figure 25. Switching Frequency vs. Temperature, f_{SW} = 1.2 MHz

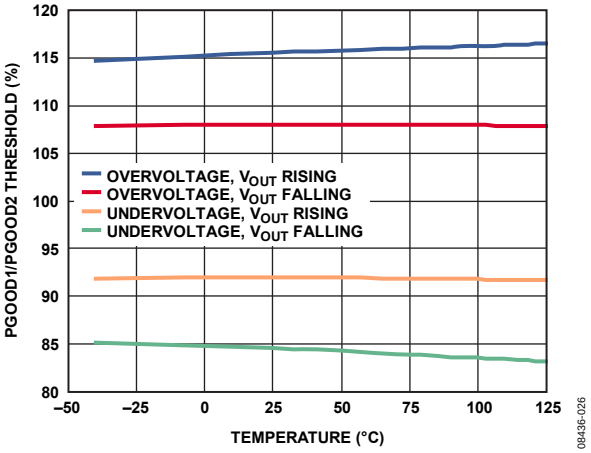


Figure 26. PGOOD1/PGOOD2 Threshold vs. Temperature

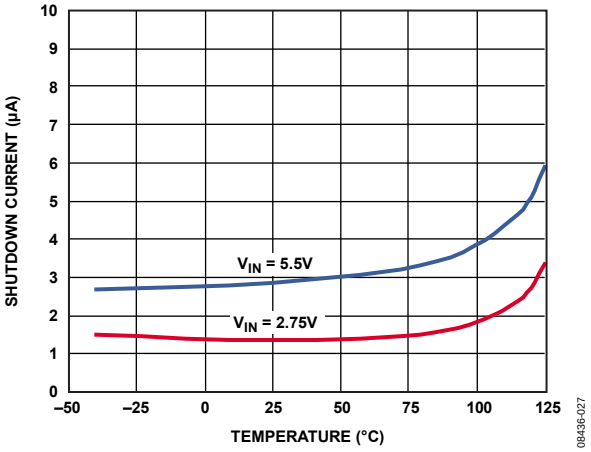


Figure 27. Shutdown Current vs. Temperature

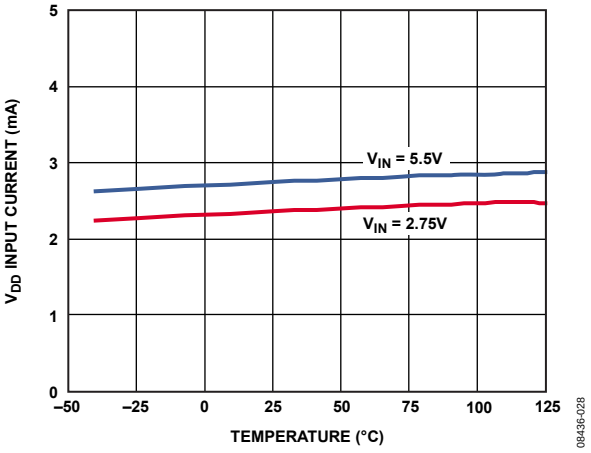


Figure 28. V_{DD} Input Current vs. Temperature, Not Switching

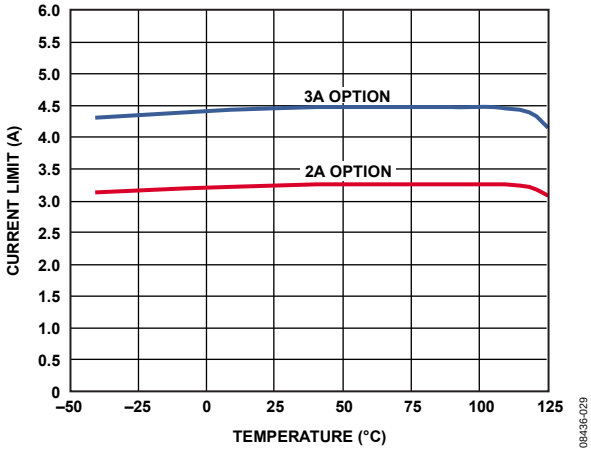


Figure 29. Peak Current Limit vs. Temperature, V_{IN} = 5 V

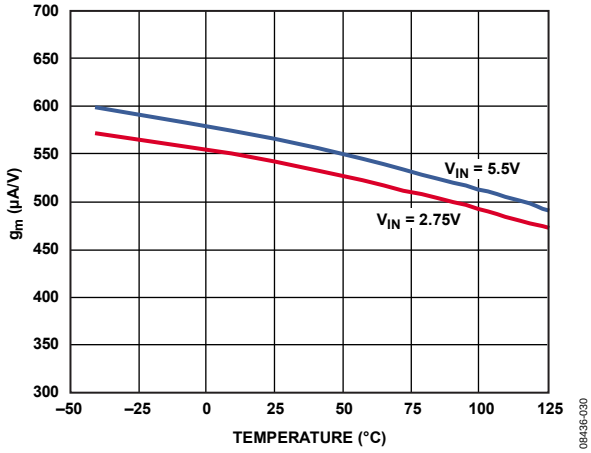


Figure 30. g_m vs. Temperature

SUPPLY CURRENT

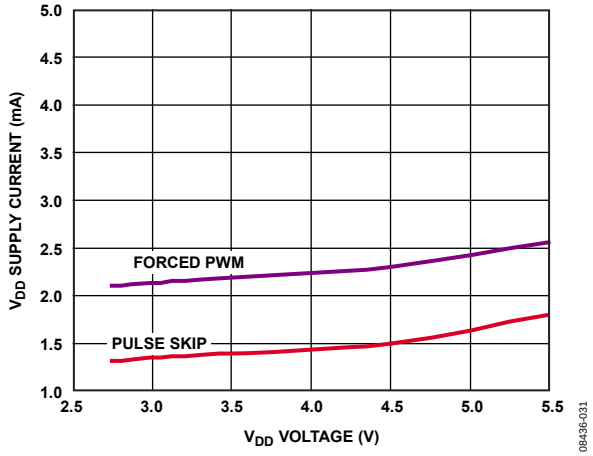


Figure 31. V_{DD} Supply Current, No Load, Channel 1: V_{OUT1} = 1.5 V, Channel 2: Off, f_{SW} = 1.2 MHz

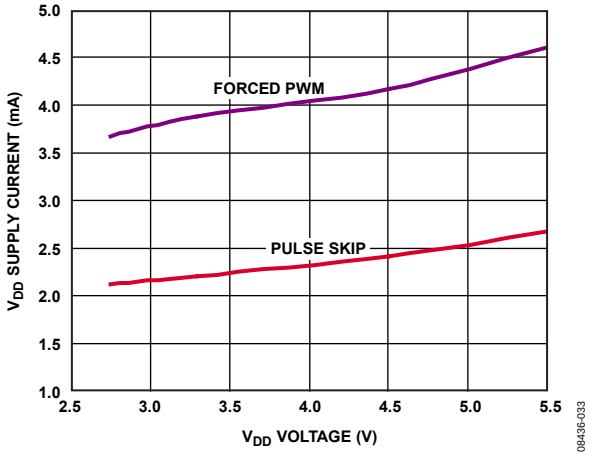


Figure 33. V_{DD} Supply Current, No Load, Channel 1: V_{OUT1} = 1.5 V, Channel 2: V_{OUT2} = 0.8 V, f_{SW} = 1.2 MHz

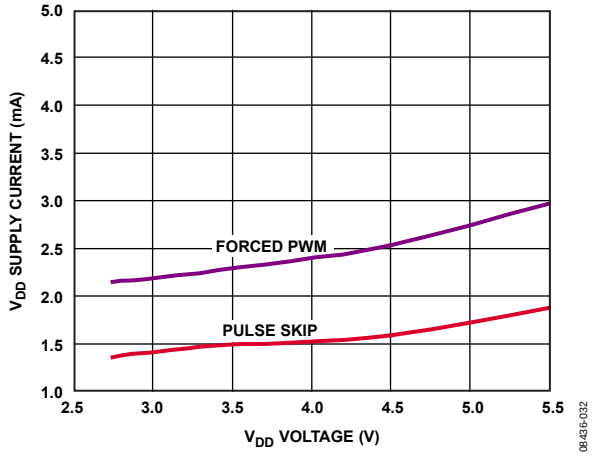


Figure 32. V_{DD} Supply Current, No Load, Channel 2: V_{OUT2} = 0.8 V, Channel 1: Off, f_{SW} = 1.2 MHz

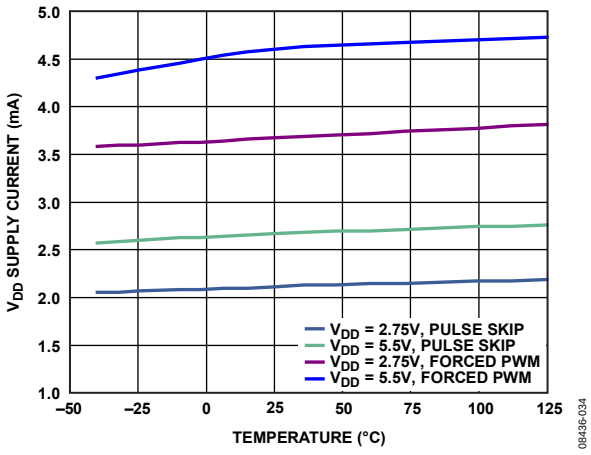


Figure 34. V_{DD} Supply Current vs. Temperature, Channel 1: V_{OUT1} = 1.5 V, Channel 2: V_{OUT2} = 0.8 V, f_{SW} = 1.2 MHz

LOAD TRANSIENT RESPONSE

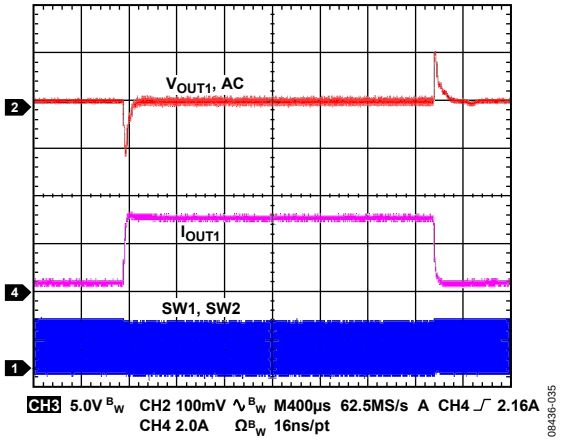


Figure 35. Load Transient Response in Pulse Skip Mode, Channel 1: 0.3 A to 3 A Load Step, V_{IN} = 5 V, V_{OUT} = 2.5 V, f_{SW} = 600 kHz (See Table 12 for the Circuit Details)

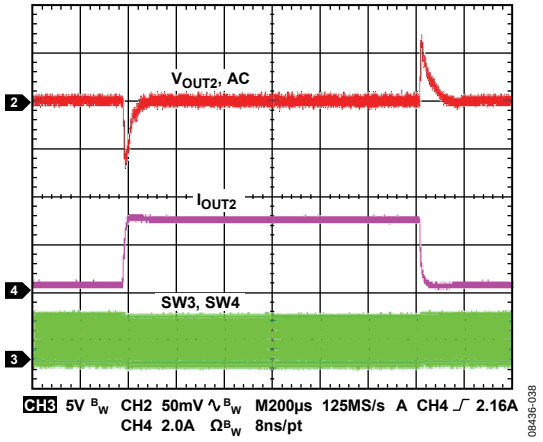


Figure 38. Load Transient Response in Pulse Skip Mode, Channel 2: 0.3 A to 3 A Load Step, V_{IN} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz (See Table 12 for the Circuit Details)

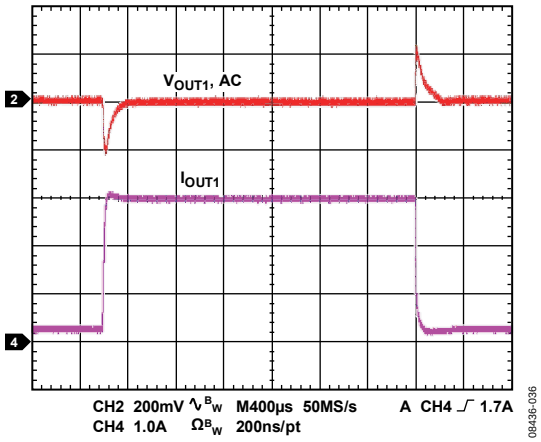


Figure 36. Load Transient Response in Pulse Skip Mode, Channel 1: 0.3 A to 3 A Load Step, V_{IN} = 5 V, V_{OUT} = 3.3 V, f_{SW} = 300 kHz (See Table 12 for the Circuit Details)

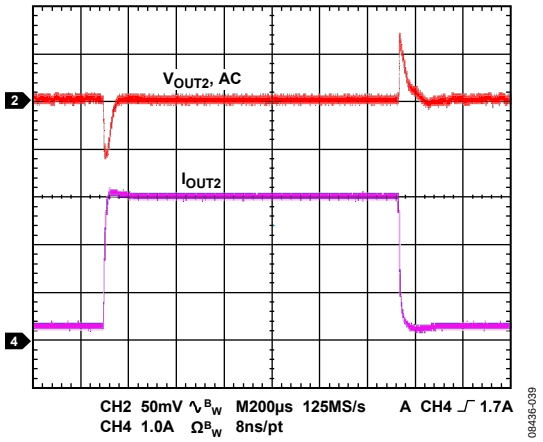


Figure 39. Load Transient Response in Pulse Skip Mode, Channel 2: 0.3 A to 3 A Load Step, V_{IN} = 3.3 V, V_{OUT} = 1.2 V, f_{SW} = 1.2 MHz (See Table 12 for the Circuit Details)

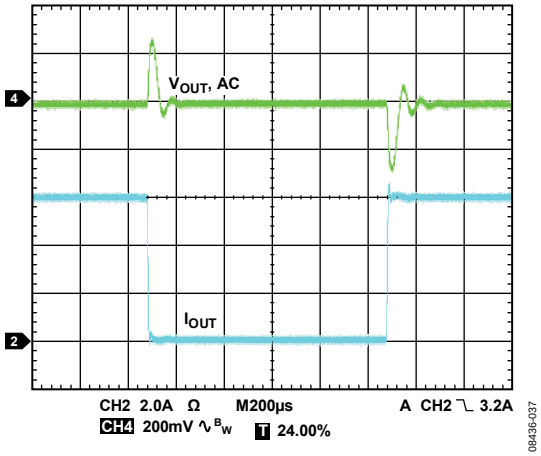


Figure 37. Load Transient Response in Forced PWM Mode, Combined Output: 0 A to 6 A Load Step, V_{IN} = 5 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz (See Table 12 for the Circuit Details)

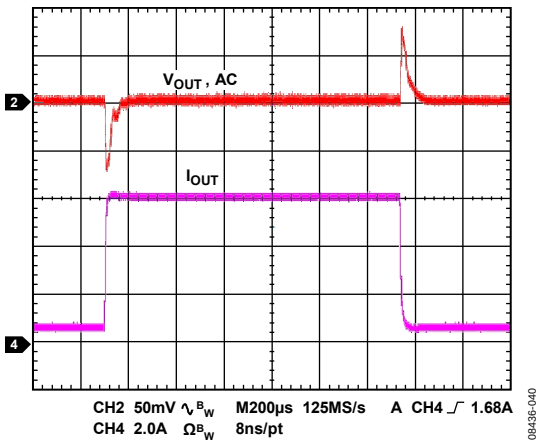


Figure 40. Load Transient Response in Forced PWM Mode, Combined Output: 0.6 A to 6 A Load Step, V_{IN} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz (See Table 12 for the Circuit Details)

BASIC FUNCTIONALITY

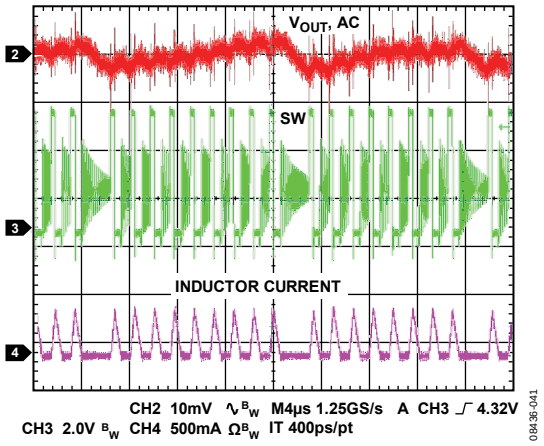


Figure 41. Pulse Skip Mode, 110 mA Load

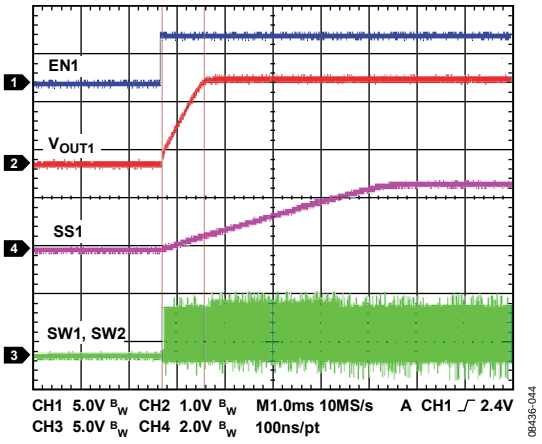


Figure 44. Soft Start, Channel 1: V_{OUT} = 1.8 V, C_{SS1} = 10 nF

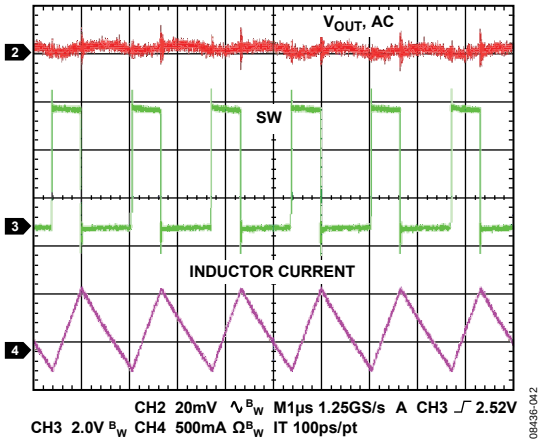


Figure 42. Forced PWM Mode, CCM Operation, 200 mA Load, f_{SW} = 600 kHz

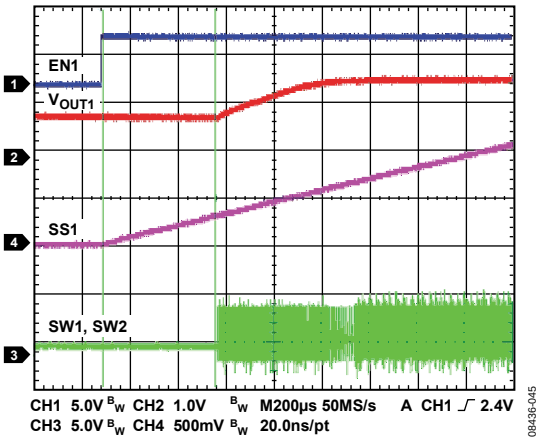


Figure 45. Soft Start with Precharged Output

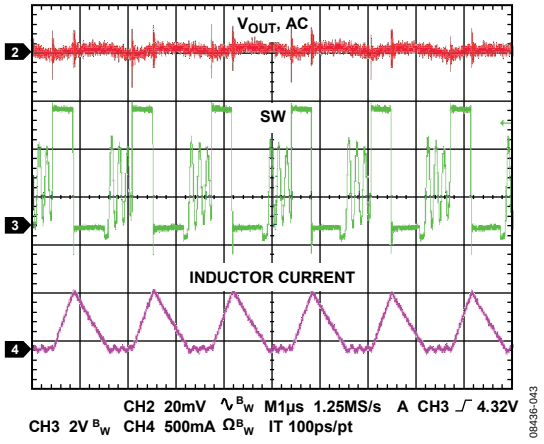


Figure 43. Pulse Skip Enabled, DCM Operation, 200 mA Load, f_{SW} = 600 kHz

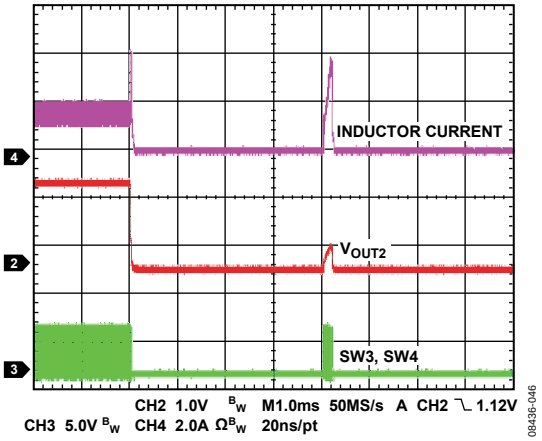


Figure 46. Current Limit Entry,
Channel 2: V_{OUT} = 1.8 V, 2 A Configuration, f_{SW} = 600 kHz

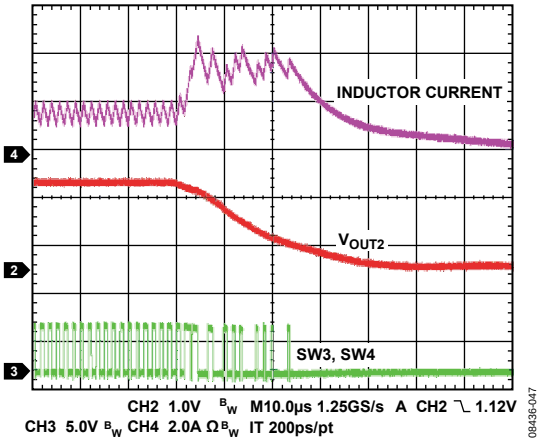


Figure 47. Current Limit Entry (Zoomed In), Channel 2: V_{OUT2} = 1.8 V, 2 A Configuration, f_{SW} = 600 kHz

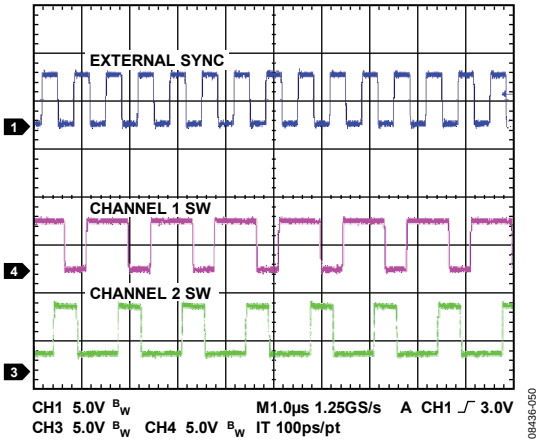


Figure 50. External Synchronization, f_{SYNC} = 1.5 MHz, f_{SW} = 750 kHz

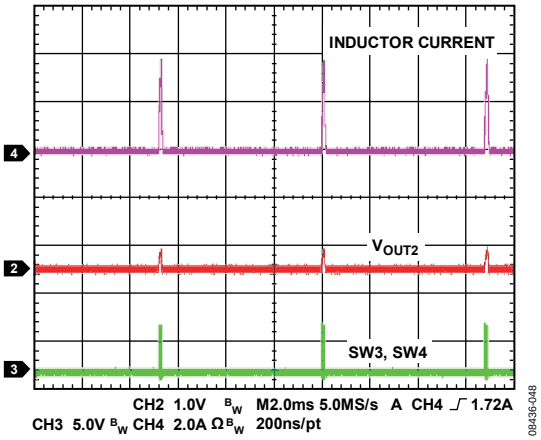


Figure 48. Hiccup Mode, f_{SW} = 600 kHz, 6.8 ms Hiccup Cycle

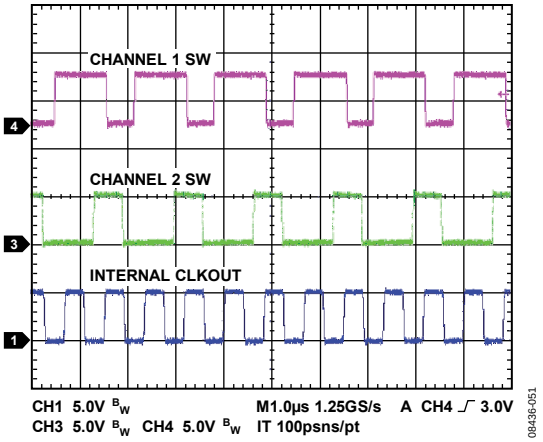


Figure 51. Internal Clock Output, f_{SW} = 600 kHz, f_{CLKOUT} = 1.2 MHz

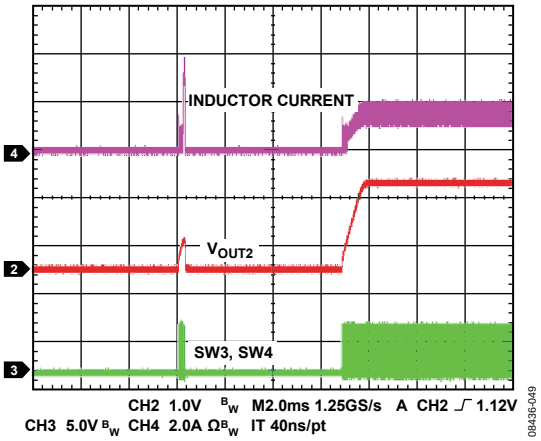


Figure 49. Exiting Hiccup Mode, Channel 2: V_{OUT2} = 1.8 V, f_{SW} = 600 kHz

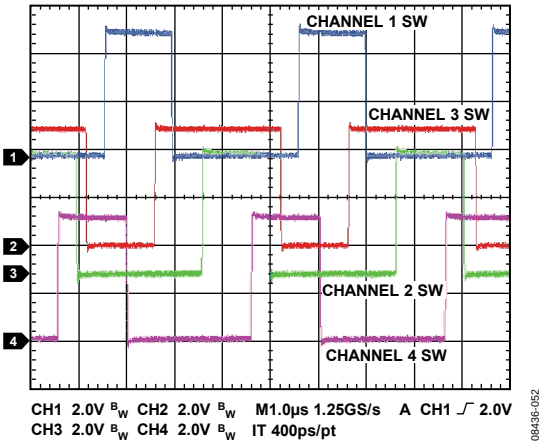


Figure 52. 4-Channel Operation, Two ADP2116 Devices, One Device Synchronizes the Other, 90° Phase-Shifted Switch Nodes

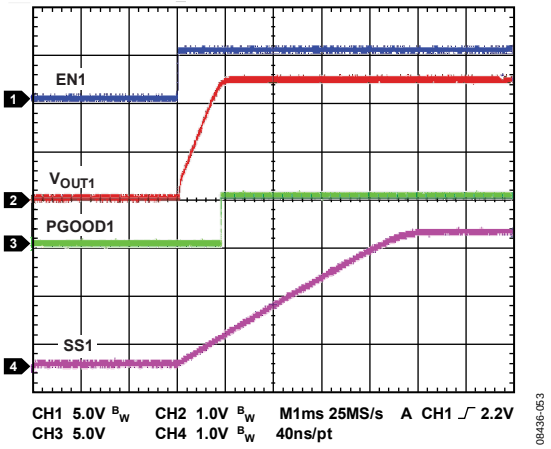


Figure 53. Power-Good Signal

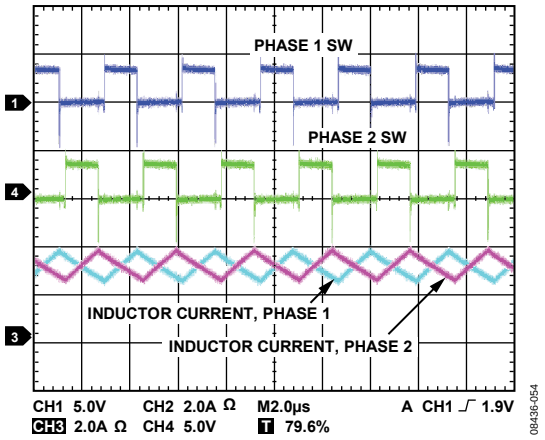
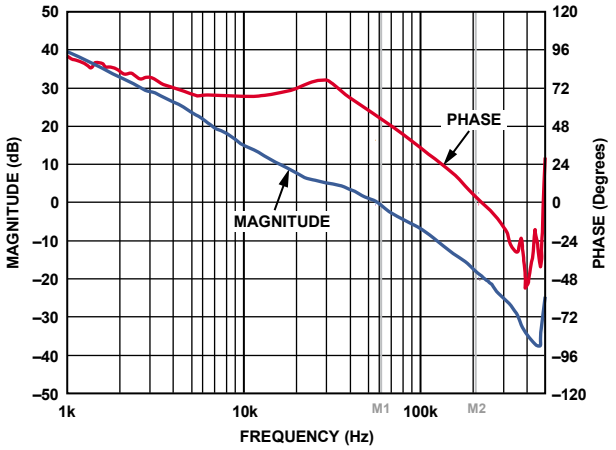


Figure 54. Combined Dual-Phase Output Operation, V_{OUT} = 1.2 V, f_{SW} = 300 kHz, 6 A Load

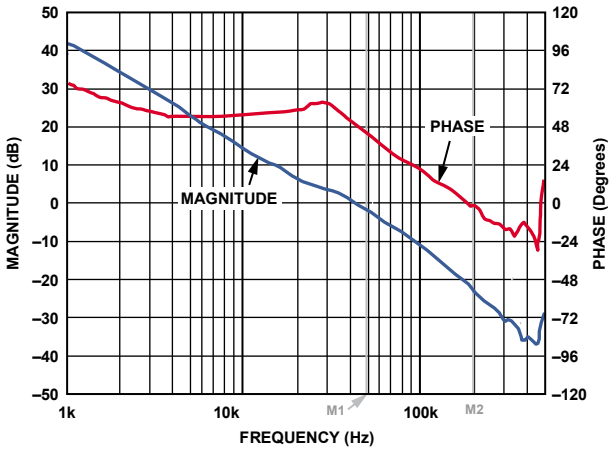
BODE PLOTS



	M1	M2	M2 – M1
FREQUENCY	56.62kHz	220.20kHz	163.58kHz
MAGNITUDE	0.029dB	–18.743dB	–18.772dB
PHASE	55.02°	–0.468°	–55.494°

08436-055

Figure 55. Magnitude and Phase vs. Frequency, V_{IN} = 5 V, V_{OUT} = 2.5 V, Load = 3 A, f_{SW} = 600 kHz, Crossover Frequency (f_{CROSS}) = 57 kHz, Phase Margin = 55° (See Table 12 for the Circuit Details)



	M1	M2	M2 – M1
FREQUENCY	46.12kHz	186.41kHz	140.29kHz
MAGNITUDE	–0.558dB	–20.906dB	–20.348dB
PHASE	47.275°	0.065°	–47.210°

08436-056

Figure 56. Magnitude and Phase vs. Frequency, V_{IN} = 5 V, V_{OUT} = 1.2 V, Load = 3 A, f_{SW} = 600 kHz, Crossover Frequency (f_{CROSS}) = 46 kHz, Phase Margin = 47° (See Table 12 for the Circuit Details)

SIMPLIFIED BLOCK DIAGRAM

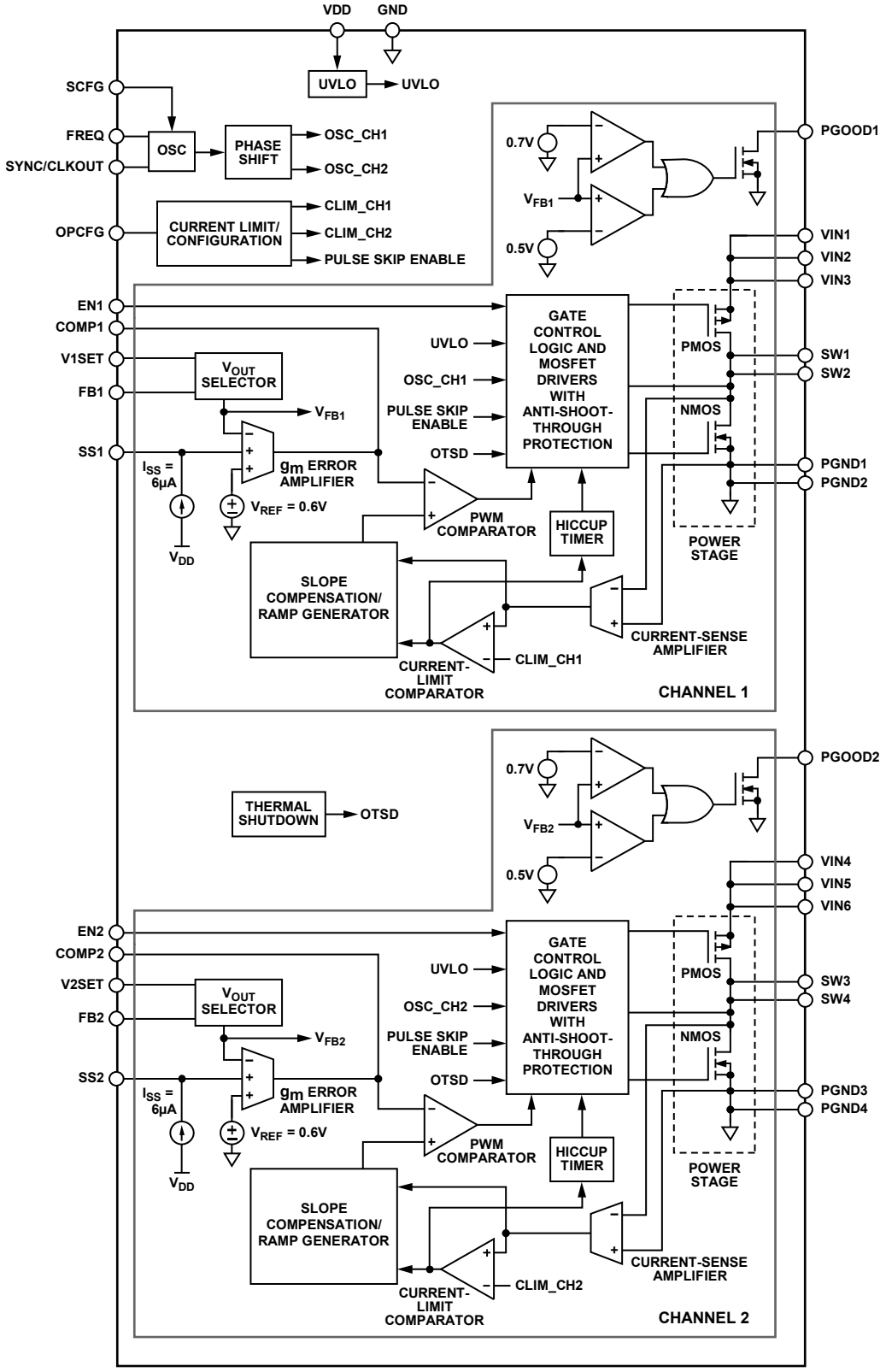


Figure 57. Simplified Block Diagram

THEORY OF OPERATION

The ADP2116 is a high efficiency, dual, fixed switching frequency, synchronous, step-down dc-to-dc converter with flex mode architecture, which is the Analog Devices, Inc., proprietary version of peak current mode control architecture. The device operates over an input voltage range of 2.75 V to 5.5 V. Each output channel can provide an adjustable output as low as 0.6 V and deliver up to 3 A of load current. When the output channels are tied together, they operate 180° out of phase to deliver up to 6 A of load current. The integrated high-side, P-channel power MOSFET and the low-side, N-channel power MOSFET yield high efficiency at medium to heavy loads. Pulse skip mode is available for improved efficiency at light loads. With a high switching frequency (up to 2 MHz) and integrated power switches, the ADP2116 is optimized to deliver high performance in a small package for power management solutions.

The ADP2116 also includes undervoltage lockout (UVLO) with hysteresis, soft start, and power good, as well as protection features such as output short-circuit protection and thermal shutdown. The output voltages, current limits, switching frequency, pulse skip operation, and soft start time are externally programmable with tiny resistors and capacitors.

CONTROL ARCHITECTURE

The ADP2116 consists of two step-down dc-to-dc converters that deliver regulated output voltages, V_{OUT1} and V_{OUT2} (see Figure 1), by modulating the duty cycle at which the internal high-side, P-channel power MOSFET and the low-side, N-channel power MOSFET are switched on and off.

In steady-state operation, the output voltage V_{OUT1} or V_{OUT2} is sensed on the corresponding feedback pin, FB1 or FB2, and attenuated in proportion to the selected output voltage on the V1SET or V2SET pin. An error amplifier integrates the error between the feedback voltage and the reference voltage (V_{REF} = 0.6 V) to generate an error voltage at the COMP1 or COMP2 pin. The valley inductor current is sensed by a current-sense amplifier when the low-side, N-channel MOSFET is on. An internal oscillator turns off the low-side, N-channel MOSFET and turns on the high-side, P-channel MOSFET at a fixed switching frequency.

When the high-side, P-channel MOSFET is enabled, the valley inductor current information is added to an emulated ramp signal and compared to the error voltage by the PWM comparator. The output of the PWM comparator modulates the duty cycle by adjusting the trailing edge of the PWM pulse that switches the power devices. Slope compensation is programmed internally into the emulated ramp signal and automatically selected, depending on the input voltage, output voltage, and switching frequency. This prevents subharmonic oscillations for greater than 50% duty cycle operation.

Control logic with the anti-shoot-through circuit monitors and adjusts the low-side and high-side driver outputs to ensure break-before-make switching. This monitoring and control prevents cross-conduction between the internal high-side, P-channel power MOSFET and the low-side, N-channel power MOSFET.

UNDERVOLTAGE LOCKOUT (UVLO)

The UVLO threshold is 2.65 V when V_{DD} is increasing and 2.47 V when V_{DD} is decreasing. The 180 mV hysteresis prevents the converter from turning off and on repeatedly in response to changing load conditions during a slow voltage transition on VDD that is close to the 2.75 V minimum operational level.

ENABLE/DISABLE CONTROL

The EN1 and EN2 pins are used to independently enable or disable Channel 1 and Channel 2, respectively. Drive ENx high to turn on the corresponding channel of the ADP2116. Drive ENx low to turn off the corresponding channel of the ADP2116, reducing the input current to less than 1 µA. To force a channel to start automatically when input power is applied, connect the corresponding ENx pin to VDD. When shut down, the ADP2116 channels discharge the soft start capacitor, causing a new soft start cycle every time the converters are reenabled.

SOFT START

The ADP2116 soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during startup. Soft start begins after the undervoltage lockout threshold is exceeded and an enable pin, EN1 or EN2, is pulled high to greater than 2.0 V. External capacitors to ground are required on both the SS1 and SS2 pins. Each regulating channel has its own soft start circuit. When the converter powers up and is enabled, the internal 6 µA current source charges the external soft start capacitor, establishing a voltage ramp slope at the SS1 or SS2 pin, as shown in Figure 58. The soft start time ends when the soft start ramp voltage exceeds the internal reference of 0.6 V.

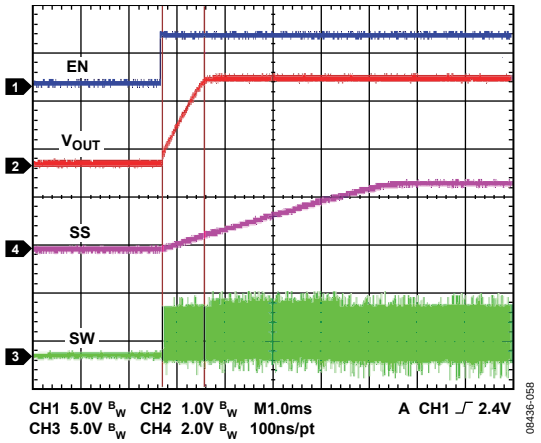


Figure 58. Soft Start

The capacitance value of the soft start capacitor defines the soft start time, t_{SS}, based on

$$\frac{V_{REF}}{t_{SS}} = \frac{I_{SS}}{C_{SS}} \quad (1)$$

where:
V_{REF} is the internal reference voltage, 0.6 V.
I_{SS} is the soft start current, 6 µA.
C_{SS} is the soft start capacitor value.

If the output voltage, V_{OUT1} or V_{OUT2}, is precharged prior to enabling Channel 1 or Channel 2, respectively, the control logic prevents inductor current reversal by keeping the power MOSFETs turned off until the soft start voltage ramp at SS1 or SS2 reaches the precharged output voltage on V_{FB1} or V_{FB2} (see Figure 59).

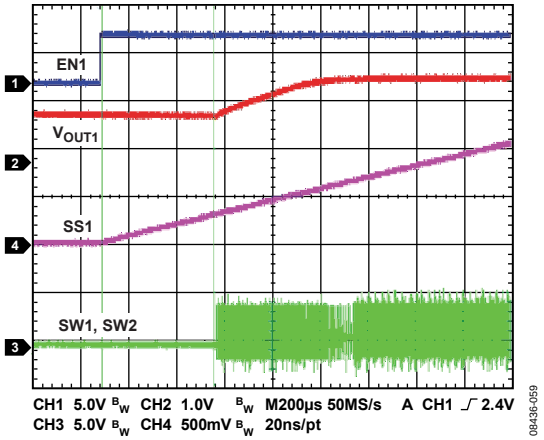


Figure 59. Soft Start with a Precharged Output

POWER GOOD

The ADP2116 features open-drain power-good outputs (PGOOD1 and PGOOD2) that indicate when the converter output voltage is within regulation. The power-good signal transitions low immediately when the corresponding channel is disabled.

The power-good circuitry monitors the output voltage on the FB1 or FB2 pin and compares it to the rising and falling thresholds specified in Table 1. If the rising output voltage (V_{OUT1} or V_{OUT2}) exceeds 116% of the target output voltage ($V_{OUT1SET}$ or $V_{OUT2SET}$), the PGOOD1 or PGOOD2 pin is held low. The PGOOD1 or PGOOD2 pin continues to be held low until the falling output voltage returns to 108% of the target value.

If the output voltage drops below 84% of the target output voltage, the corresponding PGOOD1 or PGOOD2 pin is held low. The PGOOD1 or PGOOD2 pin continues to be held low until the output voltage rises to within 92% of the target output voltage. The PGOOD1 or PGOOD2 pin is then released, signaling that the output voltage is within the power-good window.

The power-good thresholds are shown in Figure 60. The PGOOD1 and PGOOD2 outputs also sink current if an overtemperature condition is detected. Use these outputs as logic power-good signals by connecting the pull-up resistor from PGOOD1 or PGOOD2 to VDD. If the power-good function is not used, the pins can be left floating.

PULSE SKIP MODE

The ADP2116 has built-in pulse skip circuitry that turns on during light loads, switching only as necessary to maintain the output voltage within regulation. This allows the converter to maintain high efficiency during light load operation by reducing the switching losses. The pulse skip mode can be selected by configuring the OPCFG pin as indicated in Table 7. In pulse skip mode, when the output voltage dips below regulation, the ADP2116 enters PWM mode for a few oscillator cycles to increase the output voltage so that it is within regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies all of the load current. Because the output voltage dips and recovers occasionally, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

If the converter is configured to operate in forced PWM mode (by selecting this configuration using the OPCFG pin), the device operates with a fixed switching frequency, even at light loads.

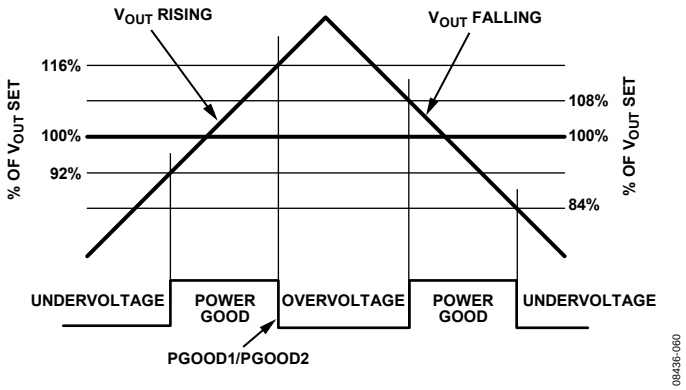


Figure 60. PGOOD1/PGOOD2 Thresholds

HICCUP MODE CURRENT LIMIT

The ADP2116 features a hiccup mode current-limit implementation. When the peak inductor current exceeds the preset current limit for more than eight consecutive clock cycles, the hiccup mode current-limit condition occurs. The channel then goes to sleep for 6.8 ms (at a 600 kHz switching frequency), which is enough time for the output to be discharged and the average power dissipation to be reduced. After the 6.8 ms elapses, the channel wakes up with a soft start period (see Figure 61). If the current-limit condition is subsequently triggered, the channel again goes to sleep and wakes up after 6.8 ms. The current limits for the two channels are programmed by configuring the OPCFG pin (see Table 7). For the 3 A/3 A option, the output current limit is set to 4.5 A per output. For the 3 A/2 A option, the current limits are set to 4.5 A and 3.3 A for V_{OUT1} and V_{OUT2}, respectively.

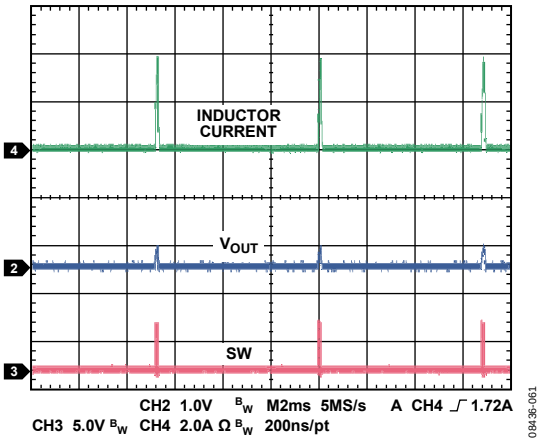


Figure 61. Hiccup Mode

THERMAL OVERLOAD PROTECTION

The ADP2116 has an internal temperature sensor that monitors the junction temperature. High current going into the switches or a hot printed circuit board (PCB) can cause the junction temperature of the ADP2116 to rise rapidly. When the junction temperature reaches approximately 150°C, the ADP2116 goes into thermal shutdown and the converter is turned off. When the junction temperature cools to less than 125°C, the ADP2116 resumes normal operation after the soft start sequence.

MAXIMUM DUTY CYCLE OPERATION

As the input voltage drops and approaches the output voltage, the ADP2116 smoothly transitions to maximum duty cycle operation, with the low-side, N-channel MOSFET switched on for the minimum off time. In maximum duty cycle operation, the output voltage dips below regulation because the output voltage is the product of the input voltage and the maximum duty cycle limitation. The maximum duty cycle limit is a function of the switching frequency and the input voltage, as shown in Figure 64.

SYNCHRONIZATION

The ADP2116 can be synchronized to an external clock such that the two channels operate at a switching frequency that is half of the input synchronization clock. The SYNC/CLKOUT pin can be configured as an input SYNC pin or an output CLKOUT pin through the SCFG pin, as detailed in Table 6. Through the input SYNC pin, the ADP2116 can be synchronized to an external clock such that the two channels switch at half the external clock frequency and are 180° out of phase. Through the output CLKOUT pin, the ADP2116 provides an output clock that is twice the switching frequency of the channels and 90° out of phase. Therefore, a single ADP2116 configured for the CLKOUT option acts as the master converter and provides an external clock for all other dc-to-dc converters (including other ADP2116 devices). These other converters are configured as slaves that accept an external clock and synchronize to it. This clock distribution approach synchronizes all dc-to-dc converters in the system and prevents beat harmonics that can lead to EMI issues.

The ADP2116 is optimized to power high performance signal chain circuits. The slew rate of the switch node is controlled by the size of the driver devices. Fast slewing of the switch node is desirable to minimize transition losses but can, in turn, lead to serious EMI issues due to parasitic inductance. To minimize EMI generation, the slew rate of the drivers is optimized such that the ADP2116 can match the performance of low dropout regulators in supplying sensitive signal chain circuits while also providing excellent power efficiency.

CONVERTER CONFIGURATION

SELECTING THE OUTPUT VOLTAGE

To set the output voltage, V_{OUT1} or V_{OUT2}, select one of the six fixed voltages, as shown in Table 4, by connecting the V1SET or V2SET pin to GND through a resistor of an appropriate value (see Figure 62). V1SET and V2SET set the voltage output levels for Channel 1 and Channel 2, respectively. The feedback pin, FB1 or FB2, should be directly connected to V_{OUT1} or V_{OUT2}.

Table 4. Output Voltage Programming

R_{V1SET} ± 5%	V_{OUT1} (V)	R_{V2SET} ± 5%	V_{OUT2} (V)
0 Ω to GND	0.8	0 Ω to GND	0.8
4.7 kΩ to GND	1.2	4.7 kΩ to GND	1.2
8.2 kΩ to GND	1.5	8.2 kΩ to GND	1.5
15 kΩ to GND	1.8	15 kΩ to GND	1.8
27 kΩ to GND	2.5	27 kΩ to GND	2.5
47 kΩ to GND	3.3	47 kΩ to GND	3.3
82 kΩ to GND	0.6 to <1.6 (adjustable)	82 kΩ to GND	0.6 to <1.6 (adjustable)
0 Ω to VDD	1.6 to 3.3 (adjustable)	0 Ω to VDD	1.6 to 3.3 (adjustable)

If the required output voltage, V_{OUT1} or V_{OUT2}, is in the adjustable range, from 0.6 V to <1.6 V, connect V1SET or V2SET through an 82 kΩ resistor to GND. For the adjustable output voltage range of 1.6 V to 3.3 V, tie V1SET or V2SET to VDD (see Table 4). The adjustable output voltage of the ADP2116 is externally set by a resistive voltage divider from the output voltage to the feedback pin (see Figure 63). The ratio of the resistive voltage divider sets the output voltage, whereas the absolute value of these resistors sets the divider string current. For lower divider string currents, the small 10 nA (100 nA maximum) feedback bias current should be taken into account when calculating the resistor values. The feedback bias current can be ignored for a higher divider string current; however, this degrades efficiency at very light loads.

To limit output voltage accuracy degradation due to feedback bias current to less than 0.05% (0.5% maximum), ensure that the divider string current is greater than 20 µA. To calculate the desired resistor values, first determine the value of the bottom divider string resistor, R1, using the following equation:

$$R1 = V_{REF}/I_{STRING} \quad (2)$$

where:
V_{REF} is the internal reference voltage, 0.6 V.
I_{STRING} is the resistor divider string current.

When R1 is determined, calculate the value of the top resistor, R2, using the following equation:

$$R2 = R1\left[\frac{V_{OUT} - V_{REF}}{V_{REF}}\right] \quad (3)$$

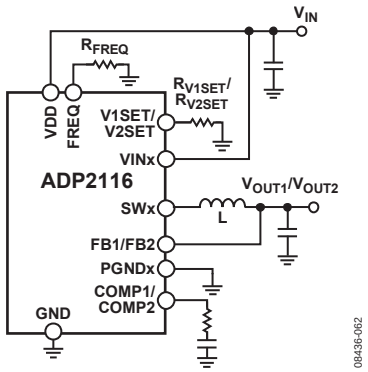


Figure 62. Configuration for Fixed Outputs

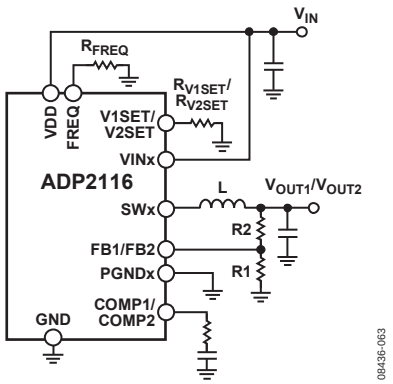


Figure 63. Configuration for Adjustable Outputs

SETTING THE OSCILLATOR FREQUENCY

The ADP2116 channels can be set to operate in one of three preset switching frequencies: 300 kHz, 600 kHz, or 1.2 MHz. For 300 kHz operation, connect the FREQ pin to GND. For 600 kHz or 1.2 MHz operation, connect a resistor between the FREQ pin and GND (see Table 5).

Table 5. Oscillator Frequency Setting

R_{FREQ} ± 5%	f_{SW} (kHz)
0 Ω to GND	300
8.2 kΩ to GND	600
27 kΩ to GND	1200

The choice of the switching frequency depends on the required dc-to-dc conversion ratio and the need for small external components. In addition, due to the minimum on and off times required for current sensing and robust operation, the frequency is limited by the minimum and maximum controllable duty cycle (see Figure 64).

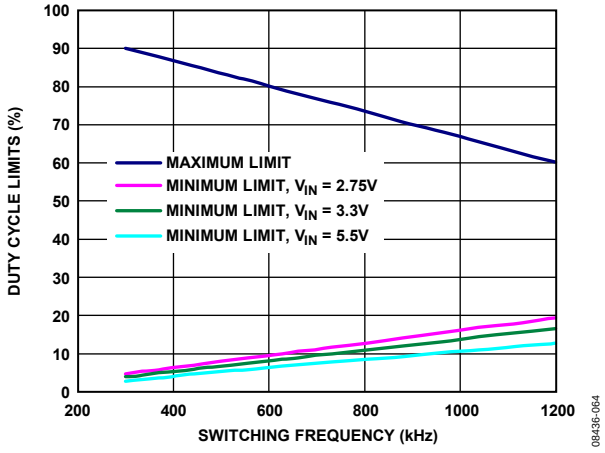


Figure 64. Duty Cycle Working Limits

For small, area-limited power solutions, use of higher switching frequencies is recommended. For single-output, multiphase applications that operate at close to 50% duty cycle, use a 1.2 MHz switching frequency to minimize crosstalk between the phases.

SYNCHRONIZATION AND CLKOUT

The ADP2116 can be configured to output an internal clock or to synchronize to an external clock at the SYNC/CLKOUT pin. The SYNC/CLKOUT pin is a bidirectional pin configured by the SCFG pin (see Table 6).

Table 6. SYNC/CLKOUT Configuration Setting

SCFG	SYNC/CLKOUT
GND	Input (SYNC)
VDD	Output (CLKOUT)

The converter switching frequency, f_{SW}, is half of the synchronization frequency, f_{SYNC} or f_{CLKOUT}, as shown in Equation 4, irrespective of whether SYNC/CLKOUT is configured as an input or an output.

$$f_{SYNC} \text{ (or } f_{CLKOUT}) = 2 \times f_{SW} \quad (4)$$

An external clock can be applied to the SYNC/CLKOUT pin when configured as an input to synchronize multiple ADP2116 devices to the same external clock. The f_{SYNC} range is 400 kHz to 4 MHz, which produces f_{SW} in the 200 kHz to 2 MHz range (see Figure 65).

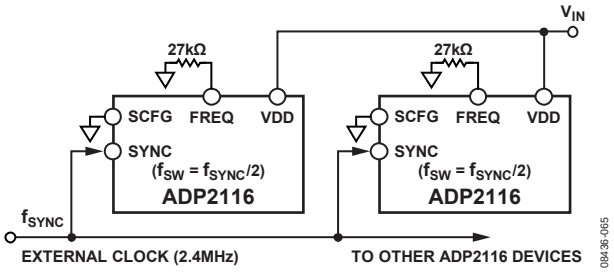


Figure 65. Synchronization with External Clock (f_{SW} = 1.2 MHz)

When synchronizing to an external clock, the switching frequency (f_{SW}) must be set close to half of the expected external clock frequency by appropriately terminating the FREQ pin (see Table 5).

The ADP2116 can also be configured to output a clock signal on the SYNC/CLKOUT pin that can be used to synchronize multiple ADP2116 devices (see Figure 66). The CLKOUT signal is 90° phase shifted relative to the internal clock of the channels so that the master ADP2116 and the slave channels are out of phase (see Figure 67 for additional information).

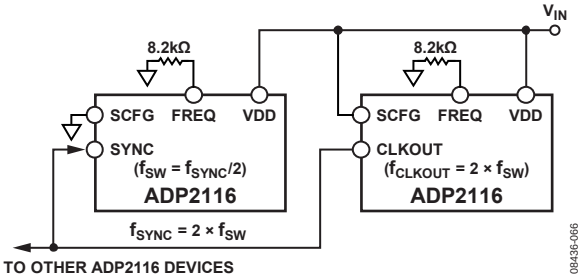


Figure 66. ADP2116 to Synchronize with Another ADP2116 (f_{SW} = 600 kHz; the SCFG Pin of the Master Is Tied to VDD)

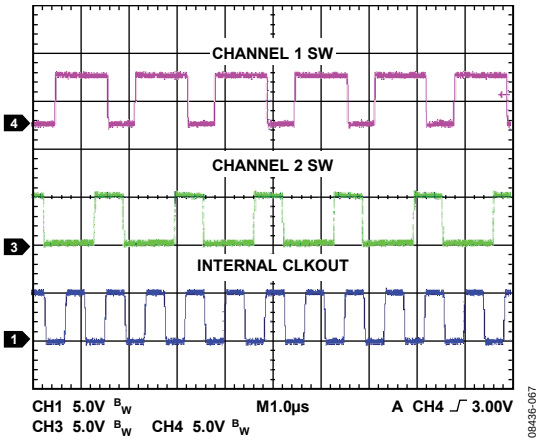


Figure 67. CLKOUT Waveforms

OPERATION MODE CONFIGURATION

The dual-channel ADP2116 can be configured to one of four modes of operation by connecting the OPCFG pin as detailed in Table 7. The configuration sets the current limit for each channel and enables or disables the transition to pulse skip mode at light loads.

In the dual-phase configuration, the outputs of the two channels are connected together and generate a single dc output voltage, V_{OUT}. For this single combined dual-phase output, only Mode 1 (see Table 7) can be used. In this mode, the error amplifiers of both phases are used. The feedback pins (FB1 and FB2) are tied together, the compensation pins (COMP1 and COMP2) are tied together, the soft start pins (SS1 and SS2) are tied together, and the enable pins (EN1 and EN2) are tied together.

In addition, if the power-good feature is used, PGOOD1 and PGOOD2 should be tied together and then connected to VDD using a single pull-up resistor.

When the ADP2116 is synchronized to an external clock, the converters always operate in fixed-frequency CCM and do not enter pulse skip mode at light loads. In this case, when configuring the OPCFG pin, choose forced PWM mode.

Table 7. Current-Limit Operation Mode and Configuration

Mode	R_{OPCFG} ± 5%	Maximum Output Current, I_{OUT1} (A)/I_{OUT2} (A)	Peak Current Limit, I_{LIMIT1} (A)/I_{LIMIT2} (A)	Power Savings at Light Load
1	0 Ω to VDD	3/3	4.5/4.5	Forced PWM
2	82 kΩ to GND	3/3	4.5/4.5	Pulse skip enabled
3	47 kΩ to GND	3/2	4.5/3.3	Forced PWM
4	27 kΩ to GND	3/2	4.5/3.3	Pulse skip enabled

EXTERNAL COMPONENTS SELECTION

ADIsimPower DESIGN TOOL

The ADP2116 is supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

INPUT CAPACITOR SELECTION

The input current to a buck converter is pulsating in nature. The current is zero when the high-side switch is off and approximately equal to the load current when the high-side switch is on. Because this pulsation occurs at reasonably high frequencies (300 kHz to 1.2 MHz), the input bypass capacitor supplies most of the high frequency current (ripple current), allowing the input power source to supply only the average (dc) current. The input capacitor needs a sufficient ripple current rating to handle the input ripple, as well as an ESR that is low enough to mitigate the input voltage ripple. For the ADP2116, place a 22 µF, 6.3 V X5R ceramic capacitor close to the VINx pin for each channel. X5R or X7R dielectrics are recommended with a voltage rating of 6.3 V or 10 V. Y5V and Z5U dielectrics are not recommended due to their poor temperature and dc bias characteristics.

VDD RC FILTER

It is recommended that the input power, V_{IN}, be apply to the VDD pin through a low-pass RC filter, as shown in Figure 68. Connecting a 10 Ω resistor in series with V_{IN} and a 1 µF, 6.3 V X5R (or X7R) ceramic capacitor between VDD and GND creates a 16 kHz (−3 dB) low-pass filter that effectively attenuates voltage glitches on the input power rail caused by the switching regulator. This provides a clean power supply to the internal, sensitive analog and digital circuits in the ADP2116, ensuring robust operation.

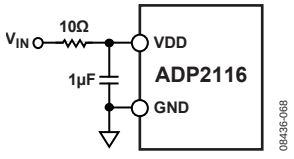


Figure 68. Low-Pass Filter at VDD

INDUCTOR SELECTION

The high switching frequency of the ADP2116 allows for minimal output voltage ripple even with small inductors. The size of the inductor is a trade-off between efficiency and transient response. A small inductor leads to larger inductor current ripple that provides excellent transient response but degrades efficiency. Due to the high switching frequency of the ADP2116, shielded ferrite core inductors are recommended for their low core losses and low EMI.

As a guideline, the inductor peak-to-peak current ripple, ΔI_L, is typically set to be one-third of the maximum load current for optimal transient response and efficiency.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \approx \frac{I_{LOAD(MAX)}}{3}$$

$$\Rightarrow L_{IDEAL} = \frac{3 \times V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times V_{IN} \times I_{LOAD(MAX)}} \quad (5)$$

where:
V_{IN} is the input voltage on the VINx terminal.
V_{OUT} is the desired output voltage.
f_{SW} is the converter switching frequency.

The internal slope compensation introduces additional limitations on the optimal inductor value for stable operation because the internal ramp is scaled for each V_{OUT} setting. The limits for different V_{IN}, V_{OUT}, and f_{SW} combinations are listed in Table 8.

Table 8. Minimum and Maximum Inductor Values

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	Min L (µH)	Max L (µH)
300	5	3.3	6.8	10
300	5	2.5	5.6	15
300	3.3	2.5	5.6	6.8
300	5	1.8	4.7	12
300	3.3	1.8	4.7	8.2
300	5	1.5	2.2	12
300	3.3	1.5	2.2	8.2
300	5	1.2	2.2	10
300	3.3	1.2	2.2	8.2
300	5	0.8	1.5	6.8
300	3.3	0.8	1.5	6.8
600	5	3.3	3.3	4.7
600	5	2.5	3.3	6.8
600	3.3	2.5	3.3	3.3
600	5	1.8	2.2	6.8
600	3.3	1.8	2.2	3.3
600	5	1.5	1.5	5.6
600	3.3	1.5	1.5	4.7
600	5	1.2	1.5	4.7
600	3.3	1.2	1.5	3.3
600	5	0.8	1.0	3.3
600	3.3	0.8	1.0	3.3
1200	5	2.5	1.0	3.3
1200	5	1.8	1.0	3.3
1200	3.3	1.8	1.0	2.2
1200	5	1.5	0.8	2.2
1200	3.3	1.5	0.8	2.2
1200	5	1.2	0.8	2.2
1200	3.3	1.2	0.8	2.2
1200	5	0.8	0.47	1.5
1200	3.3	0.8	0.47	1.5

To avoid saturation, the rated current of the inductor must be larger than the maximum peak inductor current, I_{L_PEAK}, given by

$$I_{L\_PEAK} = I_{LOAD\_MAX} + \frac{\Delta I_L}{2} \quad (6)$$

where:
I_{LOAD_MAX} is the maximum dc load current.
ΔI_L is the peak-to-peak inductor ripple current.

The ADP2116 can be configured in either a 3 A/3 A or 3 A/2 A current-limit configuration; therefore, the current-limit thresholds for the two channels are different in each setting. The inductor chosen for each channel must have at least the peak output current limit of the IC in each case for robust operation during short-circuit conditions. The following inductors are recommended:

- For 0.47 µH to 4.7 µH, the TOKO D53LC and FDV0620 series inductors
- For 4.7 µH to 15 µH, the Cooper Bussmann DR1050 series and the Würth Elektronik WE-PDF series

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the converter. The ADP2116 is designed for operation with small ceramic output capacitors that have low ESR and low ESL and are, therefore, easily able to meet stringent output voltage ripple specifications. X5R or X7R dielectrics are recommended with a voltage rating of 6.3 V or 10 V. Y5V and Z5U dielectrics are not recommended due to their poor temperature and dc bias characteristics. The minimum output capacitance, C_{OUT_MIN}, is determined by Equation 7 and Equation 8.

An acceptable maximum output voltage ripple is

$$\Delta V_{RIPPLE} \cong \Delta I_L \times \left(ESR + \frac{1}{8 \times f_{SW} \times C_{OUT\_MIN}} \right) \quad (7)$$

Therefore,

$$C_{OUT\_MIN} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (\Delta V_{RIPPLE} - \Delta I_L \times ESR)} \quad (8)$$

where:
ΔV_{RIPPLE} is the allowable peak-to-peak output voltage ripple in volts.
ΔI_L is the inductor ripple current.
ESR is the equivalent series resistance of the capacitor in ohms.
f_{SW} is the converter switching frequency in hertz.

If there is a step load, choose the output capacitor value based on the value of the step load. For the maximum acceptable output voltage droop/overshoot caused by the step load,

$$C_{OUT\_MIN} \cong \Delta I_{OUT\_STEP} \times \left(\frac{3}{f_{SW} \times \Delta V_{DROOP}} \right) \quad (9)$$

where:
ΔI_{OUT_STEP} is the load step value in amperes.
f_{SW} is the switching frequency in hertz.
ΔV_{DROOP} is the maximum allowable output voltage droop/overshoot in volts for the load step.

Note that the previous equations are approximations and are based on the following assumptions:

- The inductor value is based on the peak-to-peak current being 30% of the maximum load current.
- Voltage drops across the internal MOSFET switches and across the dc resistance of the inductor are ignored.
- In Equation 9, it is assumed that it takes up to three switching cycles until the loop adjusts the inductor current in response to the load step.

Select the largest output capacitance given by Equation 8 and Equation 9. When choosing the type of ceramic capacitor for the output filter of the converter, select a capacitor with a nominal capacitance that is 20% to 30% larger than the calculated value because the effective capacitance decreases with larger dc voltages. In addition, the rated voltage of the capacitor must be higher than the output voltage of the converter.

Recommended input and output ceramic capacitors include

- Murata GRM21BR61A106KE19L, 10 µF, 10 V, X5R, 0805
- TDK C2012X5R0J226M, 22 µF, 6.3 V, X5R, 0805
- Taiyo Yuden JMK212BJ476MG-T, 47 µF, 6.3 V, X5R, 0805
- Murata GRM32ER60J476ME20L, 47 µF, 6.3 V, X5R, 1210
- Murata GRM32ER60J107ME20L, 100 µF, 6.3 V, X5R, 1210

CONTROL LOOP COMPENSATION

The ADP2116 uses a peak current-mode control architecture for excellent load and line transient response. The external voltage loop is compensated by a transconductance amplifier with a simple external RC network between the COMP1 or COMP2 pin and GND, as shown in Figure 69.

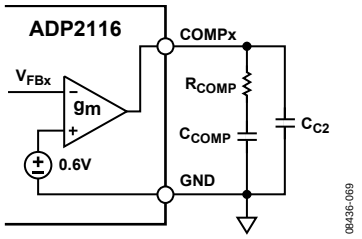


Figure 69. Compensation Components

The basic control loop block diagram is shown in Figure 70. The blocks and components shown enclosed within the dashed line in Figure 70 are embedded inside each channel of the ADP2116.

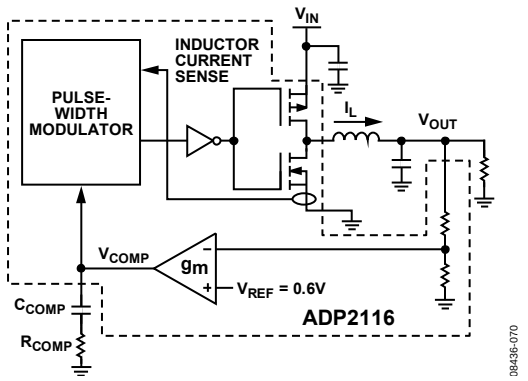


Figure 70. Basic Control Loop Block Diagram

The control loop can be broken down into the following three sections:

- V_{OUT} to V_{COMP}
- V_{COMP} to I_L
- I_L to V_{OUT}

Correspondingly, there are three transfer functions:

$$\frac{V_{COMP}(s)}{V_{OUT}(s)} = \frac{V_{REF}}{V_{OUT}} \times g_m \times Z_{COMP}(s) \quad (10)$$

$$\frac{I_L(s)}{V_{COMP}(s)} = G_{CS} \quad (11)$$

$$\frac{V_{OUT}(s)}{I_L(s)} = Z_{FILT}(s) \quad (12)$$

where:
s is the angular frequency that can be written as s = 2πf.
g_m is the transconductance of the error amplifier, 550 µS.
G_{CS} is the current-sense gain, 4 A/V.
V_{OUT} is the output voltage of the converter.
V_{REF} is the internal reference voltage, 0.6 V.
Z_{COMP} is the impedance of the RC compensation network.
Z_{FILT} is the impedance of the output filter.

$Z_{COMP}(s)$ is the impedance of the RC compensation network that forms a pole at origin and a zero as expressed in Equation 13.

$$Z_{COMP}(s) = \frac{1 + s \times R_{COMP} \times C_{COMP}}{s \times C_{COMP}} \quad (13)$$

$Z_{FILT}(s)$ is the impedance of the output filter and is expressed as

$$Z_{FILT}(s) = \frac{R_{LOAD}}{1 + s \times R_{LOAD} \times C_{OUT}} \quad (14)$$

where s is the angular frequency that can be written as s = 2πf.

The overall loop gain, H(s), is obtained by multiplying the three transfer functions previously mentioned as follows:

$$H(s) = g_m \times G_{CS} \times \frac{V_{REF}}{V_{OUT}} \times Z_{COMP}(s) \times Z_{FILT}(s) \quad (15)$$

When the switching frequency (f_{SW}), output voltage (V_{OUT}), output inductor (L), and output capacitor (C_{OUT}) values are selected, the unity crossover frequency of approximately 1/12 the switching frequency can be targeted.

At the crossover frequency, the gain of the open-loop transfer function is unity. This yields Equation 16 for the compensation network impedance at the crossover frequency.

$$Z_{COMP}(f_{CROSS}) = \frac{2 \times \pi \times f_{CROSS} \times C_{OUT}}{g_m \times G_{CS}} \times \frac{V_{OUT}}{V_{REF}} \quad (16)$$

To ensure that there is sufficient phase margin at the crossover frequency, set the compensator zero to 1/8 of the crossover frequency, as indicated in Equation 17.

$$f_{ZERO} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} \approx \frac{f_{CROSS}}{8} \quad (17)$$

Solving Equation 16 and Equation 17 yields the values for the compensation resistor and the compensation capacitor, as shown in Equation 18 and Equation 19.

$$R_{COMP} = 0.9 \times \left(\frac{(2\pi) f_{CROSS}}{g_m G_{CS}} \right) \times \left(\frac{C_{OUT} V_{OUT}}{V_{REF}} \right) \quad (18)$$

$$C_{COMP} = \frac{1}{2 \times \pi \times f_{ZERO} \times R_{COMP}} \quad (19)$$

Capacitor C_{C2} (as shown in Figure 69) forms a pole with the compensation resistor, R_{COMP}, in the feedback loop to ensure that the loop gain continues to decrease, or roll off, well beyond the unity-gain crossover frequency. The value of C_{C2}, if used, is typically set to 1/40 of the compensation capacitor, C_{COMP}.

DESIGN EXAMPLE

The external component selection procedure from the Control Loop Compensation section is used for this design example.

Table 9. 2-Channel, Step-Down DC-to-DC Converter Requirements

Parameter	Specification	Additional Requirements
Input Voltage, V_{IN}	5.0 V ±10%	None
Output Voltage for Channel 1, V_{OUT1}	2.5 V, 3 A, 1% V_{OUT} p-p ripple	Maximum load step: 1.5 A to 3 A, 5% droop maximum
Output Voltage for Channel 2, V_{OUT2}	1.2 V, 3 A, 1% V_{OUT} p-p ripple	Maximum load step: 1.5 A to 3 A, 5% droop maximum
Pulse Skip Feature	Enabled	None

CHANNEL 1 CONFIGURATION AND COMPONENTS SELECTION

Complete the following steps to configure Channel 1:

1. For a target output voltage (V_{OUT}) of 2.5 V, connect the V1SET pin through a 27 kΩ resistor to GND (see Table 4). Because one of the fixed output voltage options is chosen, the feedback pin (FB1) must be connected directly to the output of Channel 1, V_{OUT1}.
2. Estimate the duty cycle (D) range. Ideally,

$$D = \frac{V_{OUT}}{V_{IN}} \quad (20)$$

Therefore, for an output voltage of 2.5 V and a nominal input voltage (V_{IN}) of 5.0 V, the nominal duty cycle (D_{NOM}) is 0.5. Using the maximum input voltage (10% greater than the nominal, or 5.5 V) results in the minimum duty cycle (D_{MIN}) of 0.45, whereas using the minimum input voltage (10% less than the nominal, or 4.5 V) results in the maximum duty cycle (D_{MAX}) of 0.56.

However, the actual duty cycle will be larger than the calculated values to compensate for the power losses in the converter. Therefore, add 5% to 7% to the value calculated for the maximum load.

Based on the estimated duty cycle range, choose the switching frequency (f_{SW}) according to the minimum and maximum duty cycle limitations, as shown in Figure 64.

If the input voltage (V_{IN}) is 5 V and the output voltage (V_{OUT}) is 2.5 V for Channel 1, choose a switching frequency of 600 kHz with a maximum duty cycle of 0.8. This frequency option provides the smallest sized solution. If a higher efficiency is required, choose the 300 kHz option. However, the actual PCB footprint area of the converter will be larger because of the bigger inductor and output capacitors.

3. Select the inductor by using the following equation:

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

In this equation, V_{IN} = 5 V, V_{OUT} = 2.5 V, $\Delta I_L = 0.3 \times I_L$ = 0.9 A, and f_{SW} = 600 kHz, which results in L = 2.32 µH.

Therefore, when L = 3.3 µH (the closest minimum standard value from Table 8) in Equation 5, ΔI_L = 0.63 A.

Although the maximum output current required is 3 A, the maximum peak current is 4.5 A for the current-limit condition (see Table 7). Therefore, the inductor should be rated for a peak current of 4.5 A and an average current of 3 A for reliable circuit operation.

4. Select the output capacitor by using the following equations:

$$C_{OUT\_MIN} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (\Delta V_{RIPPLE} - \Delta I_L \times ESR)}$$

$$C_{OUT\_MIN} \cong \Delta I_{OUT\_STEP} \times \left(\frac{3}{f_{SW} \times \Delta V_{DROOP}} \right)$$

The first equation is based on the output ripple (ΔV_{RIPPLE}), whereas the second equation is based on the transient load performance requirements that allow, in this case, 5% maximum deviation. As previously mentioned, perform these calculations and then choose a capacitor based on the larger calculated capacitor size.

In this case, the following values are used:

ΔI_L = 0.63 A
f_{SW} = 600 kHz
ΔV_{RIPPLE} = 25 mV (1% of 2.5 V)
ESR = 3 mΩ (typical for ceramic capacitors)
ΔI_{OUT_STEP} = 1.5 A
ΔV_{DROOP} = 0.125 V (5% of 2.5 V)

Therefore, the output ripple based calculation dictates that C_{OUT} = 6.2 µF, whereas the transient load based calculation dictates that C_{OUT} = 60 µF. To meet both requirements, use the larger capacitor value. As previously mentioned in the Output Capacitor Selection section, the capacitance value decreases when dc bias is applied; therefore, select a higher value. In this case, the next higher value is 69 µF (a 47 µF capacitor in parallel with 22 µF) with a minimum voltage rating of 6.3 V.

5. Calculate the compensation component values of the feedback loop by using the following equation:

$$R_{COMP} = 0.9 \times \left(\frac{(2\pi) f_{CROSS}}{g_m G_{CS}} \right) \times \left(\frac{C_{OUT} V_{OUT}}{V_{REF}} \right)$$

where:
g_m = 550 µS.
G_{CS} = 4 A/V.
V_{REF} = 0.6 V.
V_{OUT} = 2.5 V.
C_{OUT} = 0.8 × 69 µF (capacitance derated by 20% to account for dc bias).

Therefore, from Equation 18,

R_{COMP} = 30 kΩ.

Substituting R_{COMP} in Equation 19 yields C_{COMP} = 820 pF.

Table 10. Channel 1 Circuit Settings

Circuit Parameter	Setting	Value
Output Voltage, V_{OUT}	See Step 1	2.5 V
Reference Voltage, V_{REF}	Fixed, typical	0.6 V
Error Amplifier Transconductance, g_m	Fixed, typical	550 µS
Current-Sense Gain, G_{CS}	Fixed, typical	4 A/V
Switching Frequency, f_{SW}	See Step 2	600 kHz
Crossover Frequency, f_{CROSS}	1/12 f_{SW}	50 kHz
Zero Frequency, f_{ZERO}	1/8 f_{CROSS}	6.25 kHz
Output Inductor, L_{OUT}	See Step 3	3.3 µH
Output Capacitor, C_{OUT}	See Step 4	(47 + 22) µF
Compensation Resistor, R_{COMP}	See Equation 18	30 kΩ
Compensation Capacitor, C_{COMP}	See Equation 19	820 pF

CHANNEL 2 CONFIGURATION AND COMPONENTS SELECTION

Complete the following steps to configure Channel 2:

1. For a target output voltage (V_{OUT}) of 1.2 V, connect the V2SET pin through a 4.7 kΩ resistor to GND (see Table 4). Because one of the fixed output voltage options is chosen, the feedback pin (FB2) must be directly connected to the output of Channel 2, V_{OUT2}.
2. Estimate the duty cycle (D) range. Ideally,

$$D = \frac{V_{OUT}}{V_{IN}}$$

Therefore, for an output voltage of 1.2 V and a nominal input voltage (V_{IN}) of 5.0 V, the nominal duty cycle (D_{NOM}) is 0.24. Using the maximum input voltage (10% greater than the nominal, or 5.5 V) results in the minimum duty cycle (D_{MIN}) of 0.22, whereas using the minimum input voltage (10% less than the nominal, or 4.5 V) results in the maximum duty cycle (D_{MAX}) of 0.27.

However, the actual duty cycle will be larger than the calculated values to compensate for the power losses in the converter. Therefore, add 5% to 7% to the value calculated for the maximum load.

The switching frequency (f_{SW}) of 600 kHz, which is chosen based on the Channel 1 requirements, meets the duty cycle ranges that were previously calculated. Therefore, this switching frequency is acceptable.

3. Select the inductor by using the following equation:

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

In this equation, V_{IN} = 5 V, V_{OUT} = 1.2 V, $\Delta I_L = 0.3 \times I_L$ = 0.9 A, and f_{SW} = 600 kHz, which results in L = 1.67 µH.

Therefore, when L = 2.2 µH (the closest standard value) in Equation 5, ΔI_L = 0.69 A.

Although the maximum output current required is 3 A, the maximum peak current is 4.5 A for the current-limit condition (see Table 7). Therefore, the inductor should be rated for a peak current of 4.5 A and an average current of 3 A for reliable circuit operation in all conditions.

4. Select the output capacitor by using the following equations:

$$C_{OUT\_MIN} \cong \frac{\Delta I_L}{8 \times f_{SW} \times (\Delta V_{RIPPLE} - \Delta I_L \times ESR)}$$

$$C_{OUT\_MIN} \cong \Delta I_{OUT\_STEP} \times \left(\frac{3}{f_{SW} \times \Delta V_{DROOP}} \right)$$

The first equation is based on the output ripple (ΔV_{RIPPLE}), whereas the second equation is based on the transient load performance requirements that allow, in this case, 5% maximum deviation. As previously mentioned, perform these calculations and then choose a capacitor based on the larger calculated capacitor size.

In this case, the following values are used:

ΔI_L = 0.69 A
f_{SW} = 600 kHz
ΔV_{RIPPLE} = 12 mV (1% of 1.2 V)
ESR = 3 mΩ (typical for ceramic capacitors)
ΔI_{OUT_STEP} = 1.5 A
ΔV_{DROOP} = 0.06 V (5% of 1.2 V)

The output ripple based calculation dictates that C_{OUT} = 20 µF, whereas the transient load based calculation dictates that C_{OUT} = 125 µF. To meet both requirements, use the latter to choose a capacitor. As previously mentioned in the Output Capacitor Selection section, the capacitance value decreases when dc bias is applied; therefore, select a higher value. In this case, choose a 47 µF, 6.3 V capacitor and a 100 µF, 6.3 V capacitor in parallel to meet the requirements.

5. Calculate the compensation component values of the feedback loop by using the following equation:

$$R_{COMP} = 0.9 \times \left(\frac{(2\pi) f_{CROSS}}{g_m G_{CS}} \right) \times \left(\frac{C_{OUT} V_{OUT}}{V_{REF}} \right)$$

where:
g_m = 550 µS.
G_{CS} = 4 A/V.
V_{REF} = 0.6 V.
V_{OUT} = 1.2 V.
C_{OUT} = 0.8 × (47 + 100) µF (capacitance derated by 20% to account for dc bias).

From Equation 18,

R_{COMP} = 30 kΩ.

Substituting R_{COMP} in Equation 19 yields C_{COMP} = 820 pF.

Table 11. Channel 2 Circuit Settings

Circuit Parameter	Setting	Value
Output Voltage, V_{OUT}	Nominal	1.2 V
Reference Voltage, V_{REF}	Typical	0.6 V
Error Amplifier Transconductance, g_m	Typical	550 µS
Current-Sense Gain, G_{CS}	Typical	4 A/V
Switching Frequency, f_{SW}	See Step 2	600 kHz
Crossover Frequency, f_{CROSS}	1/12 f_{SW}	50 kHz
Zero Frequency, f_{ZERO}	1/8 f_{CROSS}	6.25 kHz
Output Inductor, L_{OUT}	Step 3	2.2 µH
Output Capacitor, C_{OUT}	Step 4	(47 + 100) µF
Compensation Resistor, R_{COMP}	See Equation 18	30 kΩ
Compensation Capacitor, C_{COMP}	See Equation 19	820 pF

SYSTEM CONFIGURATION

Complete the following steps to further configure the ADP2116 for this design example:

1. Set the switching frequency (f_{SW}) to 600 kHz (see Table 5) by connecting the FREQ pin through an 8.2 kΩ resistor to GND.
2. Tie SCFG to VDD and use the CLKOUT signal to synchronize other converters on the same board with the ADP2116.
3. Tie OPCFG through an 82 kΩ resistor to GND for 3 A/3 A maximum output current operation and to enable pulse skip mode at light load conditions (see Table 7).

A schematic of the ADP2116 as configured in the design example described in the Design Example section is shown in Figure 71.

Other configurations are shown in Figure 72 to Figure 74. An application circuit of a single interleaved, dual-phase, 6 A output is shown in Figure 72. The schematic in Figure 73 depicts an application circuit with a 3A/2A dual-output load and a 300 kHz switching frequency, and the schematic of a dual-output converter that works at 1.2 MHz with an adjustable V_{OUT1} and V_{OUT2} is shown in Figure 74.

Table 12 provides the recommended inductor, output capacitor, and compensation component values for a set of popular input and output voltage combinations.

Table 12. Selection Table of L, C_{OUT}, and Compensation Values

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	Maximum Load (A)[1]	L (µH)	C_{OUT} (µF)	R_{COMP} (kΩ)	C_{COMP} (pF)
300	5	3.3	3.0	6.8	100	30	1600
300	5	2.5	3.0	5.6	122 (22 + 100)	27	1800
300	5	1.8	3.0	4.7	147 (47 + 100)	22	2200
300	5	1.2	3.0	3.3	247 (47 + 2 × 100)	30	1600
600	5	3.3	3.0	3.3	47	33	750
600	5	2.5	3.0	3.3	69 (22 + 47)	30	820
600	5	1.8	3.0	2.2	100	30	820
600	5	1.2	3.0	2.2	147 (47 + 100)	30	820
600	5	1.2	6.0	2 × 2.2	294 (2 × 47 + 2 × 100)	15	1600
1200	5	2.5	3.0	1.0	47	33	390
1200	5	1.8	3.0	1.0	57 (10 + 47)	33	390
1200	5	1.2	3.0	1.0	69 (22 + 47)	27	470
1200	5	1.2	6.0	2 × 1.0	141 (3 × 47)	13	910
1200	5	0.8	3.0	1.0	122 (22 + 100)	33	390

[1] A maximum load of 6.0 A is available only with the single interleaved, dual-phase, 6 A output configuration (see Figure 72).

APPLICATION CIRCUITS

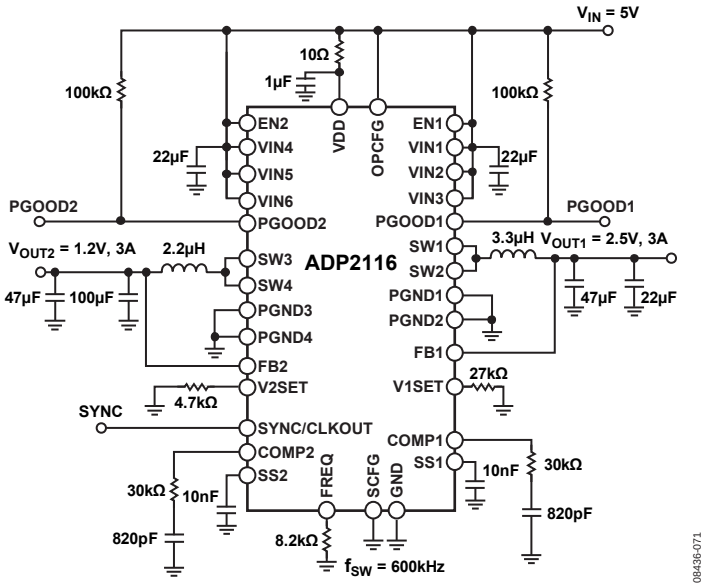


Figure 71. Application Circuit for 3 A/3 A Outputs

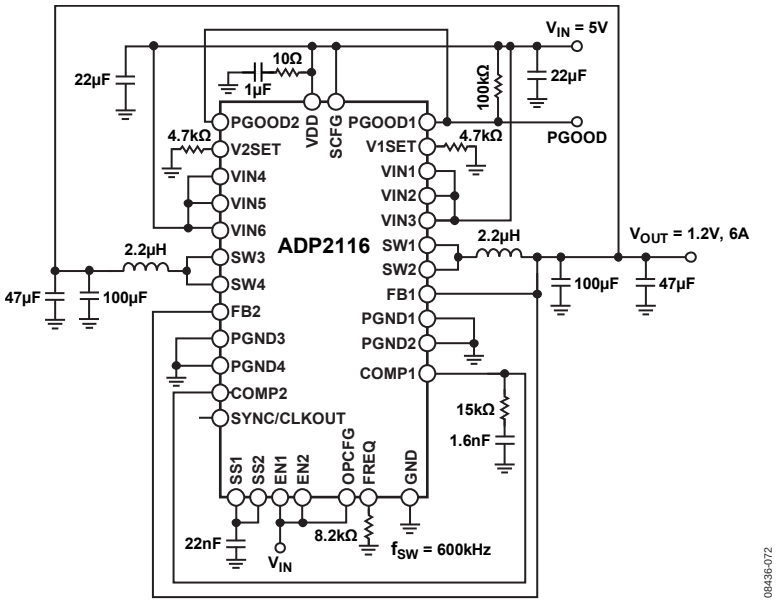


Figure 72. Application Circuit for a Single 6 A Output

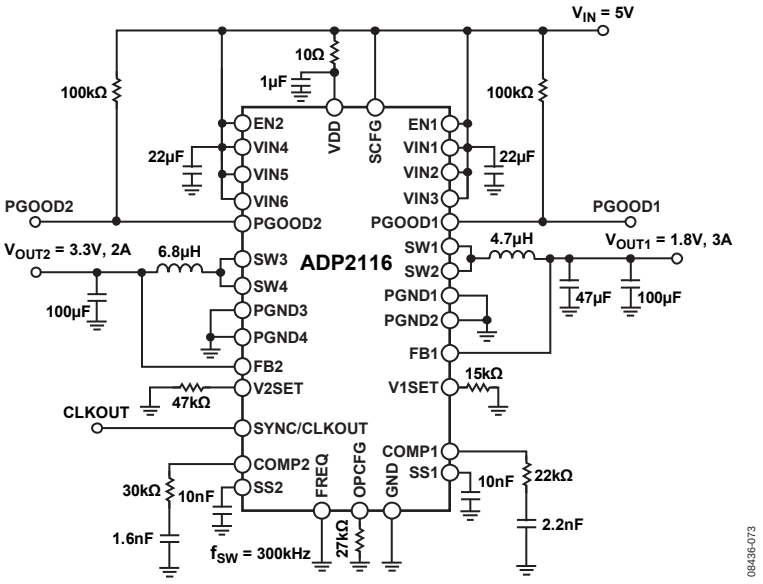


Figure 73. Application Circuit for 3 A/2 A Outputs

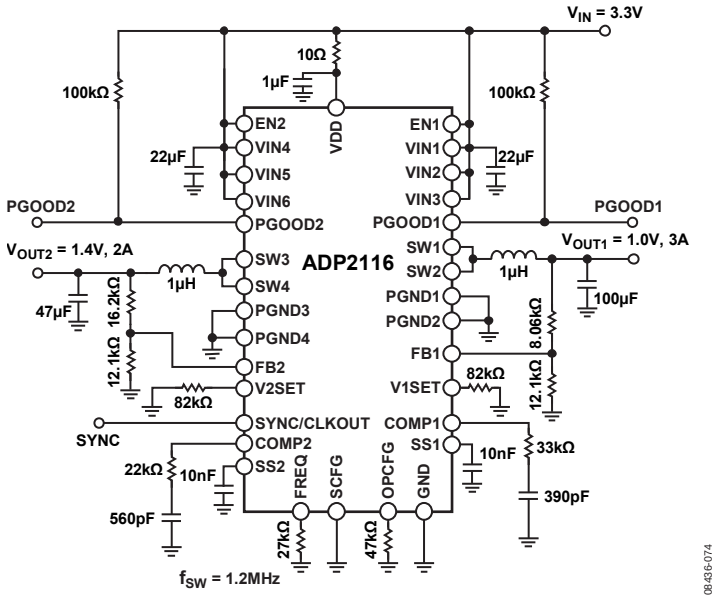


Figure 74. Application Circuit for Adjustable Outputs

POWER DISSIPATION AND THERMAL CONSIDERATIONS

Power dissipated by the ADP2116 dual switching regulator is a major factor that affects the efficiency of the two dc-to-dc converters. The efficiency is given by

$$Efficiency = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (21)$$

where:
P_{IN} is the input power.
P_{OUT} is the output power.

The difference between the input power and the output power is the power loss given by

$$P_{LOSS} = P_{IN} - P_{OUT}$$

The power loss of the step-down dc-to-dc converter is approximated by

$$P_{LOSS} = P_D + P_L \quad (22)$$

where:
P_D is the power dissipation on the ADP2116.
P_L is the inductor power losses.

The inductor losses are estimated (without core losses) by

$$P_L \cong I_{OUT}^2 \times DCR_L \quad (23)$$

where:
I_{OUT} is the dc load current.
DCR_L is the inductor series resistance.

The ADP2116 power dissipation, P_D, includes the power switch conductive losses, the switch losses, and the transition losses of each channel.

The power switch conductive losses are due to the output current (I_{OUT}) flowing through the P-channel MOSFET and the N-channel MOSFET power switches that have internal resistance (R_{DSON}). The amount of conductive power loss can be calculated by

$$P_{COND} = [R_{DSON-P} \times D + R_{DSON-N} \times (1 - D)] \times I_{OUT}^2 \quad (24)$$

where:
D is the duty cycle, determined by $D = V_{OUT}/V_{IN}$.
R_{DSON-P} is the internal resistance of the P-channel MOSFET.
R_{DSON-N} is the internal resistance of the N-channel MOSFET.

Switching losses are associated with the current drawn by the driver to turn the power of the devices on and off at the switching frequency. The amount of switching power loss is given by

$$P_{SW} = (C_{GATE-P} + C_{GATE-N}) \times V_{IN}^2 \times f_{SW} \quad (25)$$

where:
C_{GATE-P} is the P-channel MOSFET gate capacitance.
C_{GATE-N} is the N-channel MOSFET gate capacitance.

Transition losses occur because the P-channel power MOSFET cannot be turned on or off instantaneously. The amount of transition loss is calculated by

$$P_{TRAN} = V_{IN} \times I_{OUT} \times (t_{RISE} + t_{FALL}) \times f_{SW} \quad (26)$$

where t_{RISE} and t_{FALL} are the rise time and the fall time of the switching node. In the ADP2116, the rise and fall times of the switching node are in the order of 5 ns.

The power dissipated by the regulator increases the die junction temperature, T_J, above the ambient temperature, T_A.

$$T_J = T_A + T_R \quad (27)$$

where the temperature rise, T_R, is proportional to the power dissipation in the package, P_D.

The proportionality coefficient is defined as the thermal resistance from the junction of the die to the ambient temperature.

$$T_R = \theta_{JA} \times P_D \quad (28)$$

where θ_{JA} is the junction ambient thermal resistance (34°C/W for the JEDEC 1S2P board; see Table 2).

When designing an application for a particular ambient temperature range, calculate the expected ADP2116 power dissipation (P_D) due to conductive, switching, and transition losses of both channels by using Equation 24, Equation 25, and Equation 26, and estimate the temperature rise by using Equation 27 and Equation 28. The reliable operation of the two converters can be achieved only if the estimated die junction temperature of the ADP2116 (Equation 27) is less than 125°C. Therefore, at higher ambient temperatures, reduce the power dissipation of the system. Figure 75 shows the power derating for elevated ambient temperatures at various airflow conditions. The area below the curves is the safe operation area for the ADP2116 dual regulators.

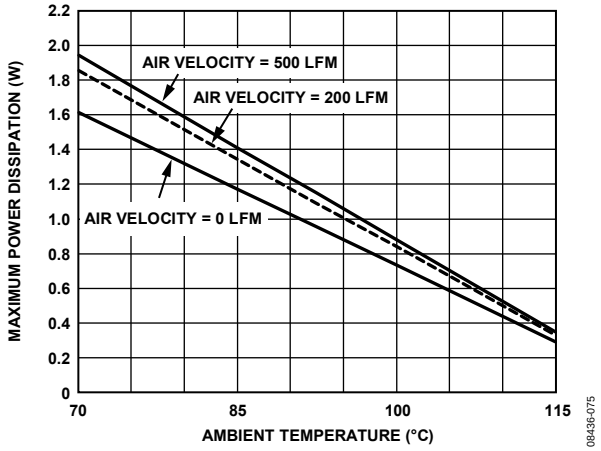


Figure 75. Power Dissipation Derating (JEDEC 1S2P Board)

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential for obtaining the best performance from each channel of the ADP2116. Poor circuit layout degrades the output ripple and regulation, as well as the EMI and electromagnetic compatibility performance. For optimum layout, refer to the following guidelines:

- Use separate analog and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, to analog ground. In addition, connect the ground references of power components, such as input and output capacitors, to power ground. Connect both ground planes to the exposed pad of the ADP2116.
- Place the input capacitor of each channel as close to the VINx pins as possible and connect the other end to the closest power ground plane.
- For low noise and better transient performance, a filter is recommended between VINx and VDD. Place a 1 µF, 10 Ω low-pass input filter between the VDD pin and the VINx pins, as close to the GND pin as possible.
- Ensure that the high current loop traces are as short and as wide as possible. Make the high current path from C_{IN} through the L, the C_{OUT}, and the power ground plane back to C_{IN} as short as possible. To accomplish this, ensure that the input and output capacitors share a common power ground plane. In addition, ensure that the high current path from the PGNDx pin through L and C_{OUT} back to the power ground plane is as short as possible by tying the PGNDx pins of the ADP2116 to the PGND plane as close as possible to the input and output capacitors (see Figure 76).
- Connect the ADP2116 exposed pad to a large copper plane to maximize its power dissipation capability. Thermal conductivity can be obtained using the method described in JEDEC Standard JESD51-7.
- Place the feedback resistor divider network as close as possible to the FBx pin to prevent noise pickup. Try to minimize the length of the trace that connects the top of the feedback resistor divider to the output while keeping the trace away from the high current traces and the switching node to avoid noise pickup. To further reduce noise pickup, place an analog ground plane on either side of the FBx trace and ensure that the trace is as short as possible to reduce the parasitic capacitance pickup.

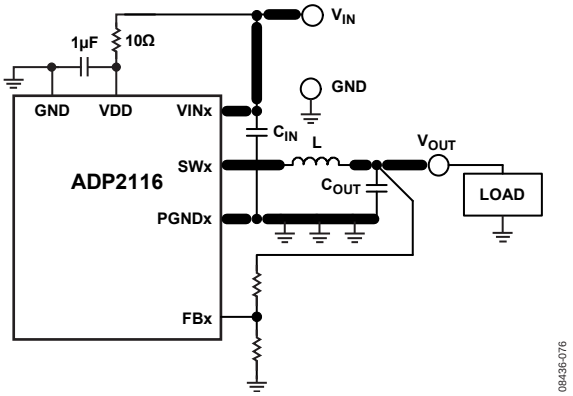


Figure 76. High Current Traces in the PCB Circuit

OUTLINE DIMENSIONS

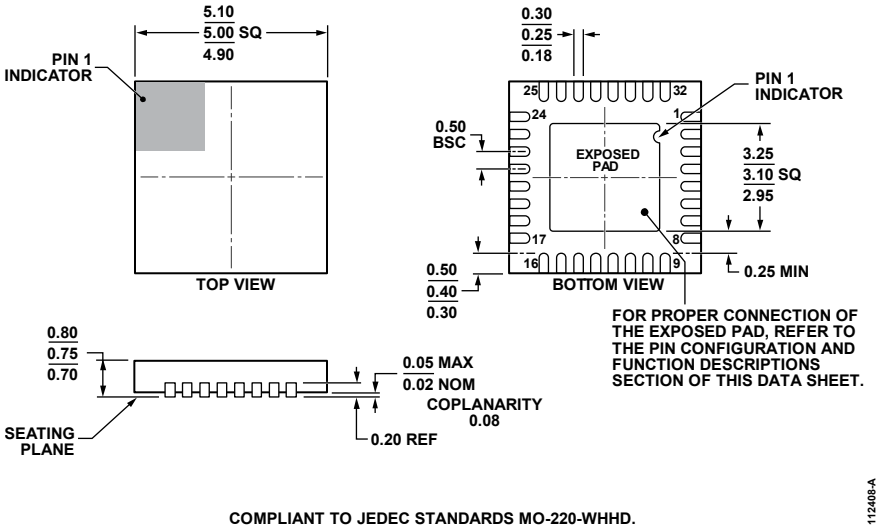


Figure 77. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option	Ordering Quantity
ADP2116ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-7	1,500
ADP2116-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] Operating junction temperature is −40°C to +125°C.

D08436-0-3/16(B)