

TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91C219

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

****CAUTION****

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0 to INT4), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficulty. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontroller

TMP91C219F

1. Outline and Features

TMP91C219 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment. With 2 Kbytes of boot ROM included, it allows your programs to be erased and rewritten on board. TMP91C219F comes in a 100-pin flat package. Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)

- Instruction mnemonics are upward compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4 channels (444 ns/2 bytes at 36 MHz)

(2) Minimum instruction execution time: 111 ns (at 36 MHz)

(3) Built-in RAM: 2 Kbytes

Built-in ROM: None

Built-in Boot ROM: 2 Kbytes

RESTRICTIONS ON PRODUCT USE

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

- (4) External memory expansion
 - Expandable up to 16 Mbytes (Shared program/data area)
 - Can simultaneously support 8- or 16-bit width external data bus
 - ... Dynamic data bus sizing
- (5) 8-bit timer: 6 channels
- (6) 16-bit timer/event counter: 1 channel
- (7) Serial bus interface: 1 channel
- (8) 10-bit AD converter: 4 channels
- (9) Watchdog timer
- (10) Chip select/wait controller: 4 blocks
- (11) Interrupts: 33 interrupts
 - 9 CPU interrupts: Software interrupt instruction and illegal instruction
 - 17 internal interrupts: 7 priority levels are selectable.
 - 7 external interrupts: 7 priority levels are selectable.
 - (Level mode, rising edge mode and falling edge mode are selectable.)
- (12) Input/output ports: 53 pins
- (13) Standby function
 - Three HALT modes: IDLE2 (Programmable), IDLE1, STOP
- (14) Operating voltage
 - $V_{CC} (5\text{ V}) = 4.75\text{ V to }5.25\text{ V}$ ($f_c \text{ max} = 36\text{ MHz}$)
 - $V_{CC} (3\text{ V}) = 3.0\text{ V to }3.6\text{ V}$ ($f_c \text{ max} = 36\text{ MHz}$)
- (15) Package: 100-pin QFP (P-LQFP100-1414-0.50F)

Power on and power off of the supply

Power on and power off of the supply require the simultaneous execution of the 5 V power supply and 3.3 V power supply. If the both power supplies cannot be turned on or off simultaneously, turn on or off each power supply within the specifications shown in Figure 3.1.2 in 3.1.2 "Power On and Power Off of the Supply". When power on and power off of the supply is performed on either of them, overlap current may run into the internal logic. Leaving overlap current running results in increase of power dissipation and short LSI life.

Please avoid leaving either of power supplies on.

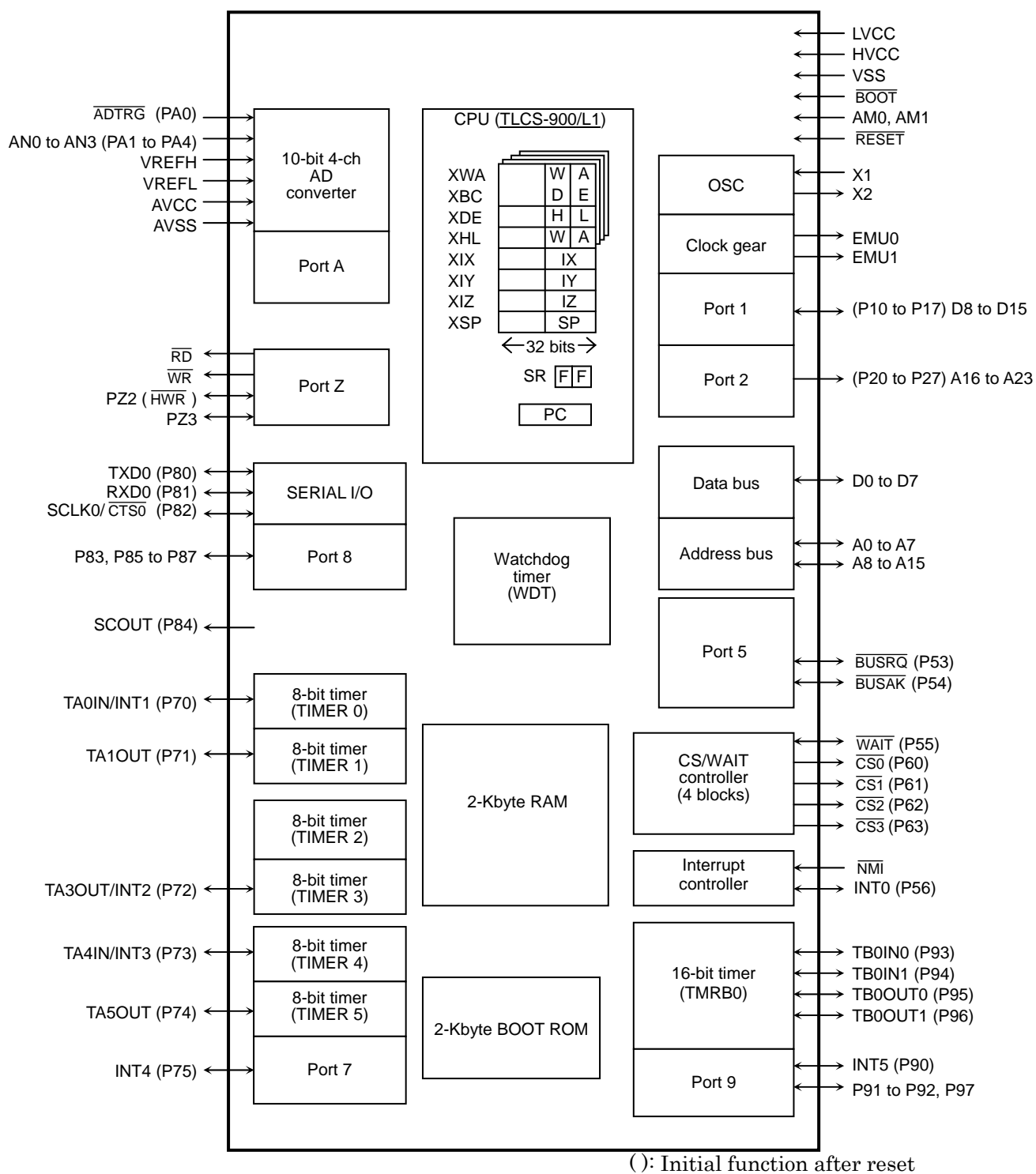


Figure 1.1 TMP91C219 Block Diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91C219, their names and functions are as follows.

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91C219F.

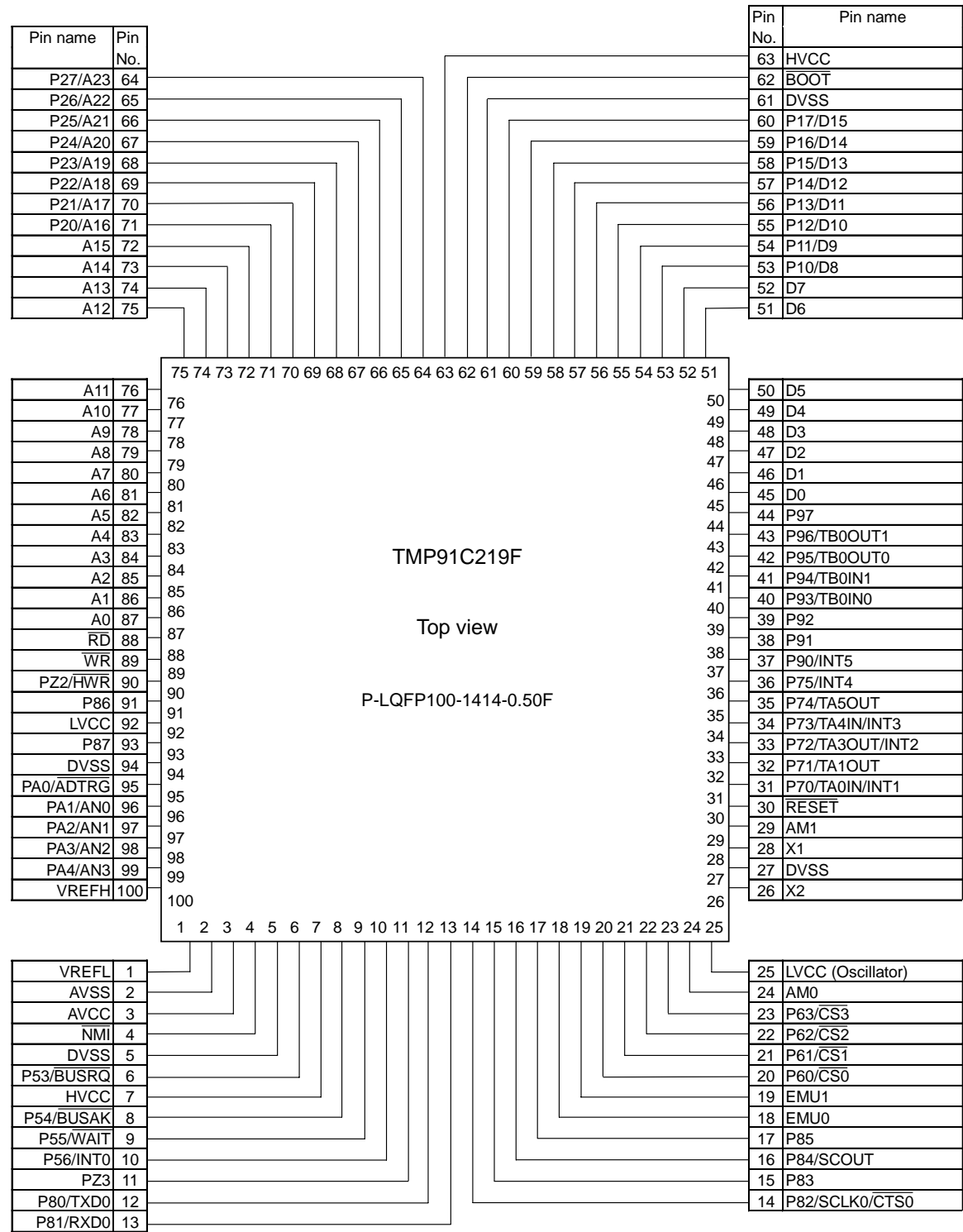


Figure 2.1.1 Pin Assignment Diagram (100-pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.

Table 2.2.1 Pin Names and Functions

Pin Name	Number of Pins	I/O	Functions
D0 to D7	8	I/O	Data (Lower): Bits 0 to 7 of data bus
P10 to P17	8	I/O	Port 1: I/O port that allows I/O to be selected at the bit level (when used to the external 8-bit bus)
D8 to D15		I/O	Data (Upper): Bits 8 to 15 of data bus
P20 to P27	8	Output	Port 2: Output port
A16 to A23		Output	Address: Bits 16 to 23 of address bus
A8 to A15	8	Output	Address: Bits 8 to 15 of address bus
A0 to A7	8	Output	Address: Bits 0 to 7 of address bus
\overline{RD}	1	Output	Read: Strobe signal for reading external memory
\overline{WR}	1	Output	Write: Strobe signal for writing data to pins D0 to D7
PZ2	1	I/O	Port Z2: I/O port (with pull-up resistor)
\overline{HWR}		Output	High write: Strobe signal for writing data to pins D8 to D15
PZ3	1	I/O	Port Z3: I/O port (with pull-up resistor)
P53	1	I/O	Port 53: I/O port (with pull-up resistor)
\overline{BUSRQ}		Input	Bus request: Signal used to request bus release (High impedance)
P54	1	I/O	Port 54: I/O port (with pull-up resistor)
\overline{BUSAK}		Output	Bus acknowledge: Signal used to acknowledge bus release (High impedance)
P55	1	I/O	Port 55: I/O port (with pull-up resistor)
\overline{WAIT}		Input	Wait: Pin used to request CPU bus wait.
P56	1	I/O	Port 56: I/O port (with pull-up resistor)
INT0		Input	Interrupt request pin0: Interrupt request pin with programmable level/rising edge/falling edge
P60	1	Output	Port 60: Output port
$\overline{CS0}$		Output	Chip select 0: Outputs 0 when address is within specified address area.
P61	1	Output	Port 61: Output port
$\overline{CS1}$		Output	Chip select 1: Outputs 0 when address is within specified address area
P62	1	Output	Port 62: Output port
$\overline{CS2}$		Output	Chip select 2: Outputs 0 when address is within specified address area
P63	1	Output	Port 63: Output port
$\overline{CS3}$		Output	Chip select 3: Outputs 0 when address is within specified address area
P70	1	I/O	Port 70: I/O port
TA0IN		Input	Timer A0 input
INT1		Input	Interrupt request pin2: Interrupt request pin with programmable level/rising edge/falling edge
P71	1	I/O	Port 71: I/O port
TA1OUT		Output	Timer A0 or timer A1 output
P72	1	I/O	Port 72: I/O port
TA3OUT		Output	Timer A2 or timer A3 output:
INT2		Input	Interrupt request pin2: Interrupt request pin with programmable level/rising edge/falling edge
P73	1	I/O	Port 73: I/O port
TA4IN		Input	Timer A4 input
INT3		Input	Interrupt request pin3: Interrupt request pin with programmable level/rising edge/falling edge
P74	1	I/O	Port 74: I/O port
TA5OUT		Output	Timer A4 or timer A5 output
P75	1	I/O	Port 75: I/O port
INT4		Input	Interrupt request pin4 : Interrupt request pin with programmable

Pin Name	Number of Pins	I/O	Functions
P80 TXD0	1	I/O Output	Port 80: I/O port (with pull-up resistor) level/rising edge/falling edge Serial send data 0: Programmable open drain output pin
P81 RXD0	1	I/O Input	Port 81: I/O port (with pull-up resistor) Serial receive data 0
P82 SCLK0 $\overline{\text{CTS0}}$	1	I/O I/O Input	Port 82: I/O port: (with pull-up resistor) Serial clock I/O 0 Serial data send enable 0 (Clear to send)
P83	1	I/O	Port 83: I/O port (with pull-up resistor)
P84 SCOUT	1	I/O Output	Port 84: I/O port (with pull-up resistor) System clock output : f_{FPH}
P85 to P87	3	I/O	Port 85 to 87: I/O port (with pull-up resistor)
P90 INT5	1	I/O Input	Port 90: I/O port Interrupt request pin 5: Interrupt request pin with programmable level/rising edge/falling edge
P91 to P92	1	I/O	Port 91 to 92: I/O port
P93 TB0IN0	1	I/O Input	Port 93: I/O port Timer B0 input 0
P94 TB0IN1	1	I/O Input	Port 94: I/O port Timer B0 input 1
P95 TB0OUT0	1	I/O Output	Port 95: I/O port Timer B0 output 0
P96 TB0OUT1	1	I/O Output	Port 96: I/O port Timer B0 output 1
P97	1	I/O	Port 97: I/O port
PA0 $\overline{\text{ADTRG}}$	1	Input Input	Port A0: Pin used to input port AD trigger: Signal used to request AD start
PA1 to PA4 AN0 to AN3	4	Input input	Port A1 to A4: Pins used to input ports Analog input 0 to 3: Pins used to input to AD converter
$\overline{\text{BOOT}}$	1	Input	This pin sets boot mode (with pull-up resistor)
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge level or with both edge levels programmable
AM0 to AM1	2	Input	Address mode : External data bus with select pin when external 16-bit bus is fixed or external 8-/16-bit buses are mixed, AM1 = 0 , AM0 = 1 when external 8-bit bus is fixed, AM1 = 0 , AM0 = 0
EMU0	1	Output	Open pin
EMU1	1	Output	Open pin
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP91C219F. (with pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1	I/O	Power supply pin for AD converter
AVSS	1		GND supply pin for AD converter (0V)
X1 X2	2	Input Output	Oscillator connection pins
HVCC	2		Power supply pins (5 V) (All HVCC pins should be connected with the power supply pin (5 V).)
LVCC	2		Power supply pins (3 V) (All LVCC pins should be connected with the power supply pin (3 V).)
DVSS	4		GND pins (0 V)

Note1: An external DMA controller cannot access the device's built-in memory or built-in I/O devices using the $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ signal.

Note2: All pins which have a built-in pull-up resistor (Other than the $\overline{\text{RESET}}$ pin and the $\overline{\text{BOOT}}$ pin) can be disconnected from the resistor in software.

3. Operation

This section describes the basic components, functions and operation of the TMP91C219.

Notes and restrictions which apply to the various items described here are outlined in section 7 “Points to Note and Restrictions” at the end of this databook.

3.1 CPU

The TMP91C219 incorporates a high-performance 16-bit CPU (The 900/L1 CPU). For a description of this CPU's operation, please refer to the section of this databook which describes the TLCS-900/L1 CPU.

The following subsections describe functions peculiar to the CPU used in the TMP91C219; these functions are not covered in the section devoted to the TLCS-900/L1 CPU.

3.1.1 Reset

When resetting the TMP91C219 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then set the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks (8.89 μs at 36 MHz). Thus, when turn on the switch, be set to the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{\text{RESET}}$ input to low level at least for 10 system clocks.

Clock gear is initialized 1/16 mode by reset operation. It means that the system clock mode f_{SYS} is set to $f_c/32$ ($= f_c/16 \times 1/2$).

When the reset is accept, the CPU:

- Sets the program counter (PC) as follows in accordance with the reset vector stored at address FFFF00H to FFFF02H:
 $\text{PC}<0:7> \leftarrow \text{Data in location FFFF00H}$
 $\text{PC}<8:15> \leftarrow \text{Data in location FFFF01H}$
 $\text{PC}<16:23> \leftarrow \text{Data in location FFFF02H}$
- Sets the stack pointer (XSP) to 100H.
- Sets bits <IFF0:2> of the status register (SR) to 111 (Thereby setting the interrupt level mask register to level 7).
- Sets the <MAX> bit of the status register to 1 (MAX mode).
 (Note: As this product does not support MIN mode, do not write a 0 to the <MAX> bit.)
- Clears bits <RFP0:2> of the status register to 000 (Thereby selecting register bank 0).

When the reset is cleared, the CPU starts executing instructions according to the program counter settings. CPU internal registers not mentioned above do not change when the reset is cleared.

When the reset is accepted, the CPU sets internal I/O, ports and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to general-purpose input or output port mode.

Note: The CPU internal register (except to PC, SR, XSP) and internal RAM data do not change by resetting.

Figure 3.1.1 shows the timing of a reset for the TMP91C219.

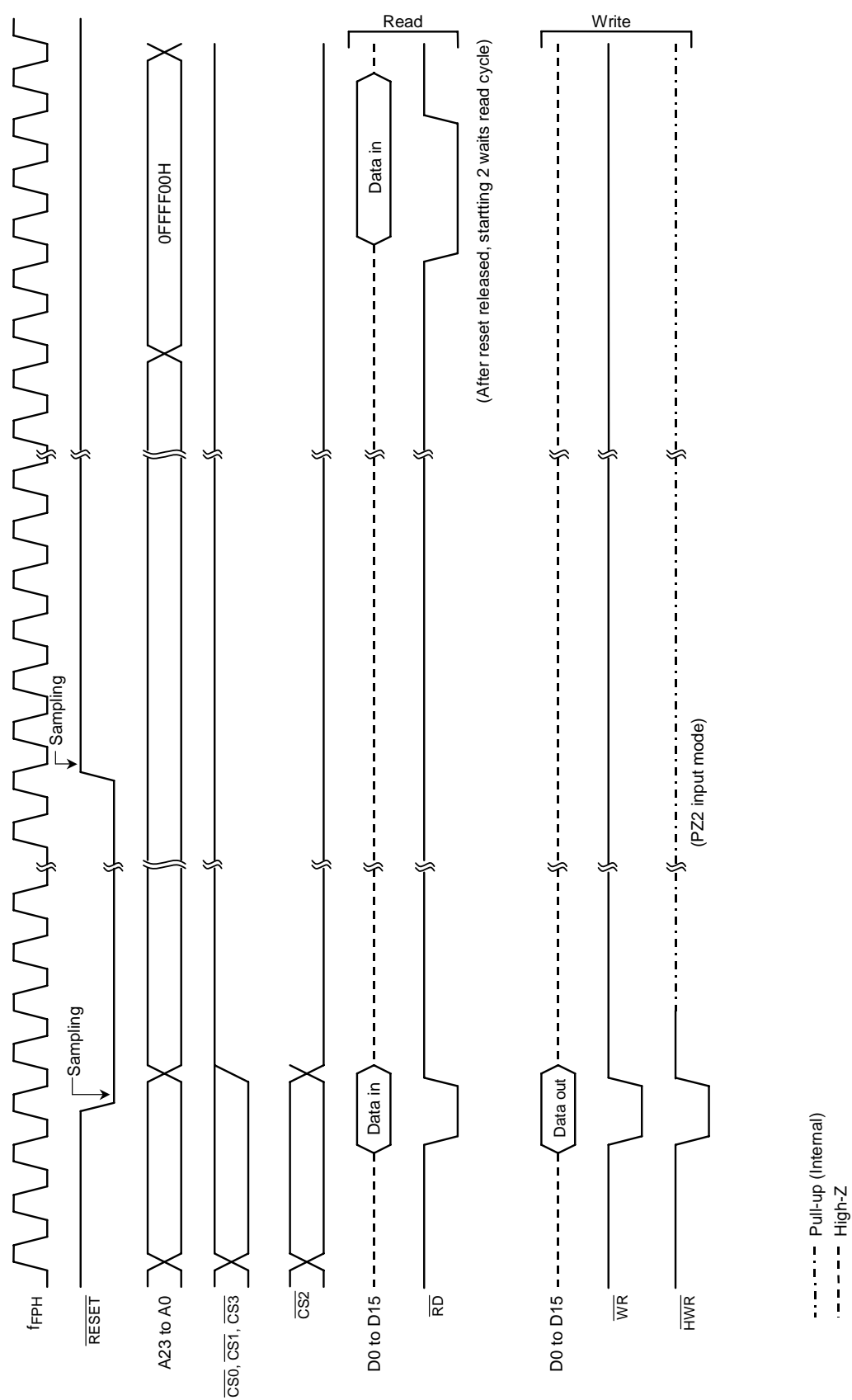


Figure 3.1.1 TMP91C219 Reset Timing Example

3.1.2 Power On and Power Off of the Supply

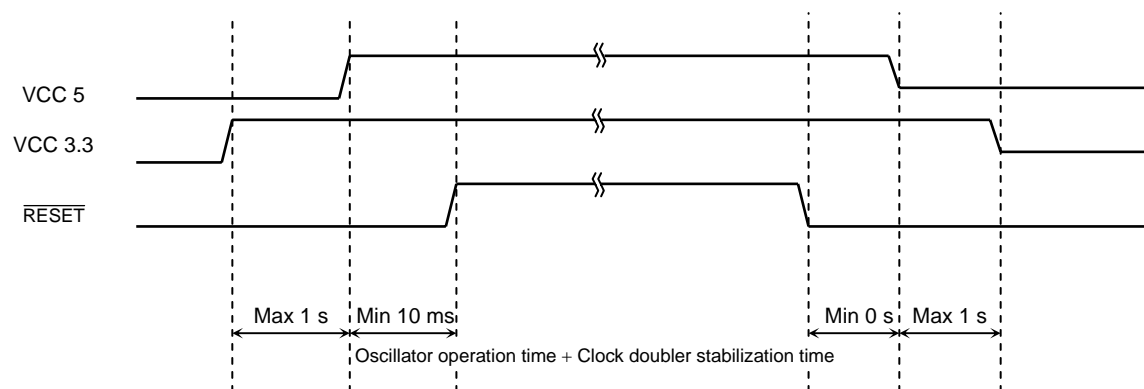



Figure 3.1.2 Power Supply On/Off Timing

3.2 Outline of Operation Modes

There are multi-chip and multi-boot modes. Which mode is selected depends on the device's pin state after a reset.

- Multi-chip mode: The device normally operations in this mode. After a reset, the device starts executing the external memory program.
- Multi-boot mode: This mode is used to rewrite the external flash memory by serial transfer (UART) or ATAPI transfer.
After a reset, internal boot program starts up, executing an on-board rewrite program.

Table 3.2.1 Operation Mode Setup Table

Operation Mode	Mode Setup Input Pin	
	RESET	BOOT
Multi-chip mode		H
Multi-boot mode		L

3.3 Memory Map

Figure 3.3.1 is a memory map of the TMP91C219.

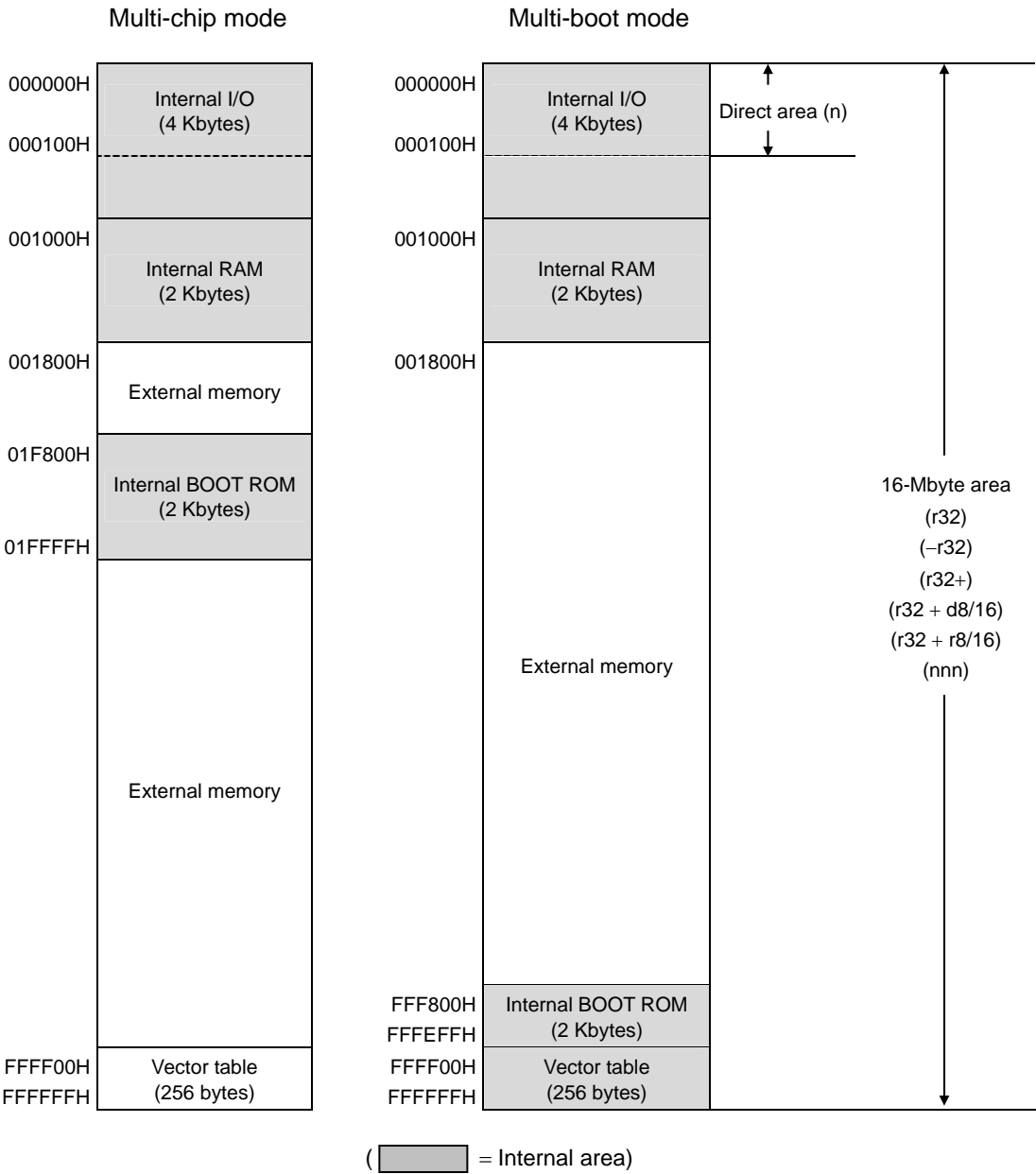


Figure 3.3.1 TMP91C219 Memory Map

4. Electrical Characteristics

4.1 Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage (5 V)	HVcc	−0.5 to 5.75	V
Power supply voltage (3 V)	LVcc	−0.5 to 4.0	
Input voltage	VIN	−0.5 to Vcc + 0.5	
Output current (Per pin)	IOL	2	mA
Output current (Per pin)	IOH	−2	
Output current (Total)	ΣIOL	80	
Output current (Total)	ΣIOH	−80	
Power dissipation (Ta = 85°C)	PD	600	mW
Soldering temperature (10 s)	TSOLDER	260	°C
Storage temperature	TSTG	−65 to 150	
Operating temperature	TOPR	−20 to 70	

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note)	Max	Unit		
Power supply voltage (5V) (AVcc = HVcc) (AVss = DVss = 0 V)		HVCC	fc = 10 to 36 MHz	4.75		5.25	V		
Power supply voltage (3V)		LVCC	fc = 10 to 36 MHz	3.0		3.6	V		
Input low voltage	D0 to D7, P10 to P17 (D8 to D15)	HV _{IL}		−0.3		0.8	V		
	The other ports	V _{IL1}				0.3 HVcc			
	RESET , NMI	V _{IL2}				0.25 HVcc			
	P56 (INT0), P70 (INT1) P72 (INT2), P73 (INT3) P75 (INT4), P90 (INT5)								
	AM0, 1		V _{IL3}					0.3	
	X1		V _{IL4}					0.2 LVcc	
	Input high voltage	D0 to D7, P10 to P17 (D8 to D15)	V _{IH}			2.2			HVcc + 0.3
The other ports		V _{IH1}		0.7 HVcc					
RESET , NMI		V _{IH2}		0.75 HVcc					
P56 (INT0), P70 (INT1) P72 (INT2), P73 (INT3) P75 (INT4), P90 (INT5)									
AM0, 1			V _{IH3}					HVcc − 0.3	
X1			V _{IH4}					0.8 LVcc	
Output low voltage		V _{OL}	IOL = 1.6 mA			0.45		V	
Output high voltage		V _{OH}	IOH = − 400 μA	4.2					

Note: Typical values are for when Ta = 25 °C and HVcc = 5.0 V, LVcc = 3.3 V unless otherwise noted.

DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note)	Max	Unit
Input leakage current	ILI	$0.0 \leq V_{IN} \leq HV_{CC}$		0.02	± 5	μA
Output leakage current	ILO	$0.2 \leq V_{IN} \leq HV_{CC} - 0.2$		0.05	± 10	
Power down voltage (at STOP, RAM backup)	VSTOP	$V_{IL2} = 0.2 HV_{CC}$, $V_{IH2} = 0.8 HV_{CC}$	2.0		3.6	V
RESET pull-up resistor	RRST	$HV_{CC} = 5 V \pm 5\%$	40		200	$k\Omega$
Pin capacitance	CIO	$F_c = 1 \text{ MHz}$			10	pF
Schmitt width RESET, NMI, INT0 to INT5	VTH		0.4	1.0		V
Programmable pull-up resistor	RKH	$HV_{CC} = 5 V \pm 5\%$	40		200	$k\Omega$
NORMAL (Note 2)	Icc	$HV_{CC} = 5 V \pm 5\%$ $LV_{CC} = 3.0 \text{ to } 3.6 V$ $f_c = 36 \text{ MHz}$			40	mA
IDLE2					20	
IDLE1					14	
STOP		$HV_{CC} = 5 V \pm 5\%$ $LV_{CC} = 3.0 \text{ to } 3.6 V$ $T_a \leq 70^\circ C$			100	μA

Note 1: Typical values are for when $T_a = 25^\circ C$ and $HV_{CC} = 5.0 V$, $LV_{CC} = 3.3 V$ unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL):

All functions are operational; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) $HV_{CC} = 5.0\text{ V} \pm 5\%$, $LV_{CC} = 3.0\text{ to }3.6\text{ V}$

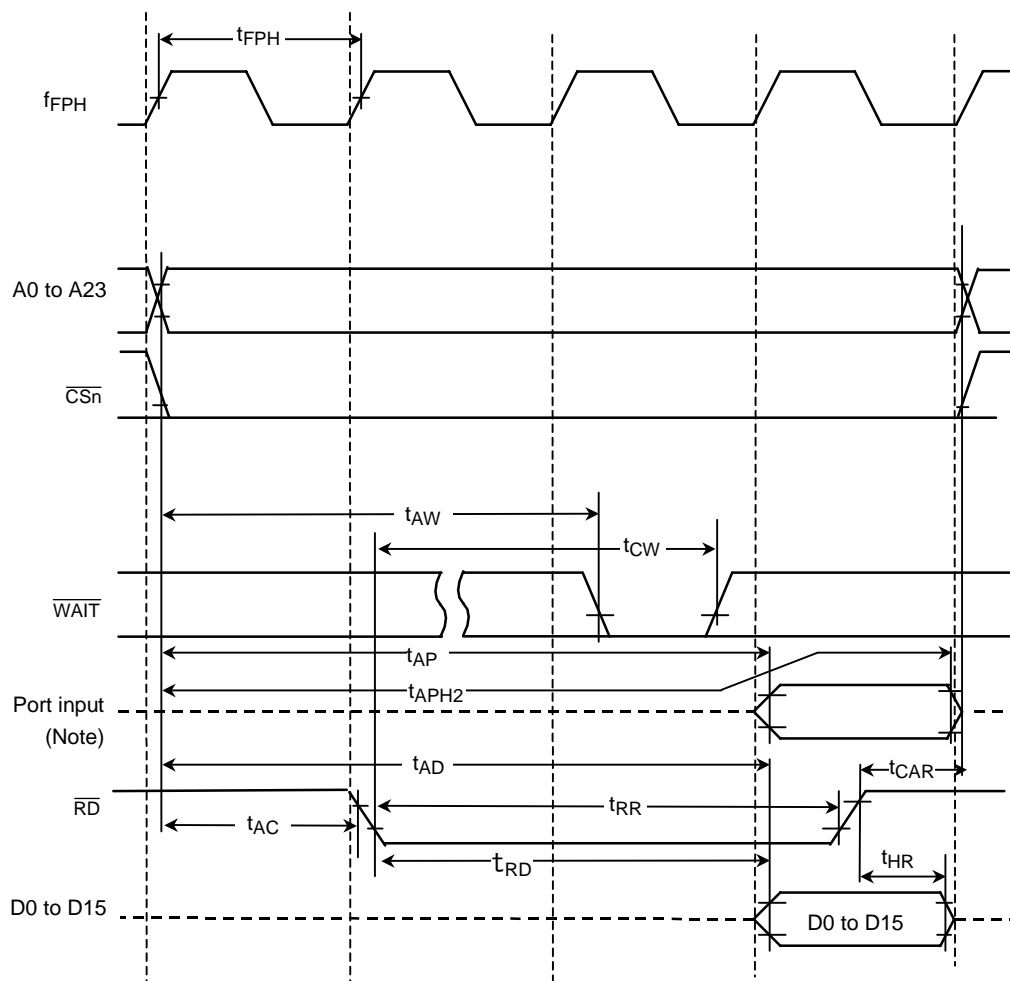
No.	Parameter	Symbol	Variable		$f_{FPH} = 36\text{ MHz}$		Unit
			Min	Max	Min	Max	
1	f_{FPH} period (= x)	t_{FPH}	27.6	100	27.6		ns
2	A0 to 23 valid $\rightarrow \overline{RD} / \overline{WR}$ fall	t_{AC}	$x - 26$		1.6		ns
3	\overline{RD} rise \rightarrow A0 to A23 hold	t_{CAR}	$0.5x - 13.8$		0.0		ns
4	\overline{WR} rise \rightarrow A0 to A23 hold	t_{CAW}	$x - 13$		14.6		ns
5	A0 to A23 valid \rightarrow D0 to D15 input	t_{AD}		$3.5x - 40$		56.6	ns
6	\overline{RD} fall \rightarrow D0 to D15 input	t_{RD}		$2.5x - 34$		35.0	ns
7	\overline{RD} low width	t_{RR}	$2.5x - 25$		44.0		ns
8	\overline{RD} rise \rightarrow D0 to D15 hold	t_{HR}	0		0		ns
9	\overline{WR} low width	t_{WW}	$2.0x - 25$		30.2		ns
10	D0 to D15 valid $\rightarrow \overline{WR}$ rise	t_{DW}	$1.5x - 35$		26.4		ns
11	\overline{WR} rise \rightarrow D0 to D15 hold (1+ N) waits	t_{WD}	$x - 25$		2.6		ns
12	A0 to A23 valid $\rightarrow \overline{WAIT}$ input (1+ N) waits	t_{AW}		$3.5x - 60$		36.6	ns
13	$\overline{RD} / \overline{WR}$ fall $\rightarrow \overline{WAIT}$ hold	t_{CW}	$2.5x + 0$		69.0		ns
14	A0 to A23 valid \rightarrow PORT input	t_{APH}		$3.5x - 76$		20.6	ns
15	A0 to A23 valid \rightarrow PORT hold	t_{APH2}	$3.5x$		96.6		ns
16	A0 to A23 valid \rightarrow PORT valid	t_{APO}		$3.5x + 60$		156.6	ns

AC measuring conditions

- Output level : High = 2.2 V, Low = 0.8 V_{CC}, CL = 50 pF
- Input level : High = 2.4 V, Low = 0.45 V (D0 to D15)
: High 0.8 V_{CC} / Low 0.2 V_{CC} (except D0 to D15)

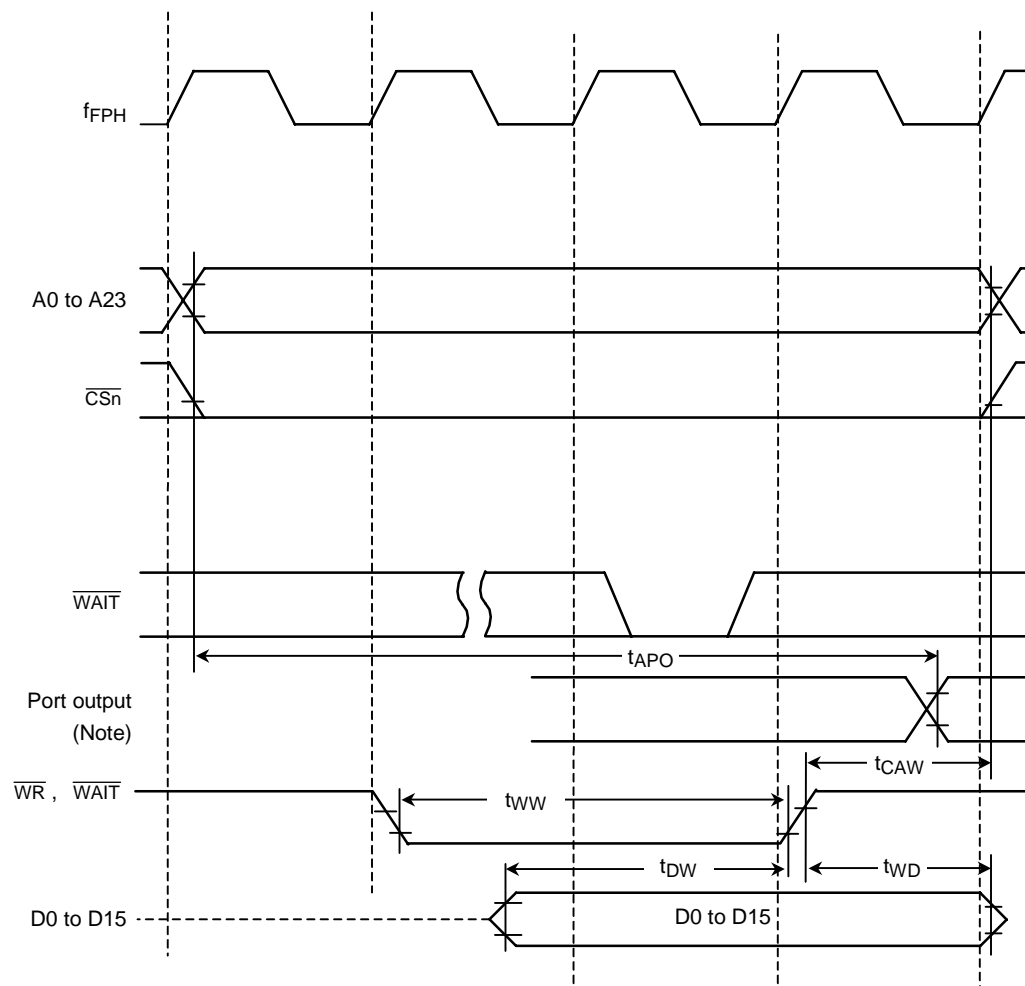
Note: Symbol "x" in the above table means the period of clock " f_{FPH} ", it's half period of the system clock " f_{SYS} " for CPU core. The period of f_{FPH} depends on the clock gear setting.

(2) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as \overline{RD} and \overline{CS} are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(3) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as \overline{WR} and \overline{CS} are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics

AVCC = HVCC, AVSS = VSS

Parameter	Symbol	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH	$HV_{CC} - 0.2\text{ V}$	HV_{CC}	HV_{CC}	V
Analog reference voltage (-)	VREFL	DV_{SS}	DV_{SS}	$DV_{SS} + 0.2\text{ V}$	
Analog input voltage range	VAIN	V_{REFL}		V_{REFH}	
Analog current for analog reference voltage <VREFON> = 1	IREF (VREFL = 0V)		0.85	1.20	mA
<VREFON> = 0			0.02	5.0	μA
Error (Not including quantizing errors)	—		± 1.0	± 4.0	LSB

Note 1: $1\text{ LSB} = (V_{REFH} - V_{REFL})/1024\text{ [V]}$

Note 2: The value for Icc includes the current which flows through the AVCC pin.

4.5 Serial Channel Timing (I/O Internal Mode)

Note: Symbol “x” in the above table means the period of clock “ f_{FPH} ”, it's half period of the system clock “ f_{SYS} ” for CPU core. The period of f_{FPH} depends on the clock gear setting.

(1) SCLK input mode

Parameter	Symbol	Variable		36 MHz (Note)		Unit
		Min	Max	Min	Max	
SCLK period	t_{SCY}	16X		0.44		μs
Output data → SCLK rising/falling edge*	t_{OSS}	$t_{SCY}/2 - 4X - 85$		25		ns
SCLK rising/falling edge* → Output data hold	t_{OHS}	$t_{SCY}/2 + 2X + 0$		276		ns
SCLK rising/falling edge* → Input data hold	t_{HSR}	$3X + 10$		92		ns
SCLK rising/falling edge* → Valid data input	t_{SRD}		$t_{SCY} - 0$		440	ns
Valid data input → SCLK rising/falling edge*	t_{RDS}	0		0		ns

*) SCLK rising/falling edge: The rising edge is used in SCLK rising mode.
The falling edge is used in SCLK falling mode.

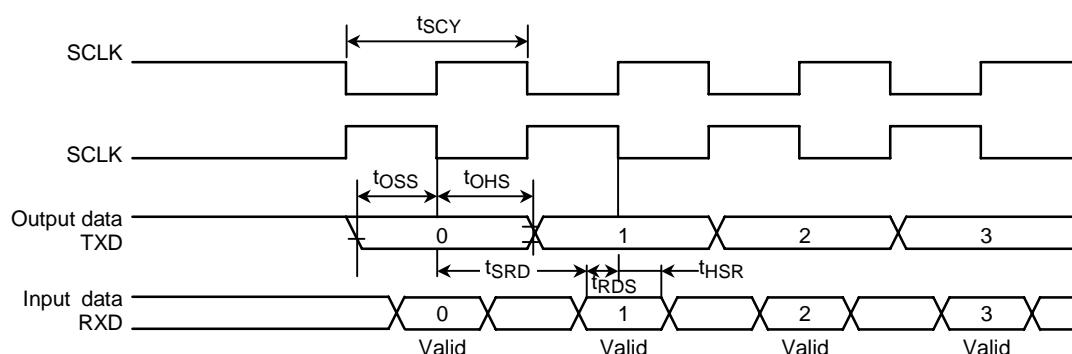
Note: at $t_{SCY} = 16X$

(2) SCLK output mode

Parameter	Symbol	Variable		36 MHz (Note)		Unit
		Min	Max	Min	Max	
SCLK period (programmable)	t_{SCY}	16X	8192X	0.44		μs
Output data → SCLK rising/falling edge*	t_{OSS}	$t_{SCY}/2 - 40$		180		ns
SCLK rising/falling edge* → Output data hold	t_{OHS}	$t_{SCY}/2 - 40$		180		ns
SCLK rising/falling edge* → Input data hold	t_{HSR}	0		0		ns
SCLK rising/falling edge* → Valid data input	t_{SRD}		$t_{SCY}/2 - 1X - 90$		324	ns
Valid data input → SCLK rising/falling edge*	t_{RDS}	$1X + 90$		117		ns

*) SCLK rising/falling edge: The rising edge is used in SCLK rising mode.
The falling edge is used in SCLK falling mode.

Note: at $t_{SCY} = 16X$



4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Parameter	Symbol	Variable		36 MHz		Unit
		Min	Max	Min	Max	
Clock period	t_{VCK}	$8X + 100$		320		ns
Clock low level width	t_{VCKL}	$4X + 40$		150		ns
Clock high level width	t_{VCKH}	$4X + 40$		150		ns

Note: Symbol “x” in the above table means the period of clock “ f_{FPH} ”, it’s half period of the system clock “ f_{SYS} ” for CPU core. The period of f_{FPH} depends on the clock gear setting .

4.7 Interrupts

(1) \overline{NMI} , INT0 to INT5 Interrupts

Parameter	Symbol	Variable		36 MHz		Unit
		Min	Max	Min	Max	
\overline{NMI} , INT0 to INT5 low level width	t_{INTAL}	$4X + 40$		150		ns
\overline{NMI} , INT0 to INT5 high level width	t_{INTAH}	$4X + 40$		150		ns

Note: Symbol “x” in the above table means the period of clock “ f_{FPH} ”, it’s half period of the system clock “ f_{SYS} ” for CPU core. The period of f_{FPH} depends on the clock gear setting .

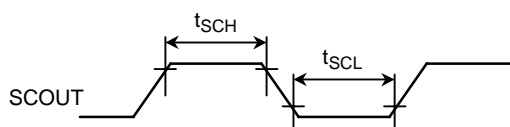
4.8 SCOUT Pin AC Characteristics

Parameter	Symbol	Variable		36 MHz		Condition	Unit
		Min	Max	Min	Max		
Low level width	t_{SCH}	$0.5T - 10$		3.8		$V_{CC} = 5V \pm 5\%$	ns
High level width	t_{SCL}	$0.5T - 10$		3.8		$V_{CC} = 5V \pm 5\%$	ns

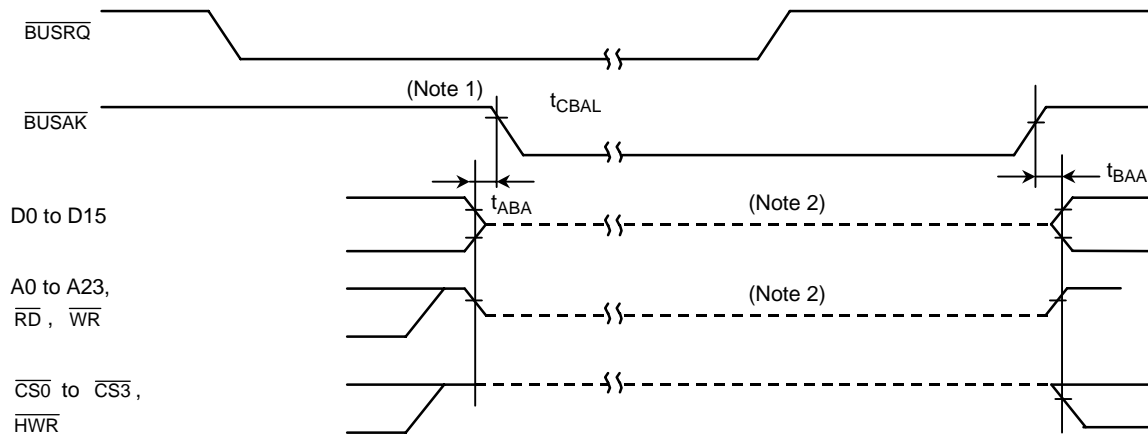
T: Period of SCOUT

Measurement conditions

- Output level: High 0.7 V_{CC} /Low 0.3 V_{CC} , $C_L = 10pF$



4.9 Bus Request/Bus Acknowledge



Parameter	Symbol	Variable		$f_{\text{FPH}} = 36 \text{ MHz}$		Unit
		Min	Max	Min	Max	
Output buffer to $\overline{\text{BUSAK}}$ low	t_{ABA}	0	80	0	80	ns
$\overline{\text{BUSAK}}$ high to output buffer on	t_{BAA}	0	80	0	80	ns

Note 1: Even if the $\overline{\text{BUSRQ}}$ signal goes low, the bus will not be released while the $\overline{\text{WAIT}}$ signal is low. The bus will only be released when $\overline{\text{BUSRQ}}$ goes low while $\overline{\text{WAIT}}$ is high.

Note 2: This line shows only that the output buffer is in the off state.

It does not indicate that the signal level is fixed.

Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary since fixing of the level is delayed.

The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.