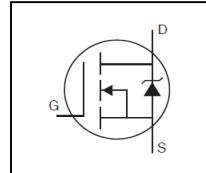
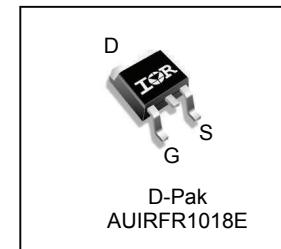


Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *



HEXFET® Power MOSFET		
V_{DSS}		60V
$R_{DS(on)}$	typ.	7.1mΩ
	max.	8.4mΩ
I_D (Silicon Limited)		79A①
I_D (Package Limited)		56A


Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFR1018E	D-Pak	Tube	75	AUIRFR1018E
		Tape and Reel Left	3000	AUIRFR1018ETRL

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	79①	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	56①	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	56	
I_{DM}	Pulsed Drain Current ②	315	
P_D @ $T_C = 25^\circ\text{C}$	Maximum Power Dissipation	110	W
	Linear Derating Factor	0.76	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ③	88	mJ
I_{AR}	Avalanche Current ②	47	A
E_{AR}	Repetitive Avalanche Energy ②	11	mJ
dv/dt	Peak Diode Recovery dv/dt ④	21	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	1.32	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑥	—	50	
$R_{\theta JA}$	Junction-to-Ambient ⑦	—	110	

HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

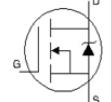
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.073	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 5\text{mA}$ ②
$R_{DS(\text{on})}$	Static Drain-to-Source On-Resistance	—	7.1	8.4	$\text{m}\Omega$	$V_{GS} = 10\text{V}, I_D = 47\text{A}$ ⑤
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 100\mu\text{A}$
g_{fs}	Forward Trans conductance	110	—	—	S	$V_{DS} = 50\text{V}, I_D = 47\text{A}$
$R_{G(\text{Int})}$	Internal Gate Resistance	—	0.73	—	Ω	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
		—	—	250		$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

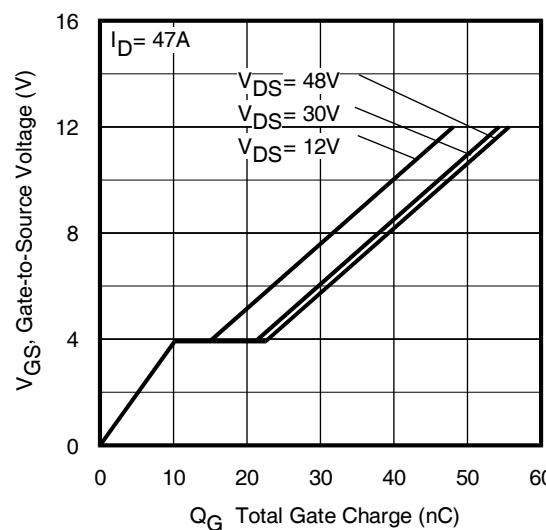
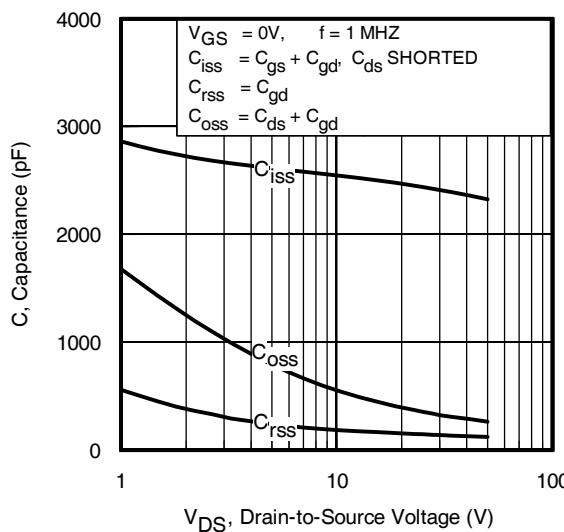
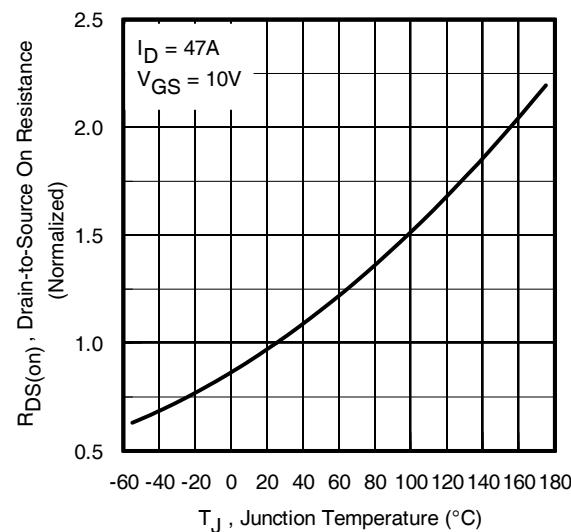
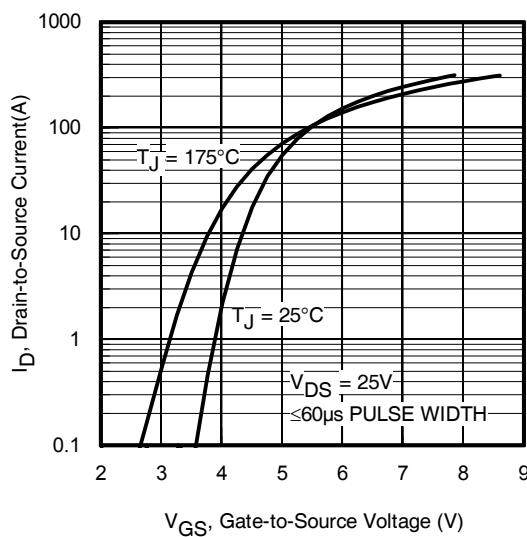
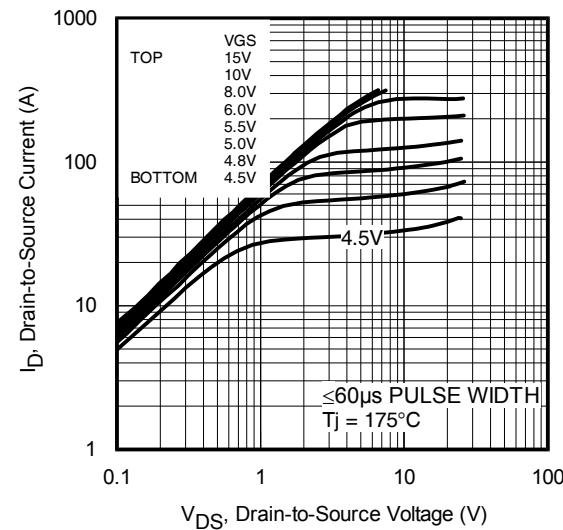
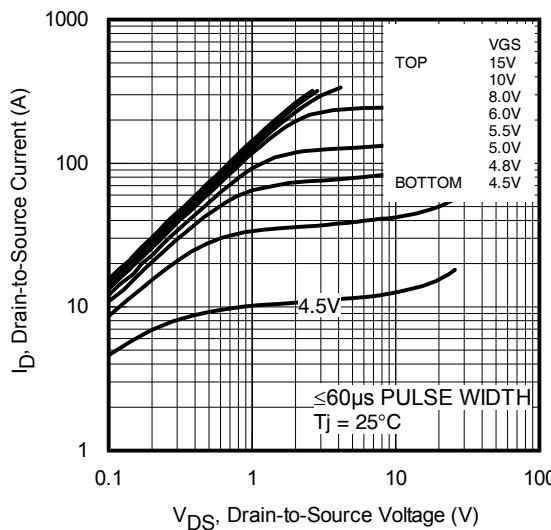
Q_g	Total Gate Charge	—	46	69	nC	$I_D = 47\text{A}$ $V_{DS} = 30\text{V}$ $V_{GS} = 10\text{V}$ ⑤
Q_{gs}	Gate-to-Source Charge	—	10	—		
Q_{qd}	Gate-to-Drain Charge	—	12	—		
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{qd}$)	—	34	—		
$t_{d(\text{on})}$	Turn-On Delay Time	—	13	—	ns	$V_{DD} = 39\text{V}$ $I_D = 47\text{A}$ $R_G = 10\Omega$ $V_{GS} = 10\text{V}$ ⑤
t_r	Rise Time	—	35	—		
$t_{d(\text{off})}$	Turn-Off Delay Time	—	55	—		
t_f	Fall Time	—	46	—		
C_{iss}	Input Capacitance	—	2290	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 50\text{V}$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	270	—		
C_{rss}	Reverse Transfer Capacitance	—	130	—		
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	390	—		$V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 48\text{V}$ ⑦
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	630	—		$V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 48\text{V}$ ⑥

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_s	Continuous Source Current (Body Diode)	—	—	79①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{sM}	Pulsed Source Current (Body Diode) ①	—	—	315		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_s = 47\text{A}, V_{GS} = 0\text{V}$ ⑤
t_{rr}	Reverse Recovery Time	—	26	39	ns	$T_J = 25^\circ\text{C}$
		—	31	47		$T_J = 125^\circ\text{C}$ $V_R = 51\text{V}$,
Q_{rr}	Reverse Recovery Charge	—	24	36	nC	$T_J = 25^\circ\text{C}$ $I_F = 47\text{A}$
		—	35	53		$T_J = 125^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ⑤
t_{on}	Forward Turn-On Time	—	1.8	—	A	$T_J = 25^\circ\text{C}$
		Intrinsic turn-on time is negligible (turn-on is dominated by L_s+L_D)				


Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by $T_{J\text{max}}$, starting $T_J = 25^\circ\text{C}$, $L = 0.08\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 47\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 47\text{A}$, $di/dt \leq 1668\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss\text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑨ R_0 is measured at T_J approximately 90°C .



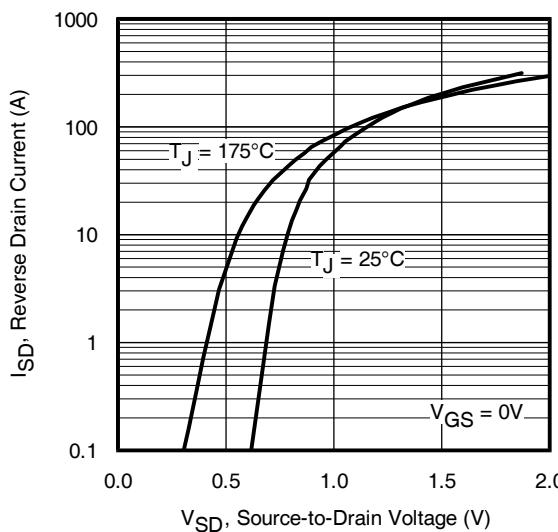


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

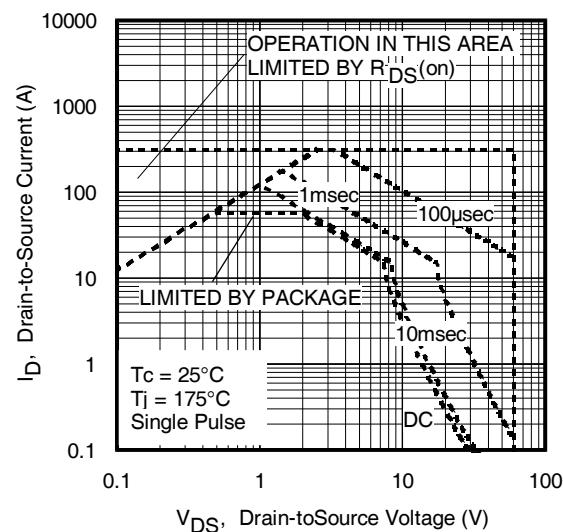


Fig 8. Maximum Safe Operating Area

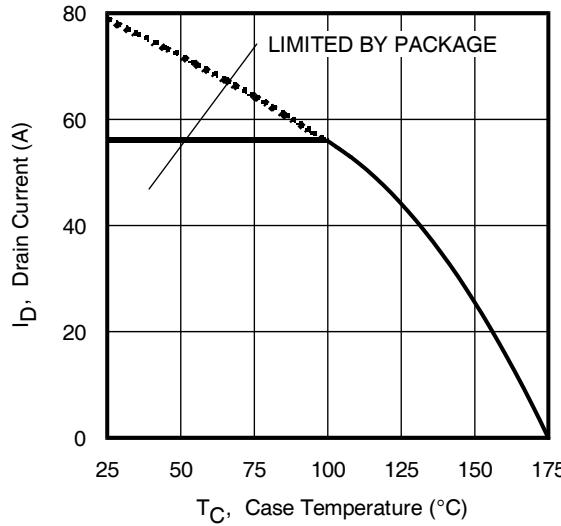


Fig. 9 Maximum Drain Current vs. Case Temperature

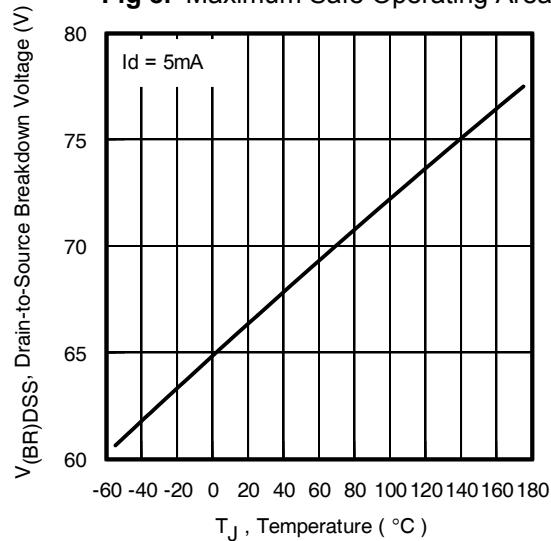


Fig 10. Drain-to-Source Breakdown Voltage

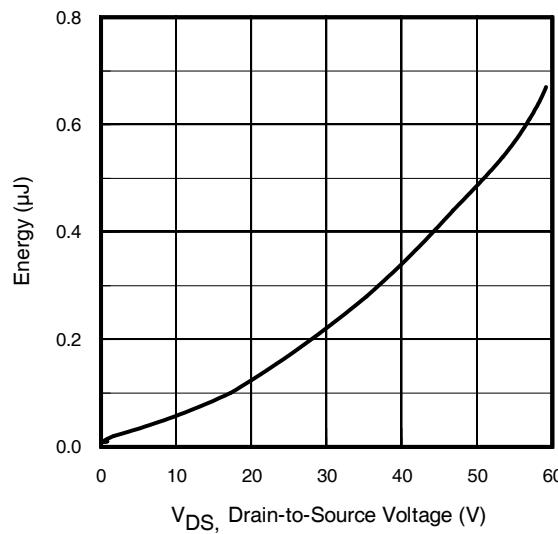


Fig. 11 Typical Coss Stored Energy

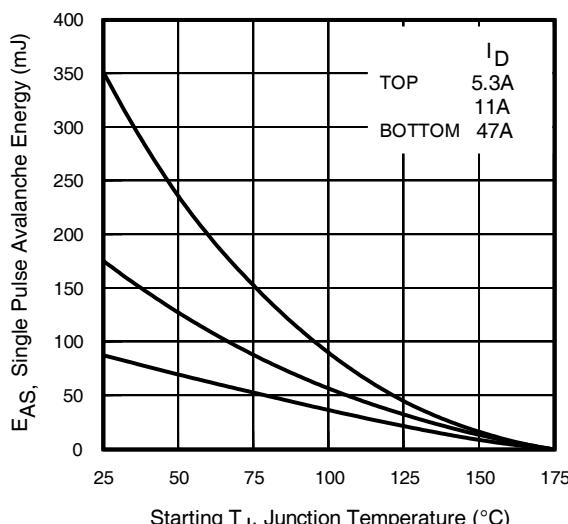


Fig 12. Maximum Avalanche Energy vs. Drain Current

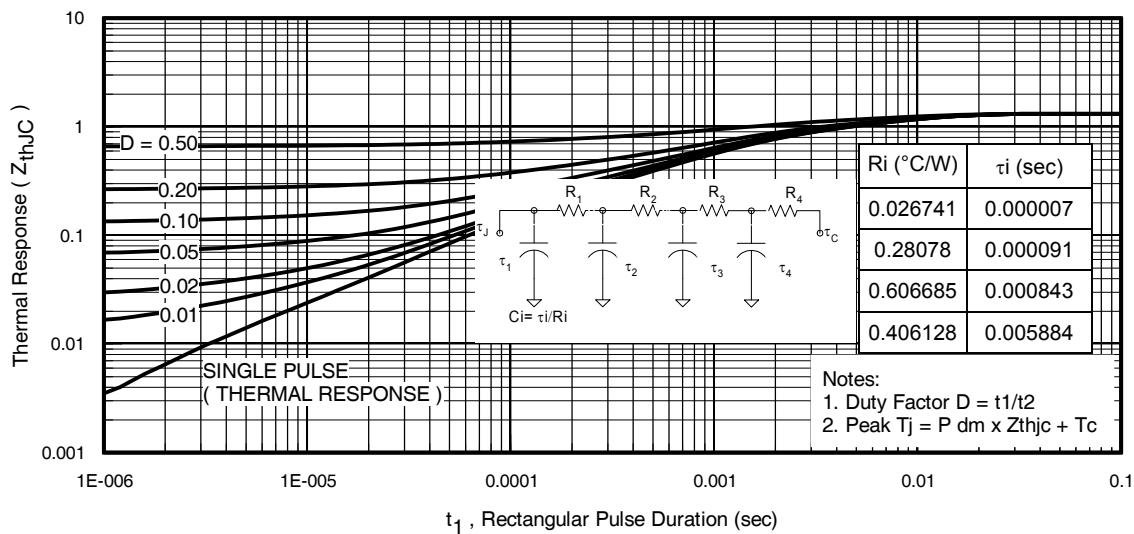


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

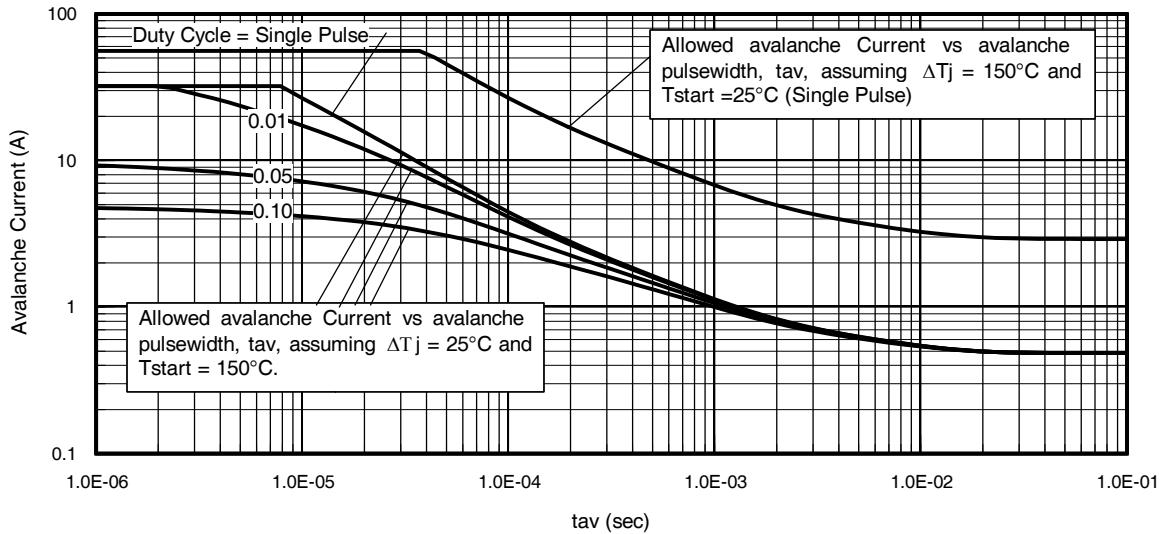


Fig 14. Typical Avalanche Current Vs. Pulse width

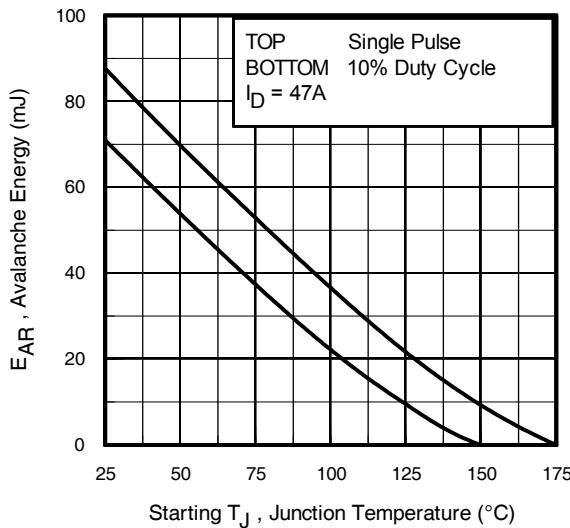


Fig 15. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as $25^{\circ}C$ in Figure 13, 14).

t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

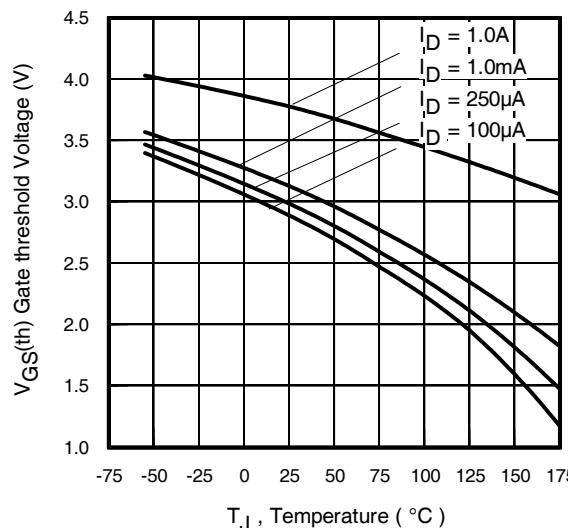


Fig. 16. Threshold Voltage vs. Temperature

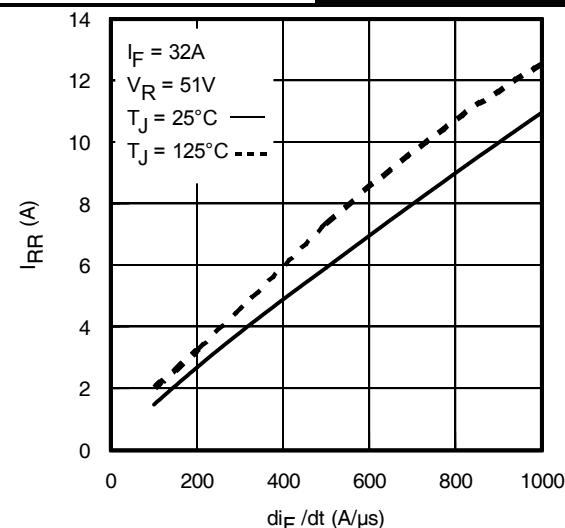


Fig. 17 - Typical Recovery Current vs. di_F/dt

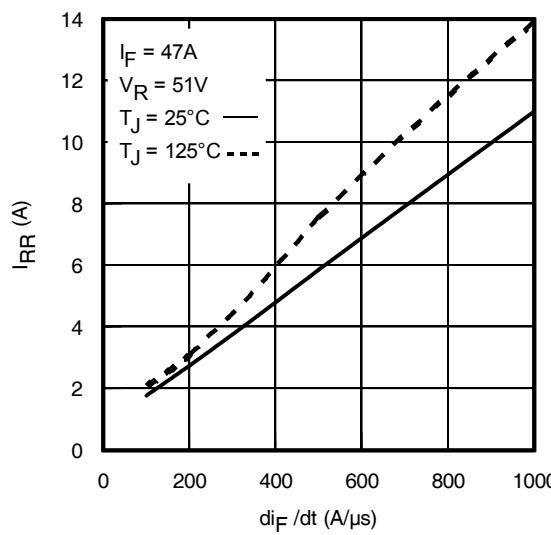


Fig. 18 - Typical Recovery Current vs. di_F/dt

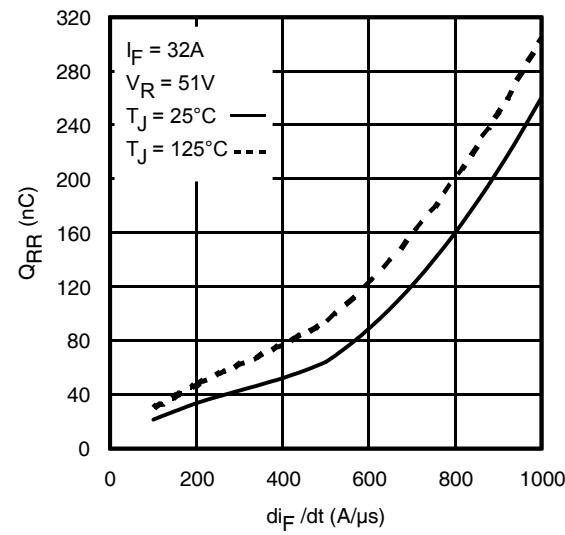


Fig. 19 - Typical Stored Charge vs. di_F/dt

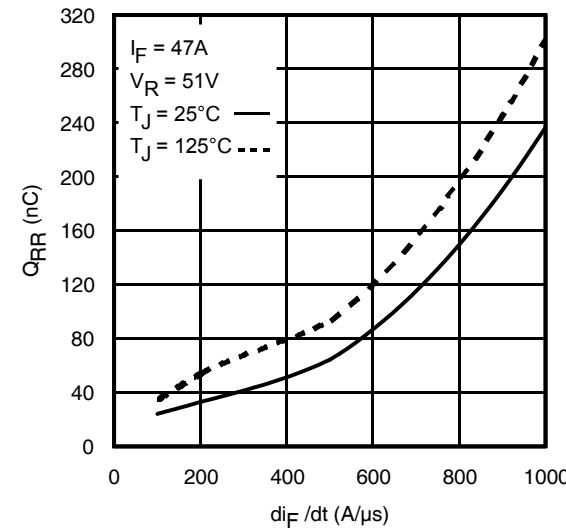


Fig. 20 - Typical Stored Charge vs. di_F/dt

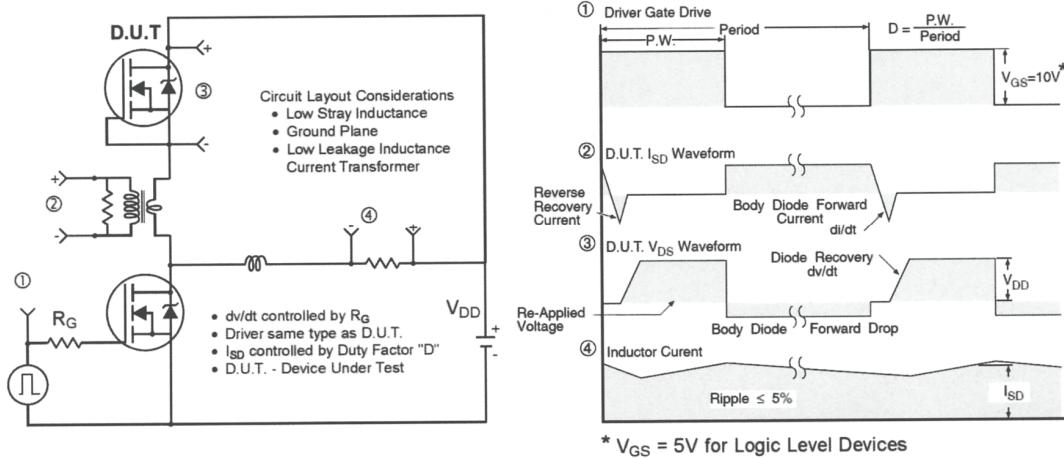


Fig 20. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

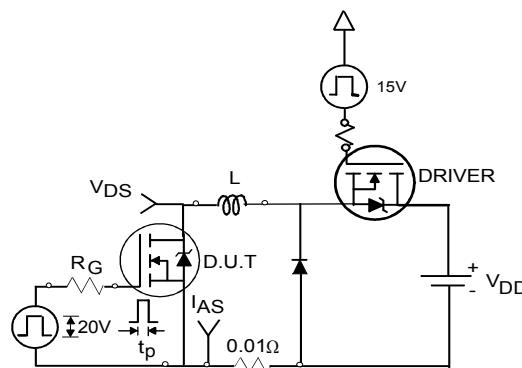


Fig 21a. Unclamped Inductive Test Circuit

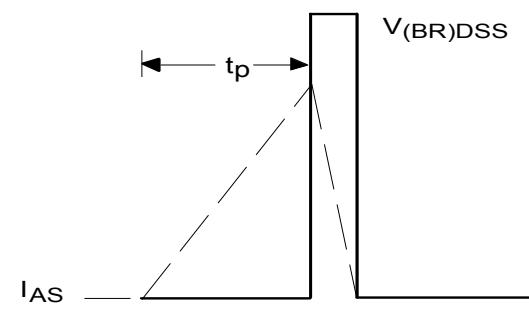


Fig 21b. Unclamped Inductive Waveforms

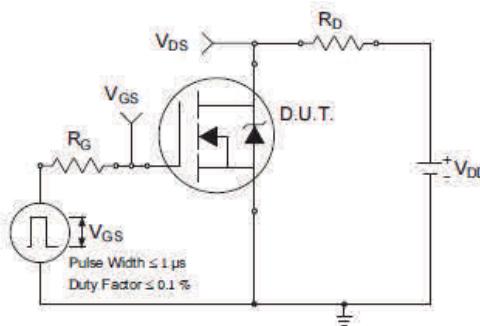


Fig 22a. Switching Time Test Circuit

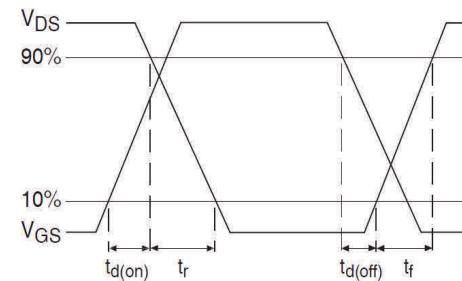


Fig 22b. Switching Time Waveforms

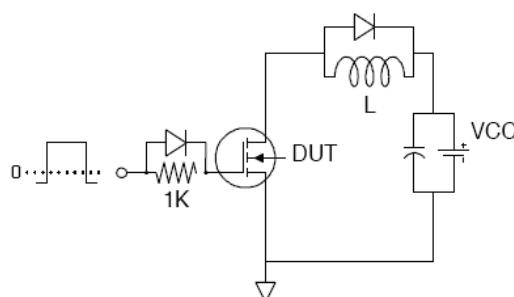


Fig 23a. Gate Charge Test Circuit

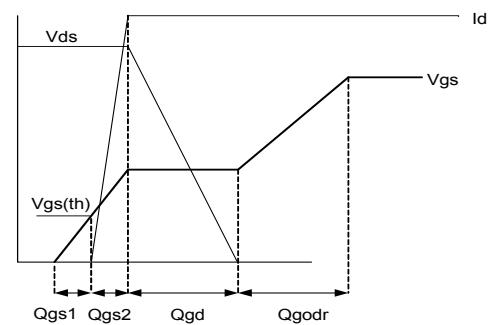
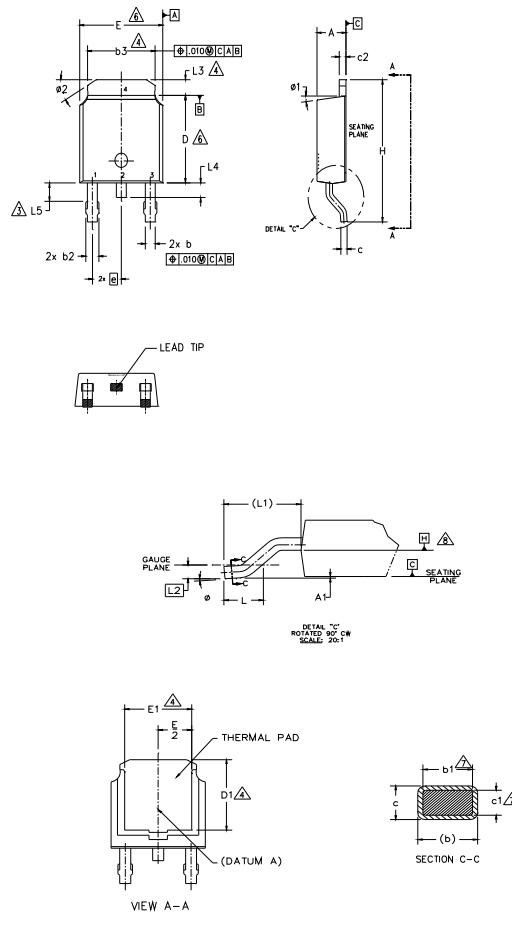


Fig 23b. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))


NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

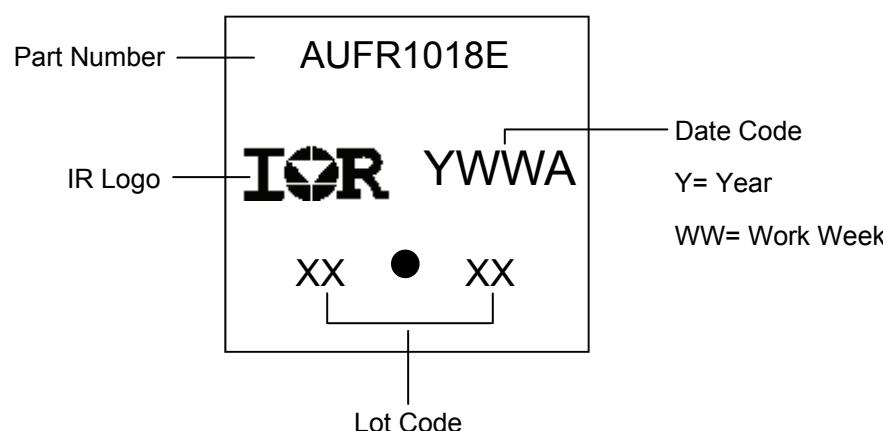
S Y M B O L	DIMENSIONS				N O T E S	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	2.18	2.39	.086	.094		
A1	—	0.13	—	.005		
b	0.64	0.89	.025	.035		
b1	0.65	0.79	.025	.031	7	
b2	0.76	1.14	.030	.045		
b3	4.95	5.46	.195	.215	4	
c	0.46	0.61	.018	.024		
c1	0.41	0.56	.016	.022	7	
c2	0.46	0.89	.018	.035		
D	5.97	6.22	.235	.245	6	
D1	5.21	—	.205	—	4	
E	6.35	6.73	.250	.265	6	
E1	4.32	—	.170	—	4	
e	2.29	BSC	.090	BSC		
H	9.40	10.41	.370	.410		
L	1.40	1.78	.055	.070		
L1	2.74	BSC	.108	REF.		
L2	0.51	BSC	.020	BSC		
L3	0.89	1.27	.035	.050	4	
L4	—	1.02	—	.040		
L5	1.14	1.52	.045	.060	3	
Ø	0°	10°	0°	10°		
Ø1	0°	15°	0°	15°		
Ø2	25°	35°	25°	35°		

LEAD ASSIGNMENTS
HEXFET

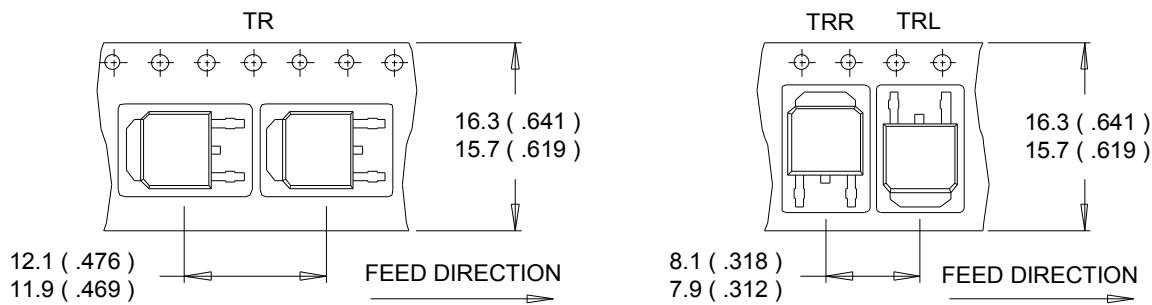
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

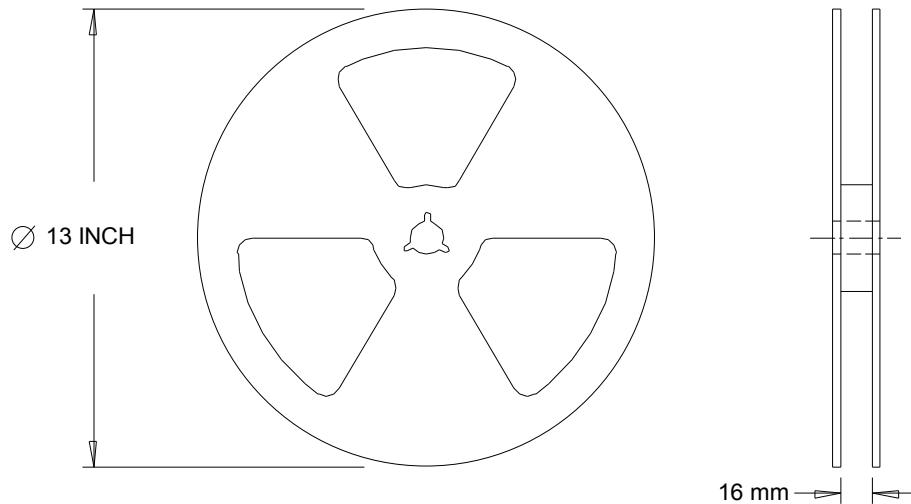
- 1.- GATE
- 2.- COLLECTOR
- 3.- Emitter
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D-Pak	MSL1
ESD	Machine Model	Class M4 (+/- 600V) [†] AEC-Q101-002	
	Human Body Model	Class H1C (+/- 1500V) [†] AEC-Q101-001	
	Charged Device Model	Class C4 (+/- 1000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

[†] Highest passing voltage.

Revision History

Date	Comments
11/19/2015	<ul style="list-style-type: none"> • Updated datasheet with corporate template • Corrected ordering table on page 1. • Corrected typo on test condition Coss eff. V_{DS} from "60V" to "48V" on page 2. • Updated typo on the fig.19 and fig.20, unit of y-axis from "A" to "nC" on page 6.

Published by

Infineon Technologies AG

81726 München, Germany

© Infineon Technologies AG 2015

All Rights Reserved.

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (www.infineon.com).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.