MC54/74HC623

Product Preview

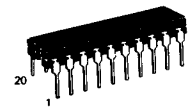
Octal 3-State Noninverting Bus Transceiver

High-Performance Silicon-Gate CMOS

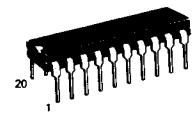
The MC54/74HC623 is identical in pinout to the LS623. The device outputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC623 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. Data is transmitted from Port A to Port B or from Port B to Port A, depending upon the levels at the two output enable inputs, OEA and OEB. When both of these inputs are enabled, the HC623 is able to store the data on data ports A and B, provided all other data sources to the two sets of bus lines are in the high impedance state.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

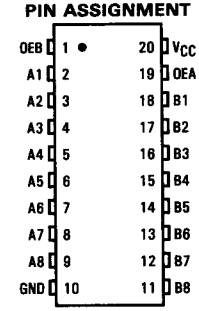
DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

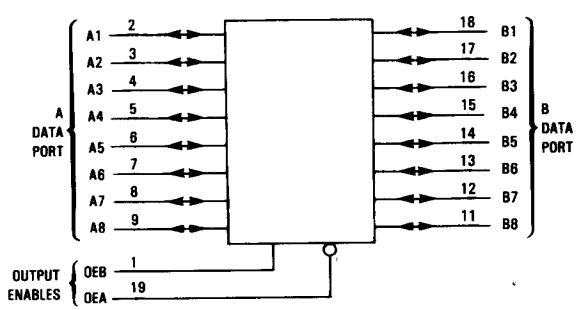
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXDW	SOIC

$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20 = V_{CC}
PIN 10 = GND

FUNCTION TABLE

Output Enables		Operation
OEB	OEA	
L	L	Data transmitted from Port B to Port A (noninverted)
H	H	Data transmitted from Port A to Port B (noninverted)
L	H	Buses isolated (High-Impedance State)
H	L	Data transmitted from Port B to Port A (noninverted) and from Port A to Port B (noninverted)

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