IFX54441

Wide Input Range Low Noise 300mA LDO

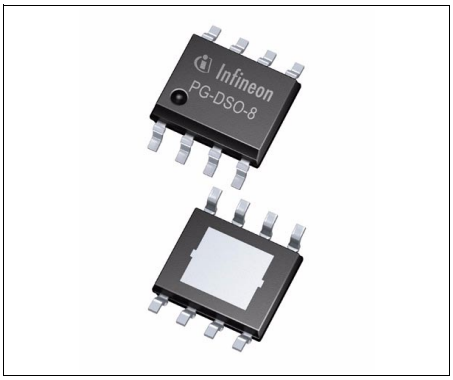
Data Sheet

Rev. 1.1, 2014-10-30

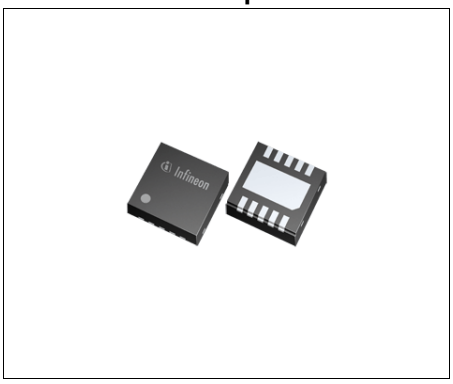
Standard Power

RoHS

1 Overview



PG-DSO-8 Exposed Pad



PG-TSON-10

Features

- Low Noise down to 24 µV_{RMS} (BW = 10 Hz to 100 kHz)
- 300mA Current Capability
- Low Quiescent Current: 30 µA
- Wide Input Voltage Range: 1.8 V to 20 V
- 2.5% Output Voltage Accuracy (over full temperature and load range)
- Low Dropout Voltage: 270 mV
- Very low Shutdown Current: < 1µA
- No Protection Diodes Needed
- Fixed Output Voltage: 3.3V
- Adjustable Version with Output from 1.22V to 20V
- Stable with ≥ 3.3 µF Output Capacitor
- Stable with Aluminium, Tantalum or Ceramic Capacitors
- Reverse Battery Protection
- No Reverse Current
- Overcurrent and Overtemperature Protected
- DSO-8 Exposed Pad and TSON-10 Exposed Pad packages
- Green Product (RoHS compliant)

Applications

- Microcontroller Supply
- Battery-Powered Systems
- Noise Sensitive Instruments
- Radar Applications
- Image Sensors

The IFX54441 is not qualified and manufactured according to the requirements of Infineon Technologies with regards to automotive and/or transportation applications. For automotive applications please refer to the Infineon TLx (TLE, TLS, TLF.....) voltage regulator products.

Type	Package	Marking
IFX54441EJV	PG-DSO-8 Exposed Pad	54441EV
IFX54441EJV33	PG-DSO-8 Exposed Pad	54441E33
IFX54441LDV	PG-TSON-10	544LV
IFX54441LDV33	PG-TSON-10	544L33

The IFX54441 is a micropower, low noise, low dropout voltage regulator. The device is capable of supplying an output current of 300 mA with a dropout voltage of 270 mV. Designed for use in battery-powered systems, the low quiescent current of 30 µA makes it an ideal choice.

A key feature of the IFX54441 is its low output noise. By adding an external 0.01 µF bypass capacitor output noise values down to 24 µV_{RMS} over a 10 Hz to 100 kHz bandwidth can be reached. The IFX54441 voltage regulator is stable with output capacitors as small as 3.3 µF. Small ceramic capacitors can be used without the series resistance required by many other regulators. Its internal protection circuitry includes reverse battery protection, current limiting and reverse current protection. The IFX54441 comes as fixed output voltage 3.3V as well as adjustable device with a 1.22 V reference voltage. It is available in a DSO-8 Exposed Pad and as well as in a TSON-10 Exposed Pad package.

2 Block Diagram

Note: Pin numbers in the block diagrams refer to the DSO-8 EP package type.

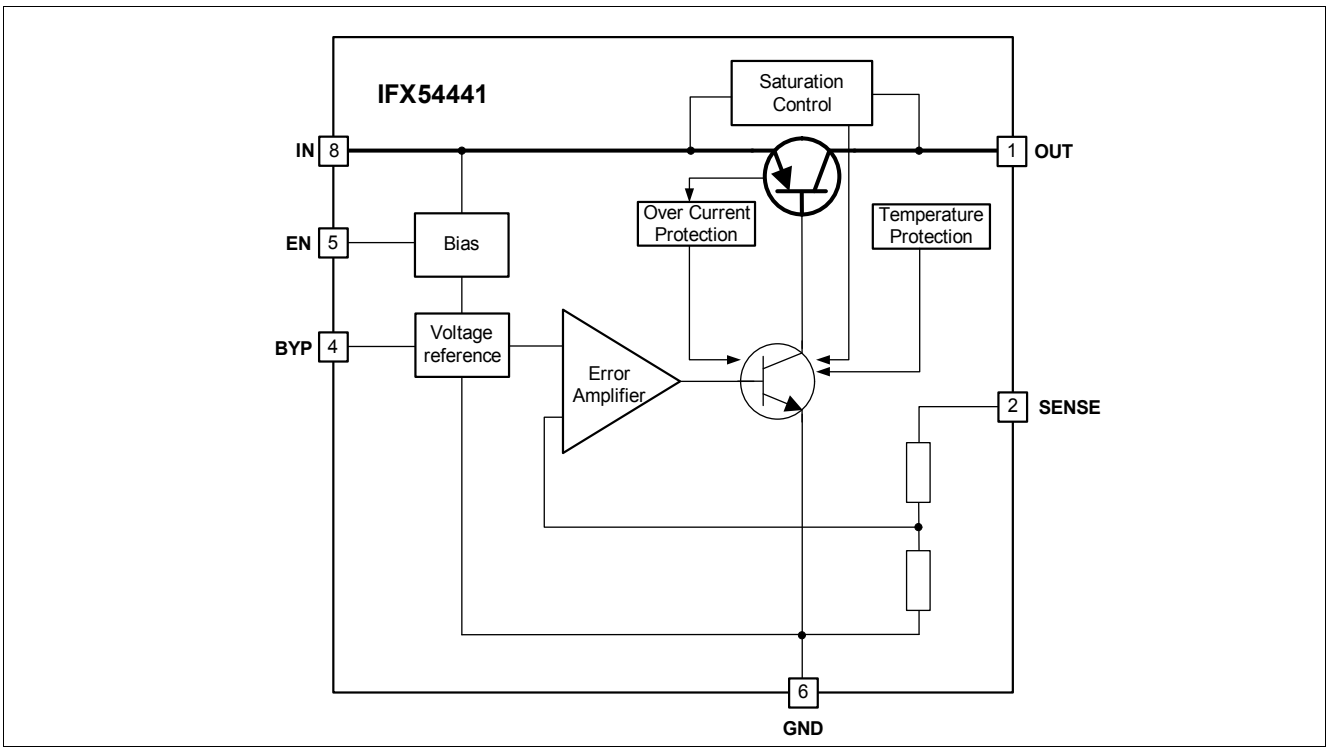


Figure 1 Block Diagram IFX54441 fixed voltage version

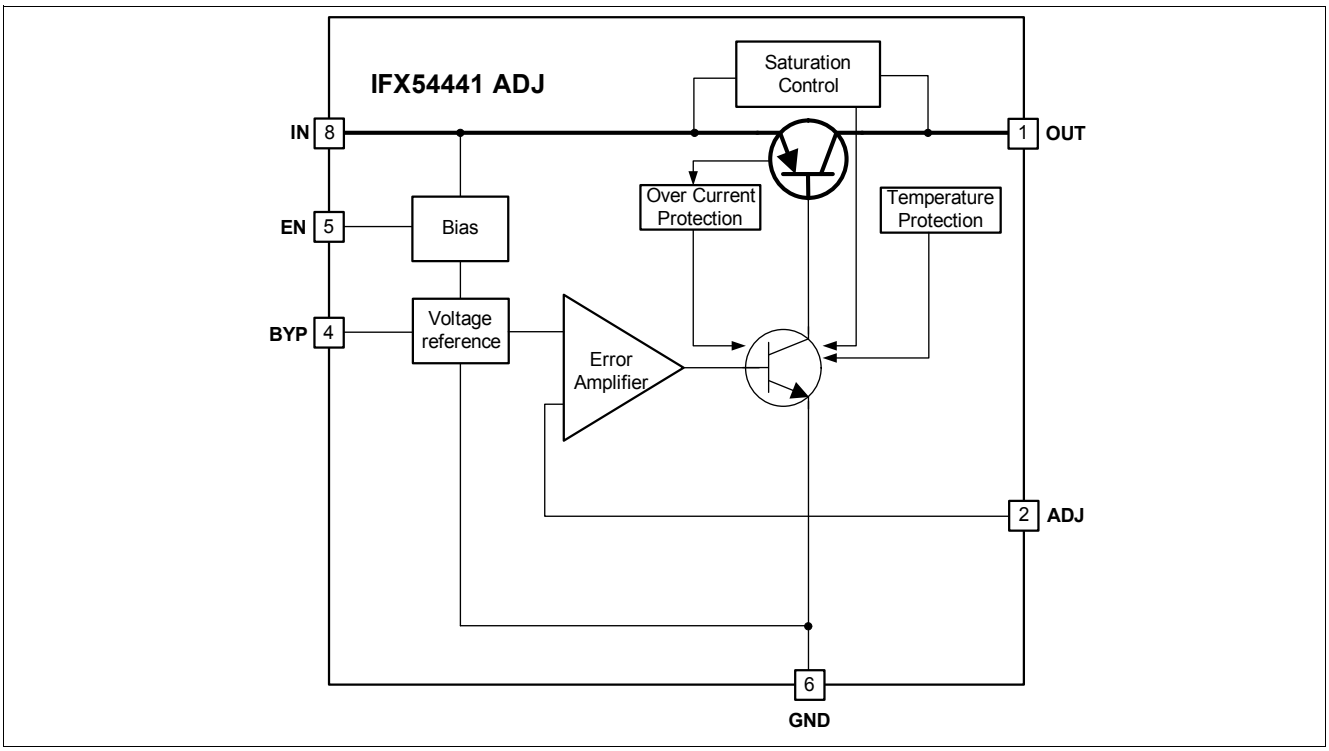


Figure 2 Block Diagram IFX54441 adjustable version

3 Pin Configuration

3.1 Pin Assignment

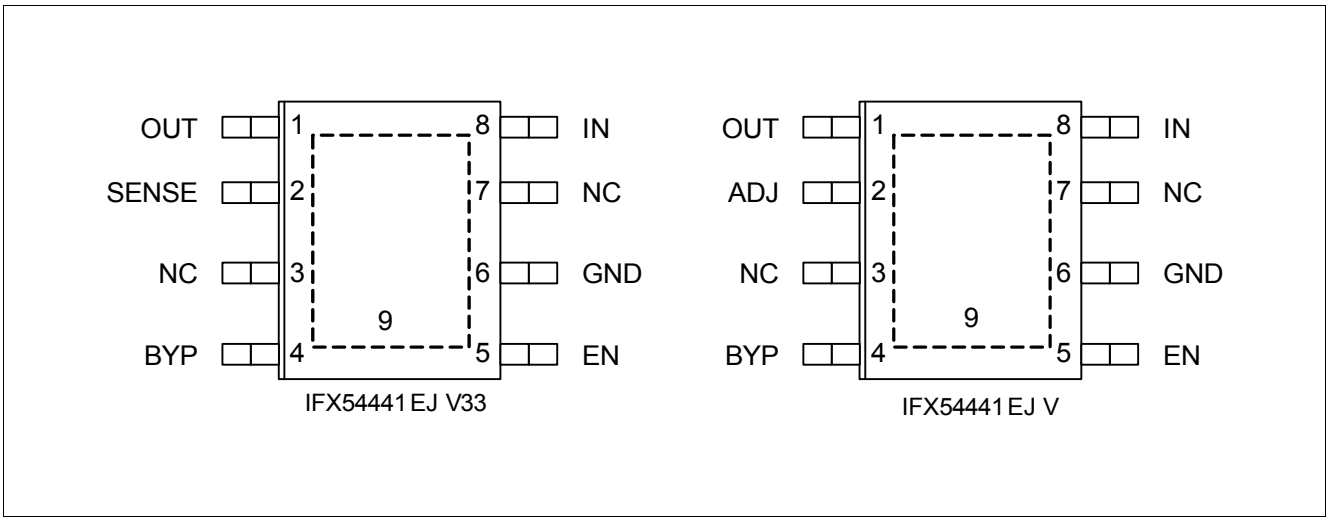


Figure 3 Pin Configuration of IFX54441 in PG-DSO-8 Exposed Pad for fixed voltage and adjustable version

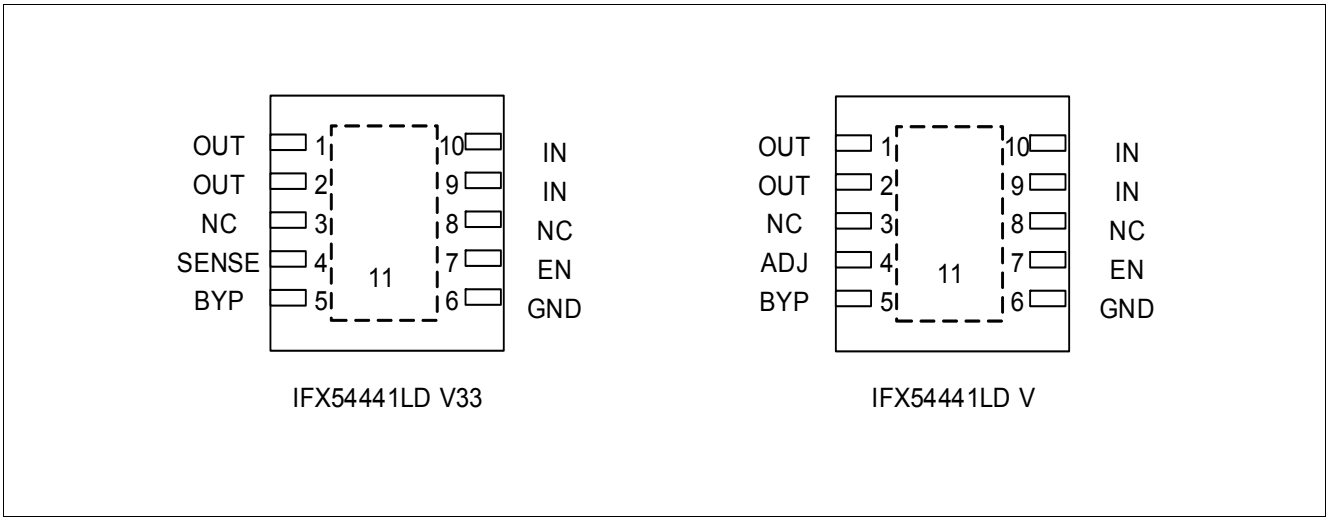


Figure 4 Pin Configuration of IFX54441 in TSON10 for fixed voltage and adjustable version

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1 (DSO-8 EP) 1,2 (TSON-10)	OUT	**Output**. Supplies power to the load. For this pin a minimum output capacitor of 3.3 µF is required to prevent oscillations. Larger output capacitors may be required for applications with large transient loads in order to limit peak voltage transients or when the regulator is applied in conjunction with a bypass capacitor. For more details please refer to the section **"Application Information" on Page 24**.
2 (DSO-8 EP) 4 (TSON-10)	SENSE (fix voltage version)	**Output Sense.** For the fixed voltage version the SENSE pin is the input to the error amplifier. This allows to achieve an optimized regulation performance in case of small voltage drops R_p that occur between regulator and load. In applications where such drops are relevant they can be eliminated by connecting the SENSE pin directly at the load. In standard configuration the SENSE pin can be connected directly to the OUT pin. For further details please refer to the section **"Kelvin Sense Connection" on Page 25**.
2 (DSO-8 EP) 4 (TSON-10)	ADJ (adjustable version)	**Adjust.** For the adjustable version the ADJ pin is the input to the error amplifier. The ADJ pin voltage is 1.22V referenced to ground and allows a output voltage range from 1.22V to 20V - V_{DR}. The ADJ pin is internally clamped to ±7 V. Please note that the bias current of the ADJ pin is flowing into the pin.[1)]
3, 7 (DSO-8 EP) 3, 8 (TSON-10)	NC	**No Connect.** The NC Pins have no connection to any internal circuitry. Connect either to GND or leave open.
4 (DSO-8) 5 (TSON-10)	BYP	**Bypass.** The BYP pin is used to bypass the reference of the IFX54441 to achieve low noise performance. The BYP-pin is clamped internally to ±0.6 V (i.e. one V_{BE}). A small capacitor from the output to the BYP pin will bypass the reference to lower the output voltage noise[2)]. If not used this pin must be left unconnected.
5 (DSO-8 EP) 7 (TSON-10)	EN	**Enable.** With the EN pin the IFX54441 can be put into a low power shutdown state. The output will be off when the EN is pulled low. The EN pin can be driven by 5V logic or open-collector logic with pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector gate[3)] and the EN pin current[4)]. Please note that if the EN pin is not used it must be connected to V_{IN}. It must not be left floating.
6 (DSO-8 EP) 6,(TSON-10)	GND	**Ground.** For the ADJ version connect the bottom of the output voltage setting resistor divider directly to the GND pin for optimum load regulation performance.
8 (DSO-8 EP) 9, 10 (TSON-10)	IN	**Input.** Via the input pin IN the power is supplied to the device. A capacitor at the input pin is required if the device is more than 6 inches away from the main input filter capacitor or if non-negligible inductance is present at the IN pin[5)]. The IFX54441 is designed to withstand reverse voltages on the Input pin with respect to GND and Output. In the case of reverse input (e.g. due to a wrongly attached battery) the device will act as if there is a diode in series with its input. In this way there will be no reverse current flowing into the regulator and no reverse voltage will appear at the load. Hence, the device will protect both - the device itself and the load.
9 (DSO-8 EP) 11 (TSON-10)	Tab	**Exposed Pad.** To ensure proper thermal performance, solder Pin 11 (exposed pad) of TSON10 to the PCB ground and tie directly to Pin 6. In the case of DSO-8 EP as well solder Pin 9 (exposed pad) to the PCB ground and tie directly to Pin 6.

1) The typical value of the ADJ pin bias current is 60 nA with a very good temperature stability.See also the corresponding Typical Performance Graph **“Adjust Pin Bias current I_{ADJ} versus Junction Temperature T_J” on Page 20**.
2) A maximum value of 10 nF can be used for reducing output voltage noise over the bandwidth from 10 Hz to 100 kHz.
3) Normally several microamperes.
4) Typical value is 1 µA.
5) In general the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. Depending on actual conditions an input capacitor in the range of 1 to 10 µF is sufficient.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage							
Voltage	V_{IN}	-20	–	20	V	–	P_4.1.1
Output Voltage							
Voltage	V_{OUT}	-20	–	20	V	–	P_4.1.2
Input to Output Differential Voltage	V_{IN} - V_{OUT}	-20	–	20	V	–	P_4.1.3
Sense Pin							
Voltage	V_{SENSE}	-20	–	20	V	–	P_4.1.4
ADJ Pin							
Voltage	V_{ADJ}	-7	–	7	V	–	P_4.1.5
BYP Pin							
Voltage	V_{BYP}	-0.6	–	0.6	V		P_4.1.6
Enable Pin							
Voltage	V_{EN}	-20	–	20	V	–	P_4.1.7
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.8
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.9
ESD Susceptibility							
All Pins	V_{ESD}	-2	–	2	kV	HBM[2)]	P_4.1.10
All Pins	V_{ESD}	-1	–	1	kV	CDM[3)]	P_4.1.11

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage Range (3.3 V voltage version)	V_{IN}	3.8 V	–	20	V	–	P_4.2.1
Input Voltage Range (adjustable voltage version)	V_{IN}	2.3	–	20	V	–[1)]	P_4.2.2
Operating Junction Temperature	T_j	-40	–	125	°C	–	P_4.2.3

1) For the IFX54441 adjustable version the minimum limit of the functional range V_{IN} is tested and specified with the ADJ- pin connected to the OUT pin.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
IFX54441 EJ (PG-DSO8 Exposed Pad)							
Junction to Case	R_{thJC}	–	7.0	–	K/W	–	P_4.3.1
Junction to Ambient	R_{thJA}	–	39	–	K/W	–[2)]	P_4.3.2
Junction to Ambient	R_{thJA}	–	155	–	K/W	Footprint only[3)]	P_4.3.3
Junction to Ambient	R_{thJA}	–	66	–	K/W	300 mm² heatsink area on PCB[3)]	P_4.3.4
Junction to Ambient	R_{thJA}	–	52	–	K/W	600 mm² heatsink area on PCB[3)]	P_4.3.5
IFX54441 LD (PG-TSON10)							
Junction to Case	R_{thJC}	–	6.4	–	K/W	–	P_4.3.6
Junction to Ambient	R_{thJA}	–	53	–	K/W	–[2)]	P_4.3.7
Junction to Ambient	R_{thJA}	–	183	–	K/W	Footprint only[3)]	P_4.3.8
Junction to Ambient	R_{thJA}	–	69	–	K/W	300 mm² heatsink area on PCB[3)]	P_4.3.9
Junction to Ambient	R_{thJA}	–	57	–	K/W	600 mm² heatsink area on PCB[3)]	P_4.3.10

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70 µm Cu).

5 Electrical Characteristics

5.1 Electrical Characteristics Table

Table 4 Electrical Characteristics

-40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Minimum Operating Voltage	$V_{IN,min}$	–	1.8	2.3	V	I_{OUT} = 300 mA[1)2)3)]	P_5.1.1
Output Voltage[4)]							
IFX54441EJ V33 IFX54441LD V33	V_{OUT}	3.220	3.30	3.380	V	1 mA < I_{OUT} < 300 mA; 4.3 V < V_{IN} < 20 V	P_5.1.2
IFX54441EJV IFX54441LDV	V_{OUT}	1.190	1.22	1.250	V	1m A < I_{OUT} < 300 mA; 2.3 V < V_{IN} < 20 V[3)]	P_5.1.3
Line Regulation							
IFX54441EJ V33 IFX54441LD V33	ΔV_{OUT}	–	1	20	mV	ΔV_{IN} = 3.8 V to 20 V; I_{OUT} = 1 mA	P_5.1.4
IFX54441EJ V IFX54441LD V	ΔV_{OUT}	–	1	20	mV	ΔV_{IN} = 2.0 V to 20 V; I_{OUT} = 1 mA[3)]	P_5.1.5
Load Regulation							
IFX54441EJV33 IFX54441LDV33	ΔV_{OUT}	–	6	15	mV	T_J = 25°C;V_{IN} = 4.3 V; Δ I_{OUT} = 1 to 300 mA	P_5.1.6
IFX54441EJV33 IFX54441LDV33	ΔV_{OUT}	–	–	28	mV	V_{IN} = 4.3 V; Δ I_{OUT} = 1 to 300 mA	P_5.1.7
IFX54441EJV IFX54441LDV	ΔV_{OUT}	–	3	8	mV	T_J = 25°C; V_{IN} = 2.3 V; ΔI_{OUT} = 1 to 300 mA[3)]	P_5.1.8
IFX54441EJV IFX54441LDV	ΔV_{OUT}	–	–	12	mV	V_{IN} = 2.3 V; ΔI_{OUT} = 1 to 300 mA[3)]	P_5.1.9
Dropout Voltage[2)5)6)]							
Dropout Voltage	V_{DR}	–	100	130	mV	I_{OUT} = 10 mA; V_{IN} = $V_{OUT,nom}$; T_J = 25°C	P_5.1.10
Dropout Voltage	V_{DR}	–	–	190	mV	I_{OUT} = 10 mA; V_{IN} = $V_{OUT,nom}$	P_5.1.11
Dropout Voltage	V_{DR}	–	150	190	mV	I_{OUT} = 50 mA; V_{IN} = $V_{OUT,nom}$; T_J = 25°C	P_5.1.12
Dropout Voltage	V_{DR}	–	–	250	mV	I_{OUT} = 50 mA; V_{IN} = $V_{OUT,nom}$	P_5.1.13
Dropout Voltage	V_{DR}	–	190	220	mV	I_{OUT} = 100 mA; V_{IN} = $V_{OUT,nom}$; T_J = 25°C	P_5.1.14
Dropout Voltage	V_{DR}	–	–	300	mV	I_{OUT} = 100 mA; V_{IN} = $V_{OUT,nom}$	P_5.1.15
Dropout Voltage	V_{DR}	–	270	300	mV	I_{OUT} = 300 mA; V_{IN} = $V_{OUT,nom}$; T_J = 25°C	P_5.1.16

Table 4 Electrical Characteristics (cont'd)

-40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Dropout Voltage	V_{DR}	–	–	400	mV	I_{OUT} = 300 mA; V_{IN} = $V_{OUT,nom}$	P_5.1.17
GND Pin Current[5)7)]							
GND Pin Current	I_{GND}	–	30	60	µA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 0 mA	P_5.1.18
GND Pin Current	I_{GND}	–	50	100	µA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 1 mA	P_5.1.19
GND Pin Current	I_{GND}	–	300	850	µA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 50 mA	P_5.1.20
GND Pin Current	I_{GND}	–	0.7	2.2	mA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 100 mA	P_5.1.21
GND Pin Current	I_{GND}	–	4	12	mA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 300 mA	P_5.1.22
Quiescent Current in Off-Mode (EN-pin low)	I_q	–	0.1	1	µA	V_{IN} = 6 V; V_{EN} = 0 V; T_J = 25°C	P_5.1.23
Enable							
Enable Threshold High	$V_{th,EN}$	–	0.8	2.0	V	V_{OUT} = Off to On	P_5.1.24
Enable Threshold Low	$V_{tl,EN}$	0.25	0.65	–	V	V_{OUT} = On to Off	P_5.1.25
EN Pin Current[8)]	I_{EN}	–	0.01	–	µA	V_{EN} = 0 V; T_J = 25°C	P_5.1.26
EN Pin Current[8)]	I_{EN}	–	1	–	µA	V_{EN} = 20 V; T_J = 25°C	P_5.1.27
Adjust Pin Bias Current[9)11)]							
ADJ Pin Bias Current	$I_{bias,ADJ}$	–	60	–	nA	T_J = 25°C	P_5.1.28
Output Voltage Noise[11)]							
Output Voltage Noise IFX54441EJV[10)] IFX54441LDV[10)]	e_{no}	–	41	–	μV_{RMS}	C_{OUT} = 10 µF ceramic; C_{BYP} = 10 nF; I_{OUT} = 300 mA; (BW = 10Hz to100kHz)	P_5.1.29
Output Voltage Noise IFX54441EJV[10)] IFX54441LDV[10)]	e_{no}	–	28	–	μV_{RMS}	C_{OUT} = 10 µF ceramic +250mΩ resistor in series; C_{BYP} = 10 nF; I_{OUT} = 300 mA; (BW = 10 Hz to100 kHz)	P_5.1.30
Output Voltage Noise IFX54441EJV[10)] IFX54441LDV[10)]	e_{no}	–	29	–	μV_{RMS}	C_{OUT} = 22 µF ceramic; C_{BYP} = 10 nF; I_{OUT} = 300 mA; (BW = 10 Hz to100 kHz)	P_5.1.31
Output Voltage Noise IFX54441EJV[10)] IFX54441LDV[10)]	e_{no}	–	24	–	μV_{RMS}	C_{OUT} = 22 µF ceramic +250mΩ resistor in series; C_{BYP} = 10 nF; I_{OUT} = 300 mA; (BW = 10 Hz to100 kHz)	P_5.1.32

Table 4 Electrical Characteristics (cont'd)

-40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage Noise IFX54441EJV33 IFX54441LDV33	e_{no}	–	45	–	μV_{RMS}	C_{OUT} = 10 µF ceramic; C_{BYP} = 10 nF; I_{OUT} = 300 mA; (BW = 10 Hz to100 kHz)	P_5.1.33
Output Voltage Noise IFX54441EJV33 IFX54441LDV33	e_{no}	–	35	–	μV_{RMS}	C_{OUT} = 10 µF ceramic +250mΩ resistor in series; C_{BYP} = 10 nF; I_{OUT} = 300 mA; (BW = 10 Hz to100 kHz)	P_5.1.34
Output Voltage Noise IFX54441EJV33 IFX54441LDV33	e_{no}	–	33	–	μV_{RMS}	C_{OUT} = 22 µF ceramic; C_{BYP} = 10 nF; I_{OUT} = 300 mA; (BW = 10 Hz to100 kHz)	P_5.1.35
Output Voltage Noise IFX54441EJV33 IFX54441LDV33	e_{no}	–	30	–	μV_{RMS}	C_{OUT} = 22 µF ceramic +250mΩ resistor in series; C_{BYP} = 10 nF; I_{OUT} = 300 mA; (BW = 10 Hz to100 kHz)	P_5.1.36
Power Supply Ripple Rejection[11)]							
Power Supply Ripple Rejection	$PSRR$	–	65	–	dB	V_{IN} - V_{OUT} = 1.5 V (avg); V_{RIPPLE} = 0.5 Vpp; f_r = 120 Hz; I_{OUT} = 300 mA	P_5.1.37
Output Current Limitation							
Output Current Limit	$I_{OUT,limit}$	320	–	–	mA	V_{IN} = 7 V; V_{OUT} = 0 V	P_5.1.38
Output Current Limit	$I_{OUT,limit}$	320	–	–	mA	V_{IN} = $V_{OUT,nom}$ + 1 V or 2.3V[12)]; ΔV_{OUT} = -0.1 V	P_5.1.39
Input Reverse Leakage Current							
Input Reverse Leakage	$I_{leak,rev}$	–	–	1	mA	V_{IN} = -20 V; V_{OUT} = 0 V	P_5.1.40
Reverse Output Current[13)]							
Fixed Voltage Versions	$I_{Reverse}$	–	10	20	µA	V_{OUT} = $V_{OUT,nom}$; V_{IN} < $V_{OUT,nom}$; T_J = 25°C	P_5.1.41
Adjustable Voltage Version	$I_{Reverse}$	–	5	10	µA	V_{OUT} = 1.22 V; V_{IN} < 1.22 V; T_J = 25°C[3)]	P_5.1.42

Table 4 Electrical Characteristics (cont'd)

-40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

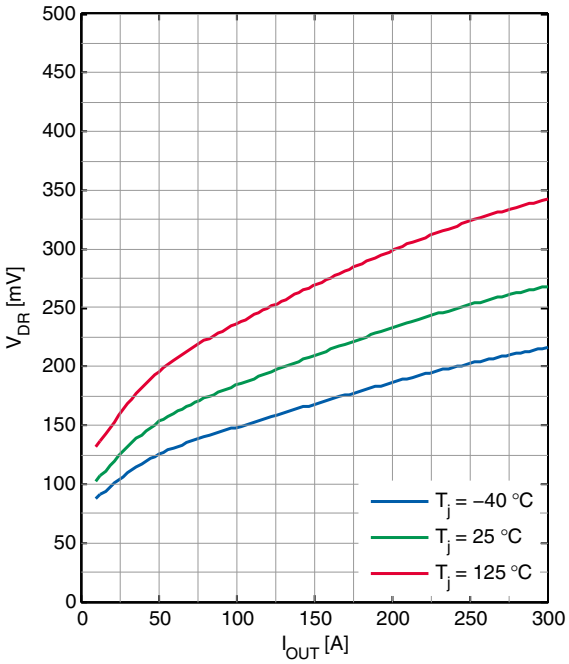
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Capacitor[11]							
Output Capacitance	C_{OUT}	3.3	–	–	µF	C_{BYP} = 0 nF	P_5.1.43
ESR	ESR	–[14]	–	3	Ω	–	P_5.1.44

1) This parameter defines the minimum input voltage for which the device is powered up and provides the maximum output current of 300 mA. Due to the nominal output voltage of 3.3 V of the fixed voltage version or depending on the chosen setting of the external voltage divider as well as on the applied conditions the device may either regulate its nominal output voltage or it may be in tracking mode. For further details please also refer to the V_{OUT} specification in **Table 4**.
2) For the IFX54441EJV and IFX54441LDV adjustable versions the dropout voltage for certain output voltage / load conditions will be restricted by the minimum input voltage specification.
3) The adjustable versions of the IFX54441 are tested and specified for these conditions with the ADJ pin connected to the OUT pin.
4) The operation conditions are limited by the maximum junction temperature. The regulated output voltage specification will only apply for conditions where the limit of the maximum junction temperature is fulfilled. It will therefore not apply for all possible combinations of input voltage and output current at a given output voltage. When operating at maximum input voltage, the output current must be limited for thermal reasons. The same holds true when operating at maximum output current where the input voltage range must be limited for thermal reasons.
5) To satisfy requirements for minimum input voltage, the adjustable version of the IFX54441 is tested and specified for these conditions with an external resistor divider (two 250 kΩ resistors) for an output voltage of 2.44 V. The external resistors will add a 5 µA DC load on the output.
6) The dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to V_{IN} - V_{DR}.
7) GND-pin current is tested with V_{IN} = $V_{OUT,nom}$ or V_{IN} = 2.3 V, whichever is greater, and a current source load. This means that this parameter is tested while being in dropout condition and thus reflects a worst case condition. The GND-pin current will in most cases decrease slightly at higher input voltages - please also refer to the corresponding typical performance graphs.
8) The EN pin current flows into EN pin.
9) The ADJ pin current flows into ADJ pin.
10) ADJ pin connected to OUT pin.
11) Not subject to production test, specified by design.
12) whichever of the two values of V_{IN} is greater in order to also satisfy the requirements for $V_{IN,min}$.
13) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out of the GND pin.
14) C_{BYP} = 0 nF, C_{OUT} ≥ 3.3 µF; please note that for cases where a bypass capacitor at BYP is used - depending on the actual applied capacitance of C_{OUT} and C_{BYP} - a minimum requirement for ESR may apply. For further details please also refer to the corresponding typical performance graph.

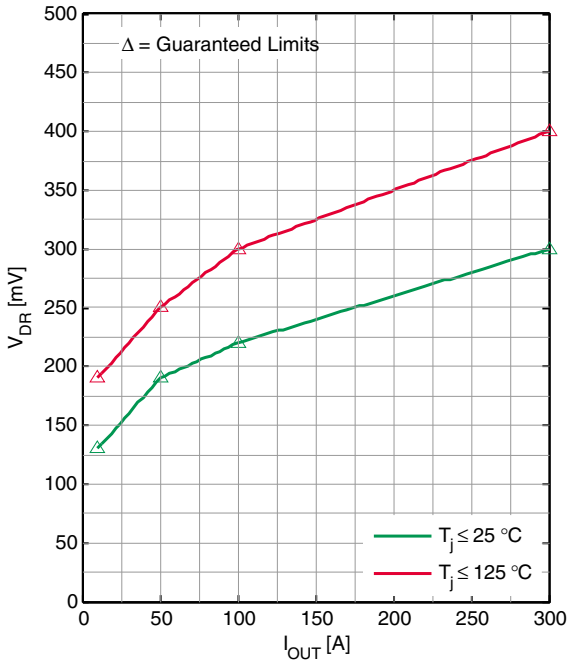
Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specified mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

6 Typical Performance Characteristics

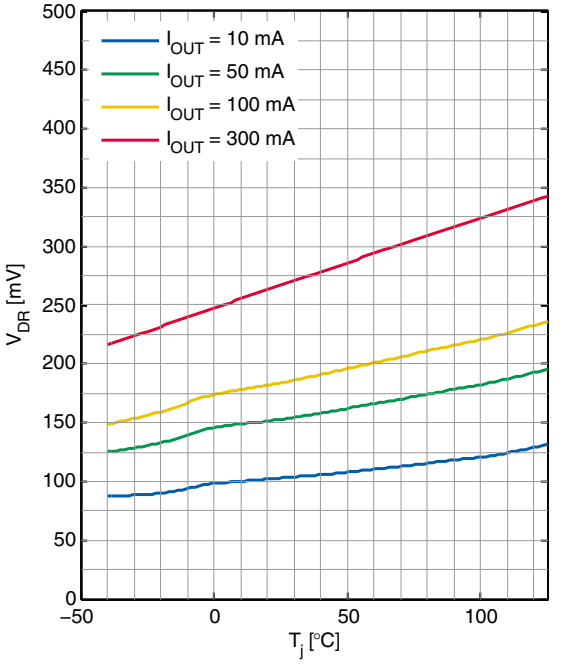
Dropout Voltage V_{DR} versus Output Current I_{OUT}



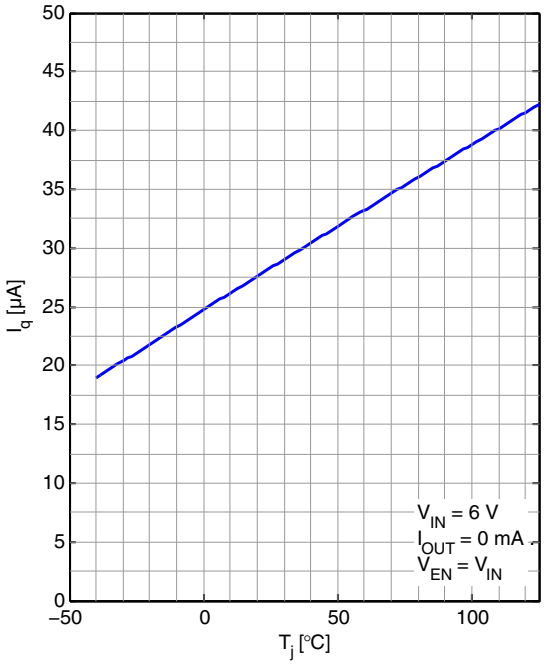
Guaranteed Dropout Voltage V_{DR} versus Output Current I_{OUT}



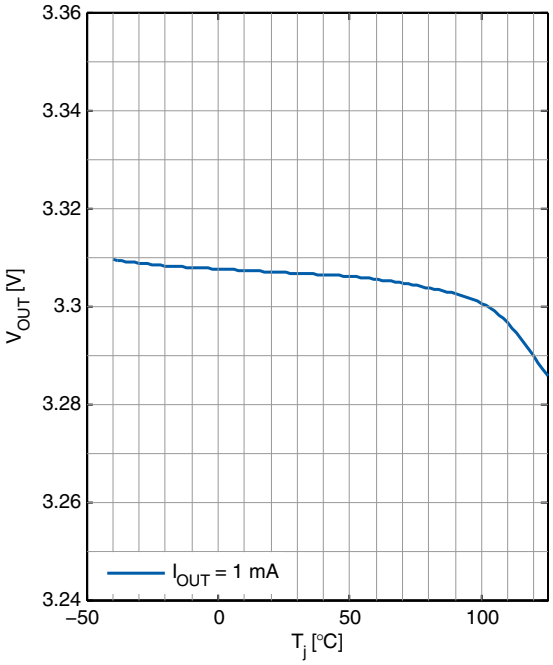
Dropout Voltage V_{DR} versus Junction Temperature T_J



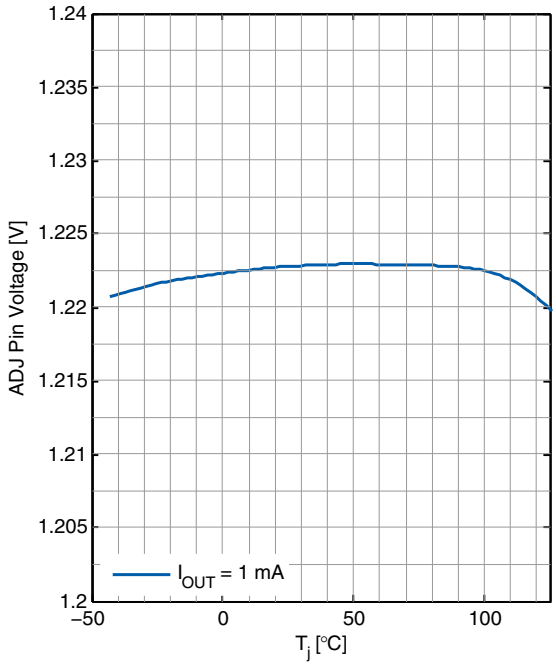
Quiescent Current versus Junction Temperature T_J



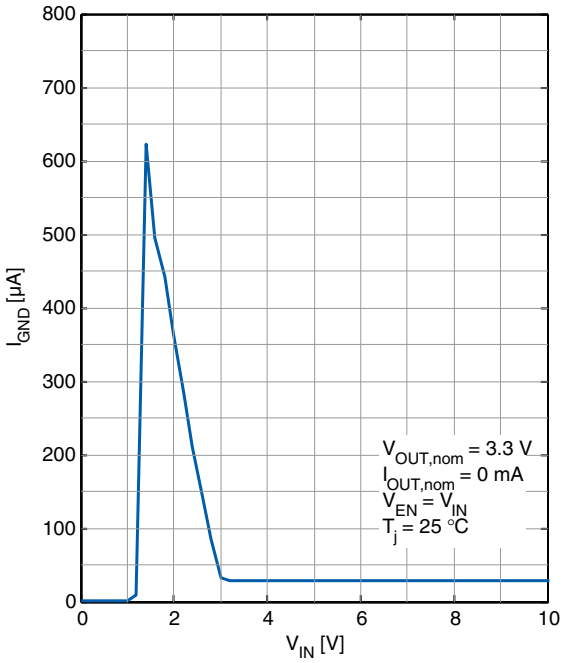
Output Voltage V_{OUT} versus Junction Temperature T_J (IFX54441EJV33)



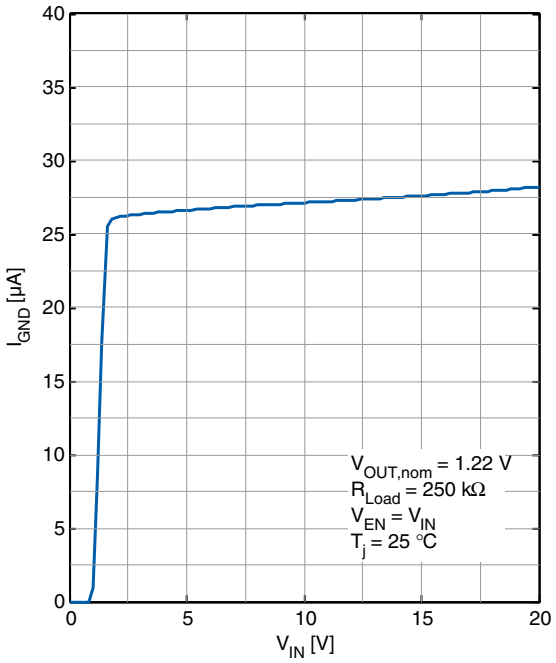
Output / ADJ Pin Voltage V_{OUT} versus Junction Temperature T_J (IFX54441EJV)



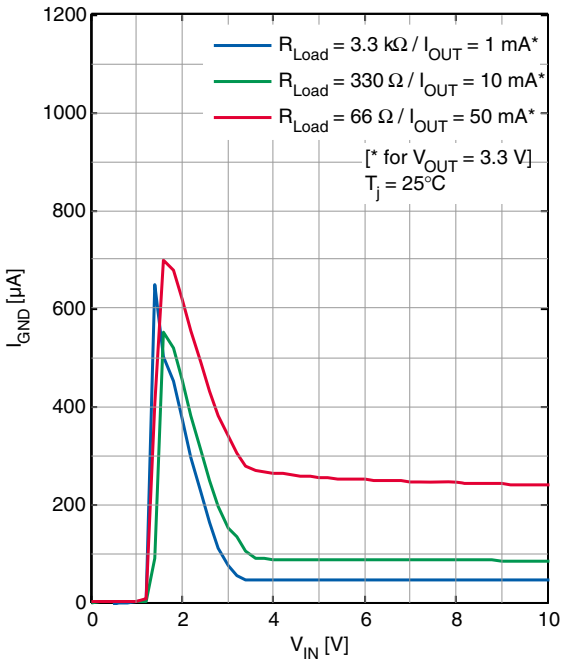
Quiescent Current I_q versus Input Voltage V_{IN} (IFX54441EJV33)



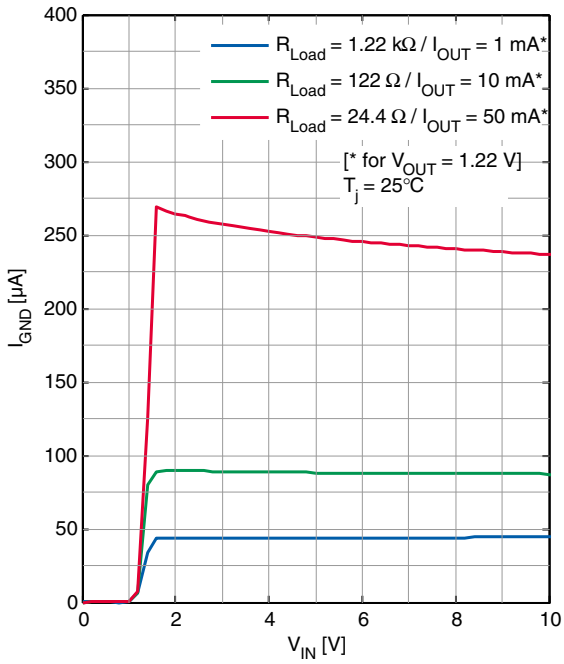
Quiescent Current I_q versus Input Voltage V_{IN} (IFX54441EJV)



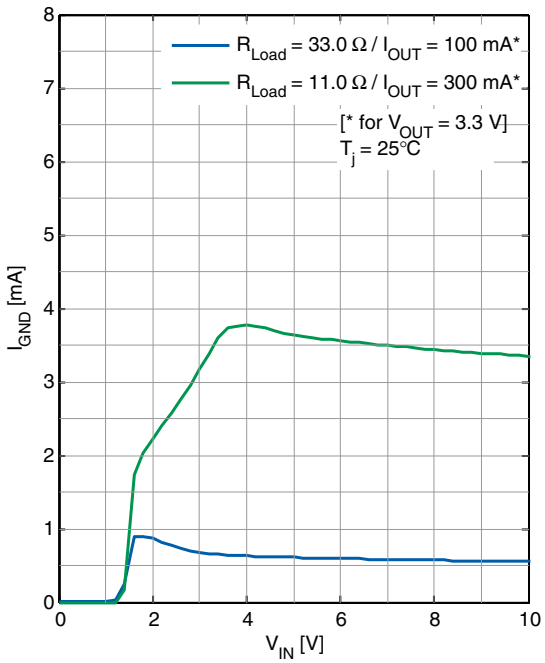
GND Current I_{GND} versus Input Voltage V_{IN} (IFX54441EJV33)



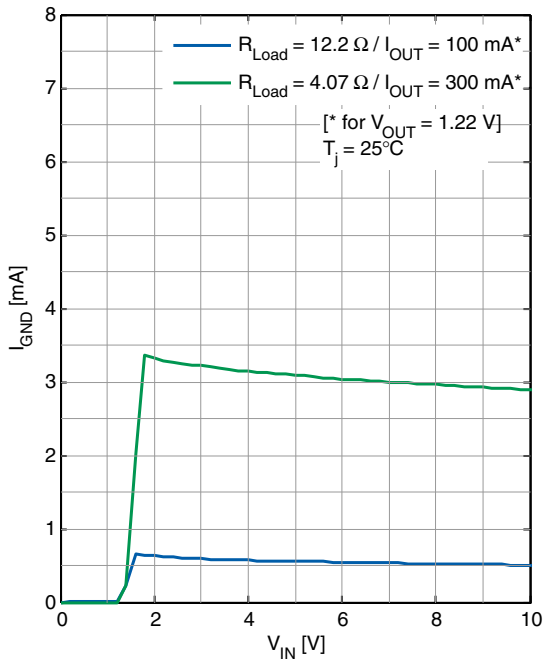
GND Current I_{GND} versus Input Voltage V_{IN} (IFX54441EJV)



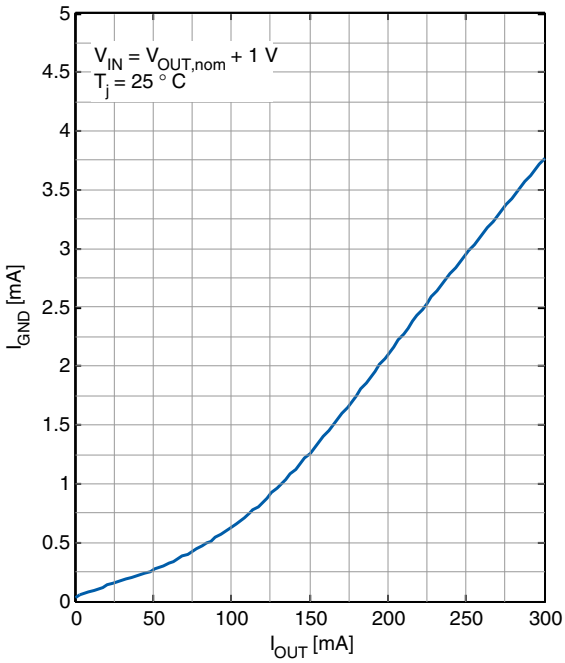
GND Current I_{GND} versus Input Voltage V_{IN} (IFX54441EJV33)



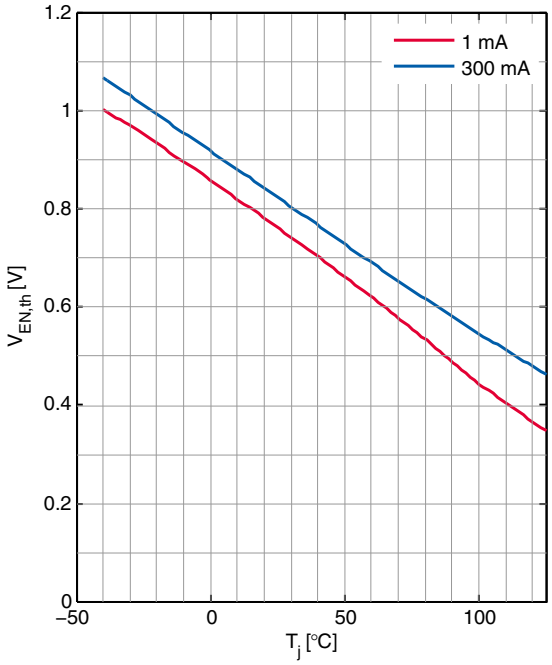
GND Current I_{GND} versus Input Voltage V_{IN} (IFX54441EJV)



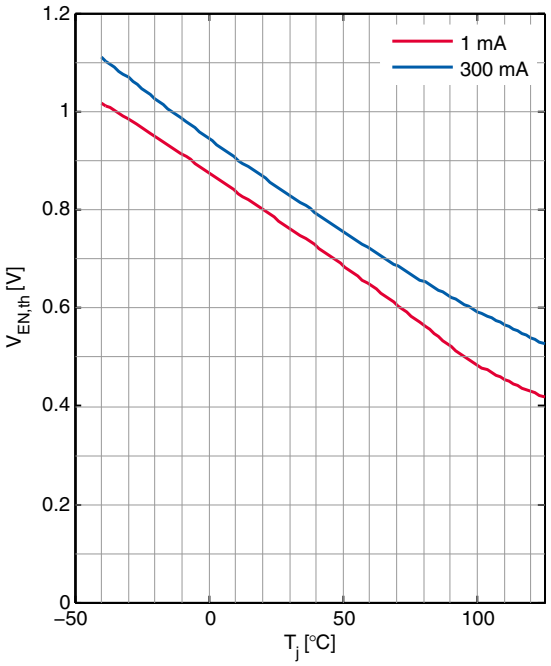
GND Current I_{GND} versus Output Current I_{OUT}



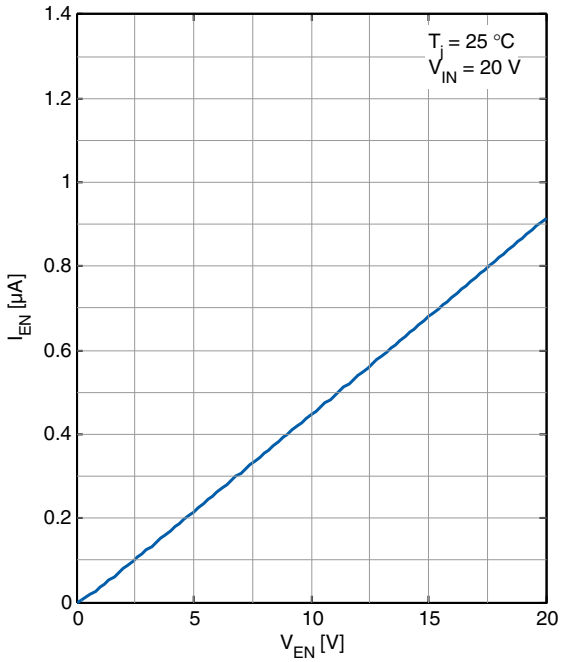
EN Pin Threshold (On-to-Off) versus Junction Temperature T_J



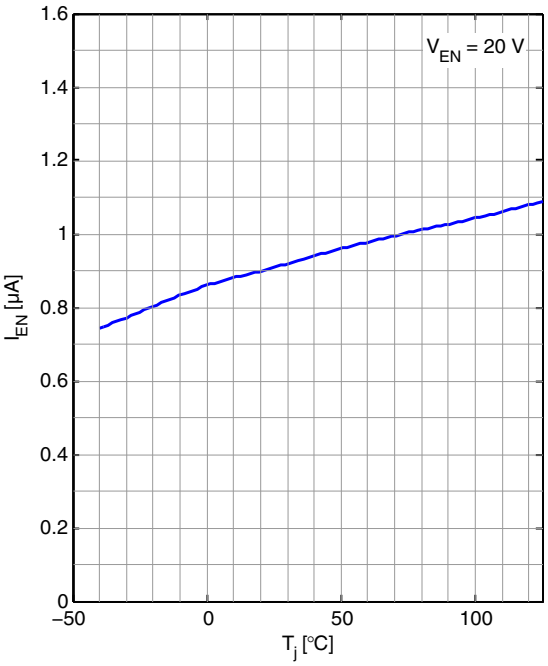
EN Pin Threshold (Off-to-On) versus Junction Temperature T_J



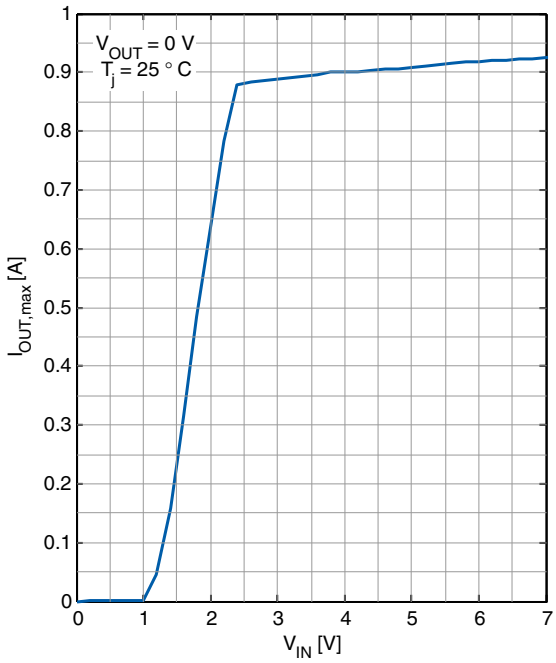
EN Pin Input Current versus EN Pin Voltage V_{EN}



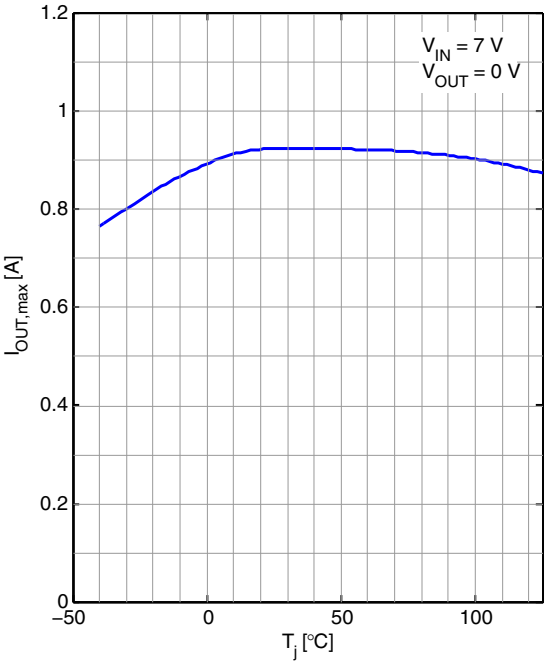
EN Pin Input Current versus Junction Temperature T_J



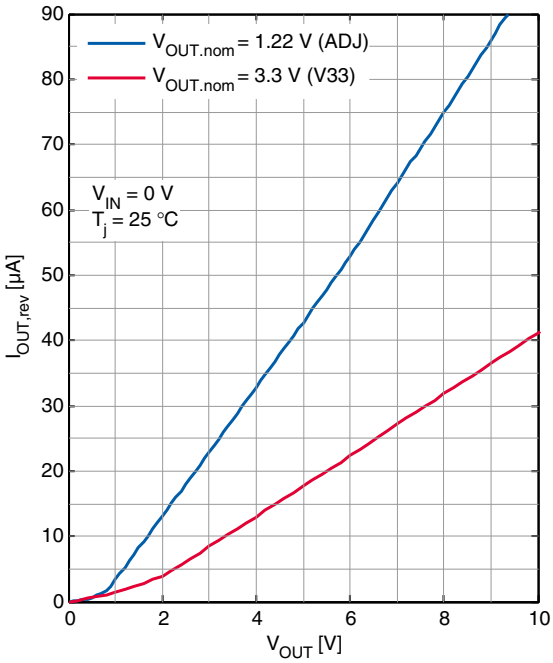
Current Limit versus Input Voltage V_{IN}



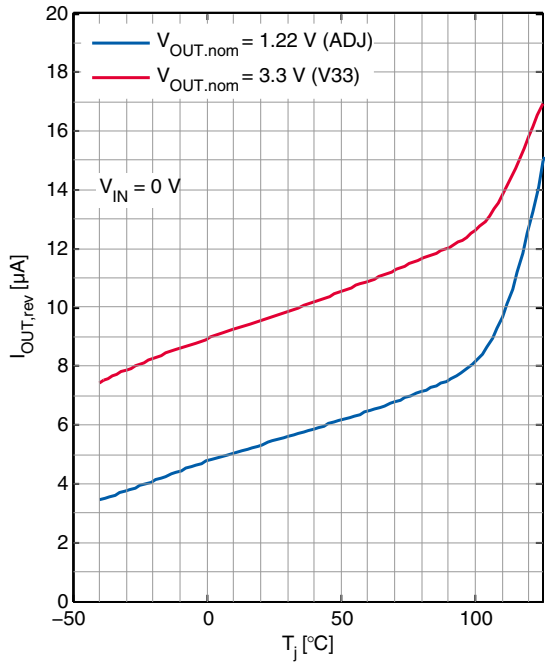
Current Limit versus Junction Temperature T_J



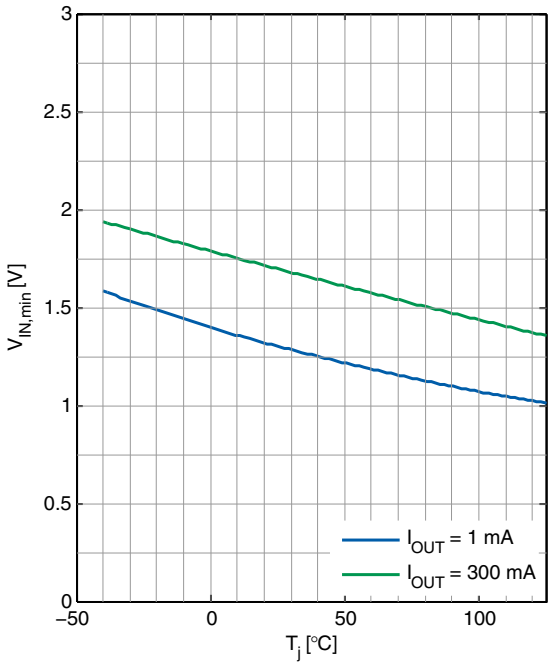
Reverse Output Current versus Output Voltage V_{OUT}



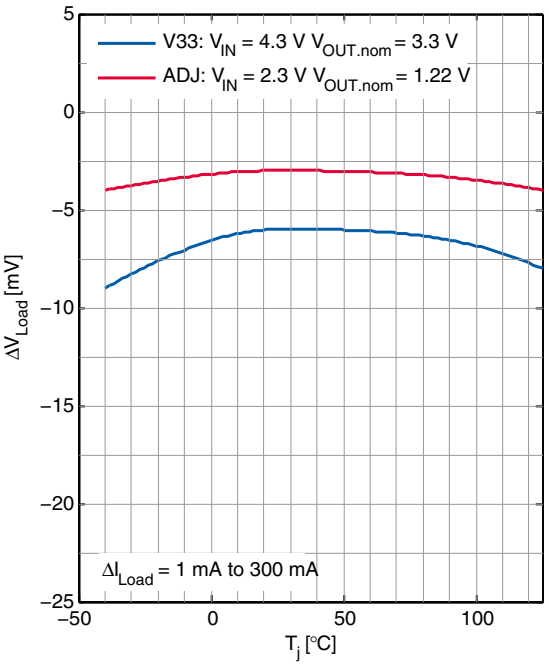
Reverse Output Current versus Junction Temperature T_J



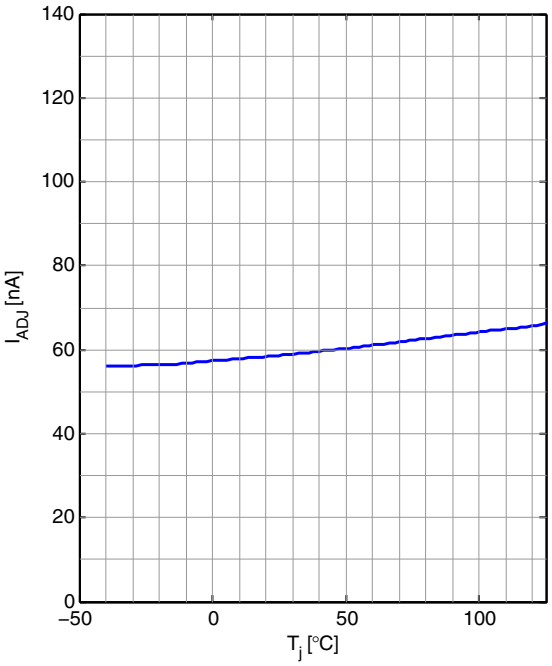
Minimum Input Voltage[1] versus Junction Temperature T_J



Load Regulation versus Junction Temperature T_J

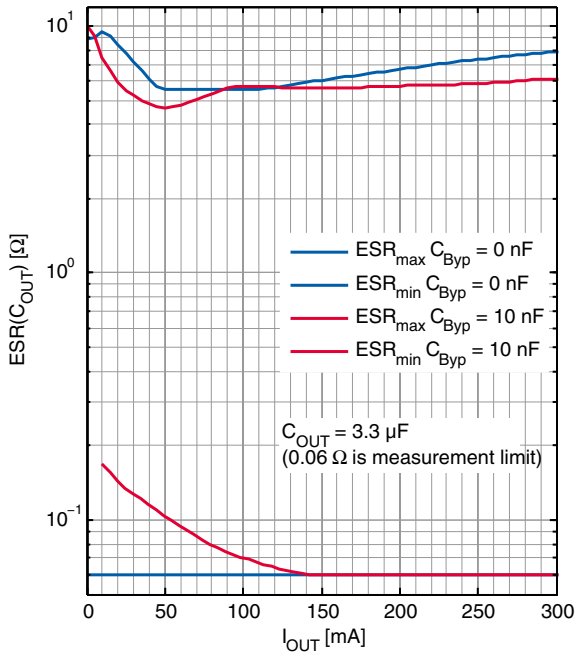


Adjust Pin Bias current I_{ADJ} versus Junction Temperature T_J

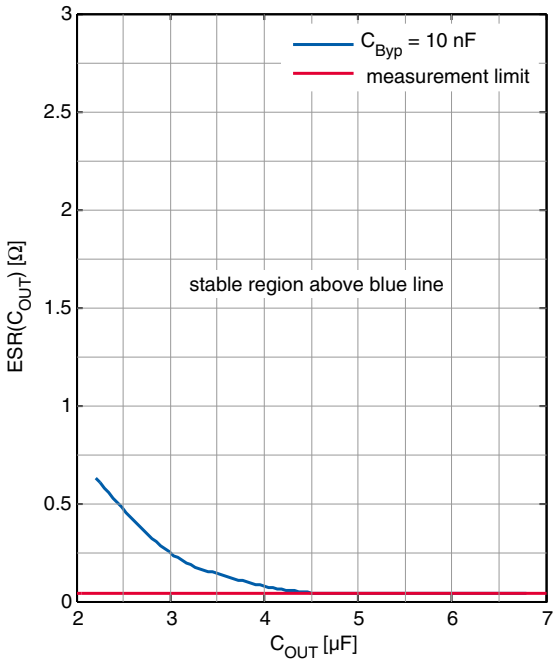


1) V_{IN},min is referred here as the minimum input voltage for which the requested current is provided and V_{OUT} reaches 1 V.

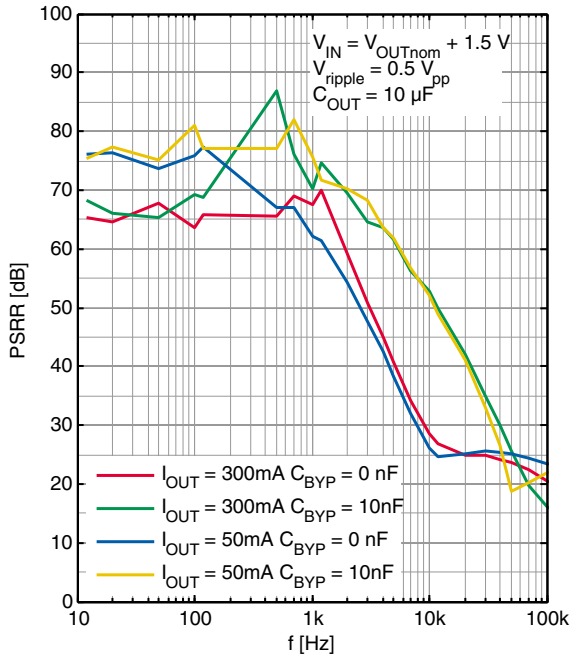
ESR Stability versus Output Current I_{OUT} (for C_{OUT} = 3.3µF)



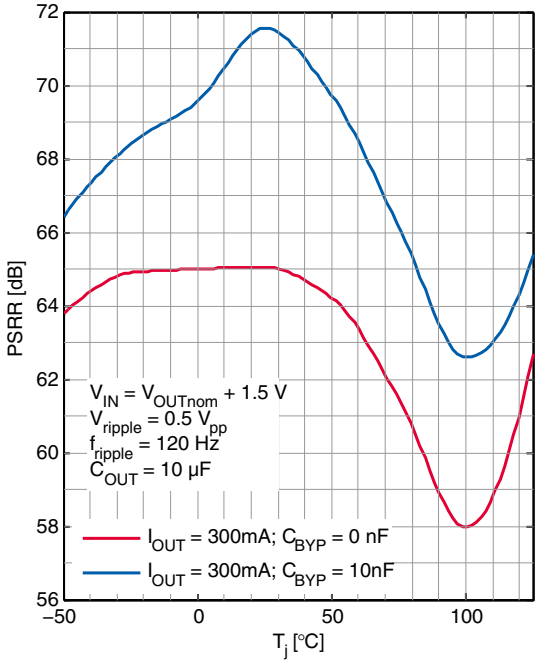
ESR(C_{OUT}) with C_{BYP} = 10 nF versus Output Capacitance C_{OUT}



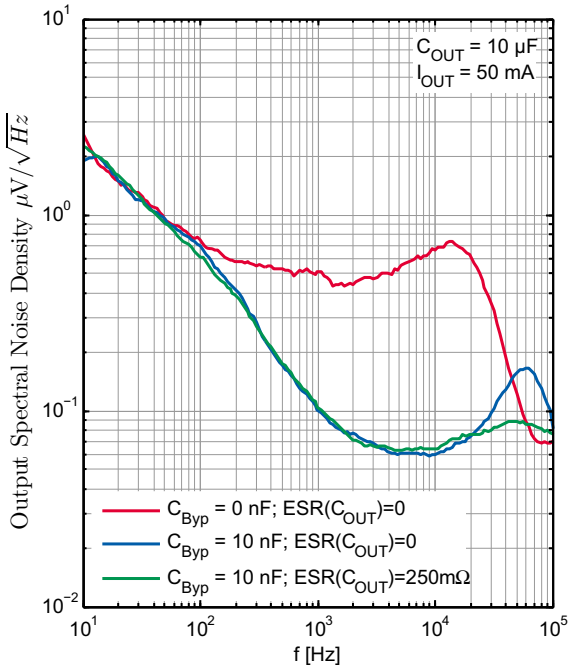
Input Ripple Rejection PSRR versus Frequency f



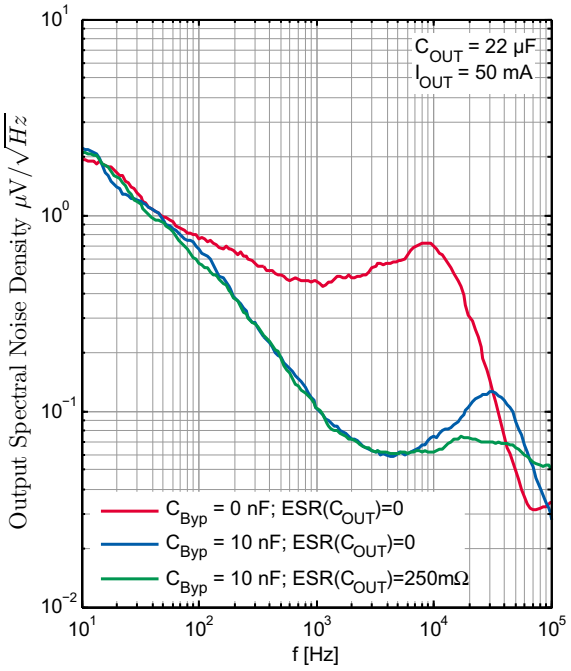
Input Ripple Rejection PSRR versus Junction Temperature T_J



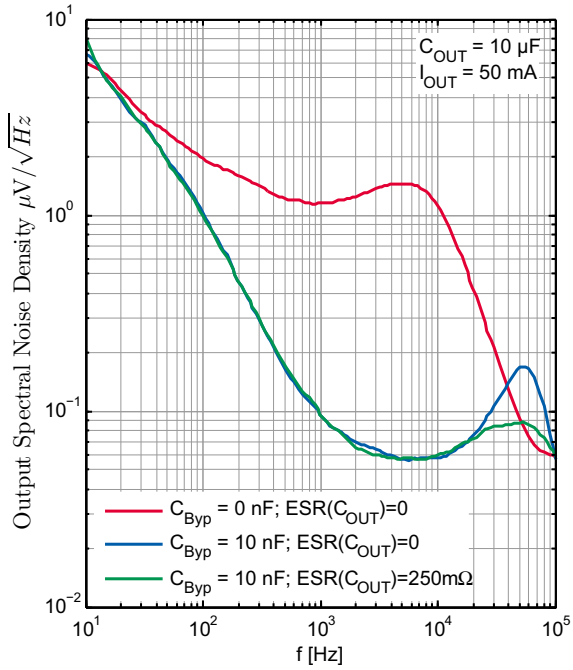
Output Noise Spectral Density (ADJ) versus Frequency (C_{OUT} = 10 µF, I_{OUT} = 50 mA[1])



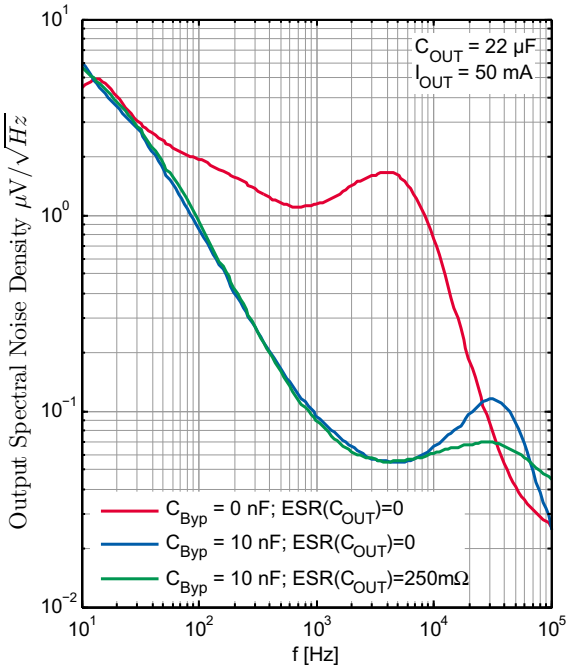
Output Noise Spectral Density (ADJ) versus Frequency (C_{OUT} = 22 µF, I_{OUT} = 50 mA[1])



Output Noise Spectral Density (3.3 V) versus Frequency (C_{OUT} = 10 µF, I_{OUT} = 50 mA[1])

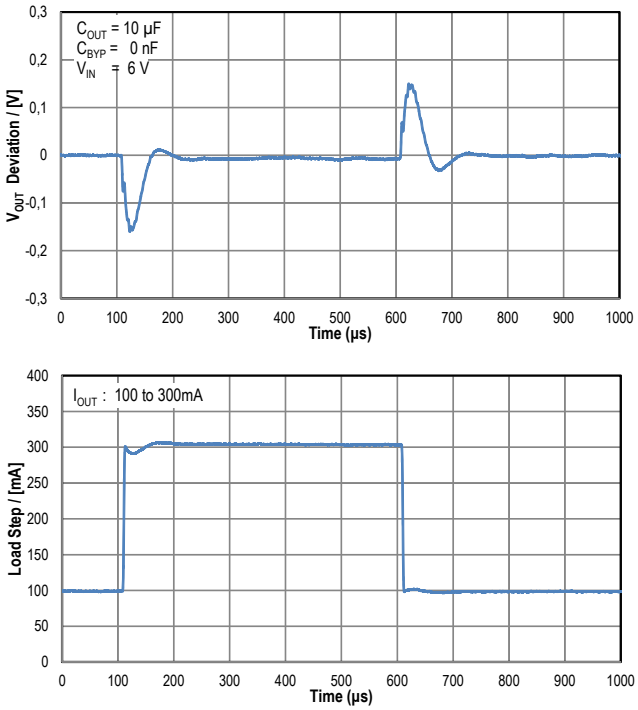


Output Noise Spectral Density (3.3 V) versus Frequency (C_{OUT} = 22 µF, I_{OUT} = 50 mA[1])

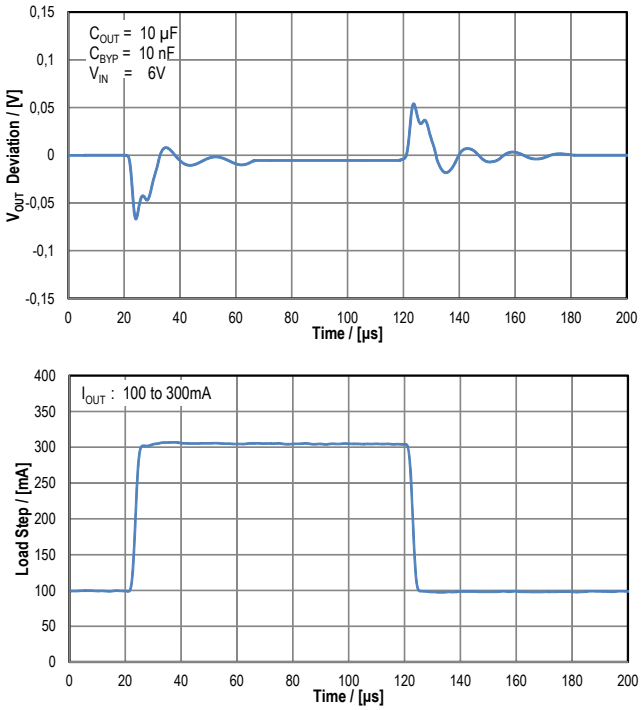


1) Load condition 50 mA is representing a worst case condition with regard to output voltage noise performance.

Transient Response C_{BYP} = 0nF (IFX54441EJV33)



Transient Response C_{BYP} = 10nF (IFX54441EJV33)



7 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

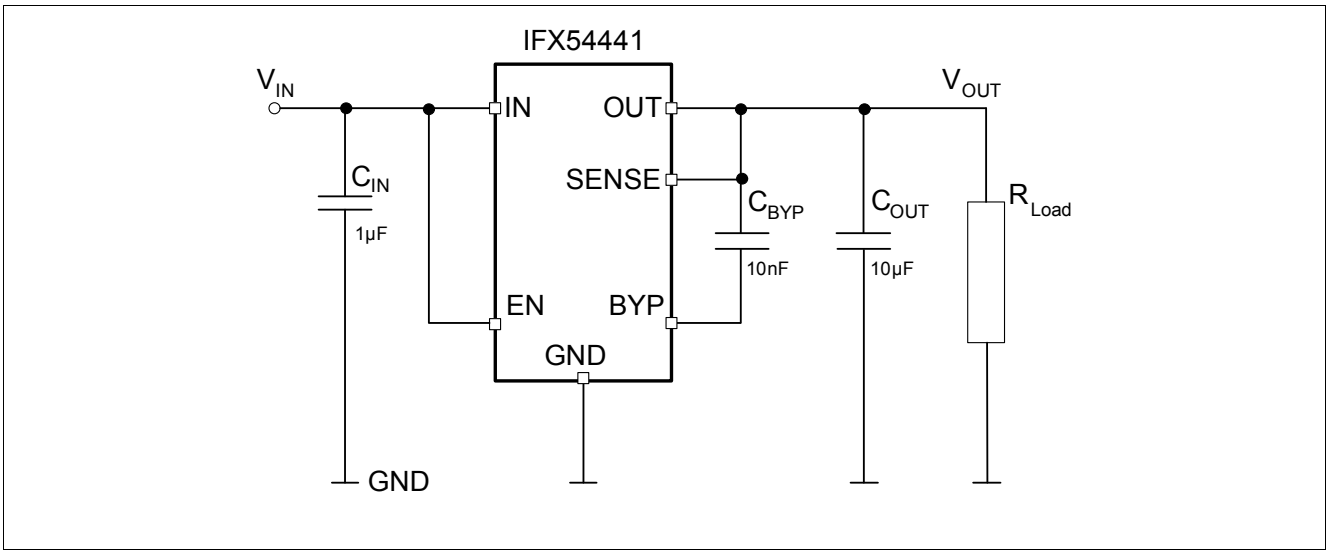


Figure 5 Typical Application Circuit IFX54441 (fixed voltage version)

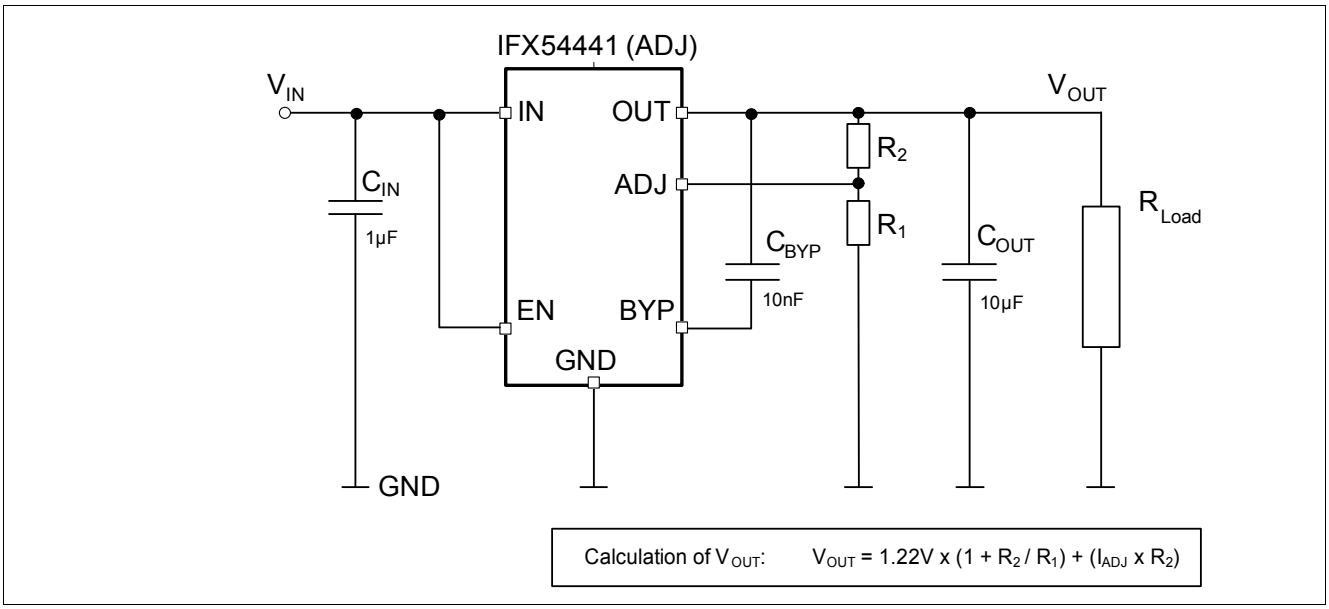


Figure 6 Typical Application Circuit IFX54441 (adjustable version)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application[1)2)].

1) Please note that in case a non-negligible inductance at IN pin is present, e.g. due to long cables, traces, parasitics, etc, a bigger input capacitor C_{IN} may be required to filter its influence. As a rule of thumb if the IN pin is more than six inches away from the main input filter capacitor an input capacitor value of C_{IN} = 10 µF is recommended.

2) For specific needs a small optional resistor may be placed in series to very low ESR output capacitors C_{OUT} for enhanced noise performance (for details please see **"Bypass Capacitance and Low Noise Performance" on Page 25**).

The IFX54441 is a 300 mA low dropout regulator with very low quiescent current and Enable-functionality. The device is capable of supplying 300 mA at a dropout voltage of 270 mV. Output voltage noise numbers down to 24 μV_{RMS} can be achieved over a 10 Hz to 100 kHz bandwidth with the addition of a 10 nF reference bypass capacitor. The usage of a reference bypass capacitor will additionally improve transient response of the regulator, lowering the settling time for transient load conditions. The device has a low operating quiescent current of typical 30 µA that drops to less than 1 µA in shutdown (EN-pin pulled to low level). The device also incorporates several protection features which makes it ideal for battery-powered systems. It is protected against both reverse input and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground the device behaves like it has a diode in series with its output and prevents reverse current flow.

7.1 Adjustable Operation

The adjustable version of the IFX54441 has an output voltage range of 1.22 V to 20 V - V_{DR}. The output voltage is set by the ratio of two external resistors, as it can be seen in **Figure 6** (for the calculation of V_{OUT} the formula given in the figure can be used). The device controls the output to maintain the ADJ pin at 1.22 V referenced to ground. The current in R_1 is then equal 1.22 V / R_1 and the current in R_2 equals the current in R_1 plus the ADJ pin bias current. The ADJ pin bias current, which is ~ 60 nA @ 25°C, flows through R_2 into the ADJ pin. The value of R_1 should be not greater than 250 kΩ in order to minimize errors in the output voltage caused by the ADJ pin bias current. Note that when the device is shutdown (i.e. low level applied to EN pin) the output is turned off and consequently the divider current will be zero. For details of the ADJ pin bias current see also the corresponding typical performance graph **Figure "Adjust Pin Bias current I_{ADJ} versus Junction Temperature T_J" on Page 20**.

7.2 Kelvin Sense Connection

For the fixed voltage version of the IFX54441 the SENSE pin is the input to the error amplifier. An optimum regulation will be obtained at the point where the SENSE pin is connected to the OUT pin of the regulator. In critical applications however small voltage drops can be caused by the resistance R_p of the PC-traces and thus may lower the resulting voltage at the load. This effect may be eliminated by connecting the SENSE pin to the output as close as possible at the load (see **Figure 7**). Please note that the voltage drop across the external PC trace will add up to the dropout voltage of the regulator.

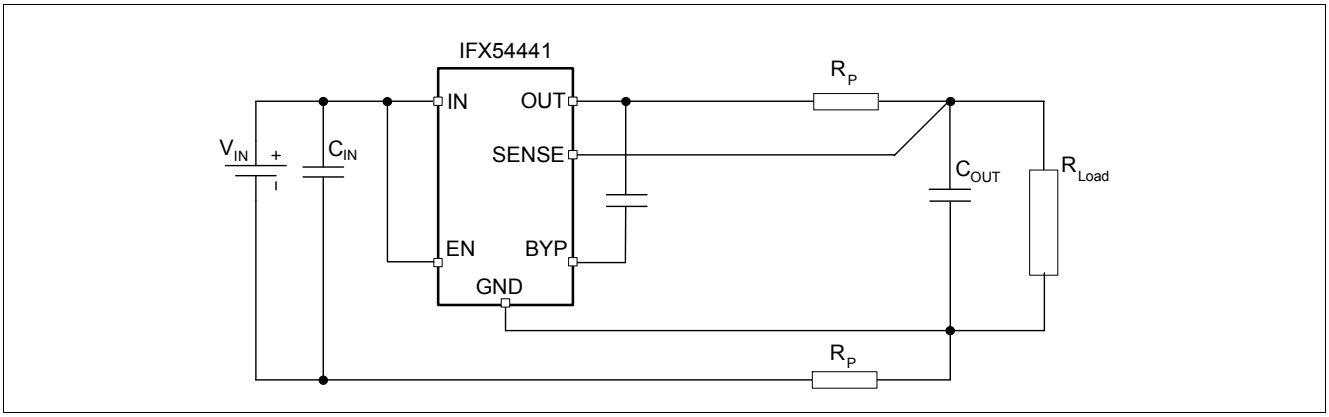


Figure 7 Kelvin Sense Connection

7.3 Bypass Capacitance and Low Noise Performance

The IFX54441 regulator may be used in combination with a bypass capacitor connecting the OUT pin to the BYP pin in order to minimize output voltage noise[1)].This capacitor will bypass the reference of the regulator, providing

1) a good quality low leakage capacitor is recommended.

a low frequency noise pole. The noise pole provided by such a bypass capacitor will lower the output voltage noise in the considered bandwidth. For a given output voltage actual numbers of the output voltage noise will - next to the bypass capacitor itself - be dependent on the capacitance of the applied output capacitor and its ESR: In case of the IFX54441EJV applied with unity gain (i.e. V_{OUT} = 1.22 V) the usage of a bypass capacitor of 10 nF in combination with a (low ESR) ceramic C_{OUT} of 10 µF will result in output voltage noise numbers of typical 41 μV_{RMS}. This Output Noise level can be reduced to typical 28 μV_{RMS} under the same conditions by adding a small resistor of ~250 mΩ in series to the 10 µF ceramic output capacitor acting as additional ESR. A reduction of the output voltage noise can also be achieved by increasing capacitance of the output capacitor. For C_{OUT} = 22 µF (ceramic low ESR) the output voltage noise will be typically around 29 μV_{RMS} and can again be further lowered to 24 μV_{RMS} by adding a small resistance of ~250 mΩ in series to C_{OUT}. In case of the fix voltage version IFX54441EJV33 the output voltage noise for the described cases vary from 45 μV_{RMS} down to 30 μV_{RMS}. For further details please also see **"Output Voltage Noise[11])" on Page 12**,, of the Electrical Characteristics. Please note that next to reducing the output voltage noise level the usage of a bypass capacitor has the additional benefit of improving transient response which will be also explained in the next chapter. However one needs to take into consideration that on the other hand the regulator start-up time is proportional to the size of the bypass capacitor and slows down to values around 15 ms when using a 10 nF bypass capacitor in combination with a 10 µF C_{OUT} output capacitor.

7.4 Output Capacitance Requirements and Transient Response

The IFX54441 is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor is an essential parameter with regard to stability, most notably with small capacitors. A minimum output capacitor of 3.3 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. Like in general for LDO's the output transient response of the IFX54441 will be a function of the output capacitance. Larger values of output capacitance decrease peak deviations and thus improve transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the IFX54441 will increase the effective output capacitor value. Please note that with the usage of bypass capacitors for low noise operation either larger values of output capacitors are needed or a minimum ESR requirement of C_{OUT} may have to be considered (see also **Figure "ESR(C_{OUT}) with C_{BYP} = 10 nF versus Output Capacitance C_{OUT}" on Page 21** as example). In conjunction with the usage of a 10 nF bypass capacitor an output capacitor C_{OUT} ≥ 6.8 µF is recommended. The benefit of a bypass capacitor to the transient response performance is impressive and illustrated as one example in **Figure 8** where the transient response of the IFX54441EJV33 to one and the same load step from 100 mA to 300 mA is shown with and without a 10 nF bypass capacitor: for the given configuration of C_{OUT} = 10 µF with no bypass capacitor the load step will settle in the range of less than 100 µs while for C_{OUT} = 10 µF in conjunction with a 10 nF bypass capacitor the same load step will settle in the range of 10 µs. Due to the shorter reaction time of the regulator by adding the bypass capacitor not only the settling time improves but also output voltage deviations due to load steps are sharply reduced.

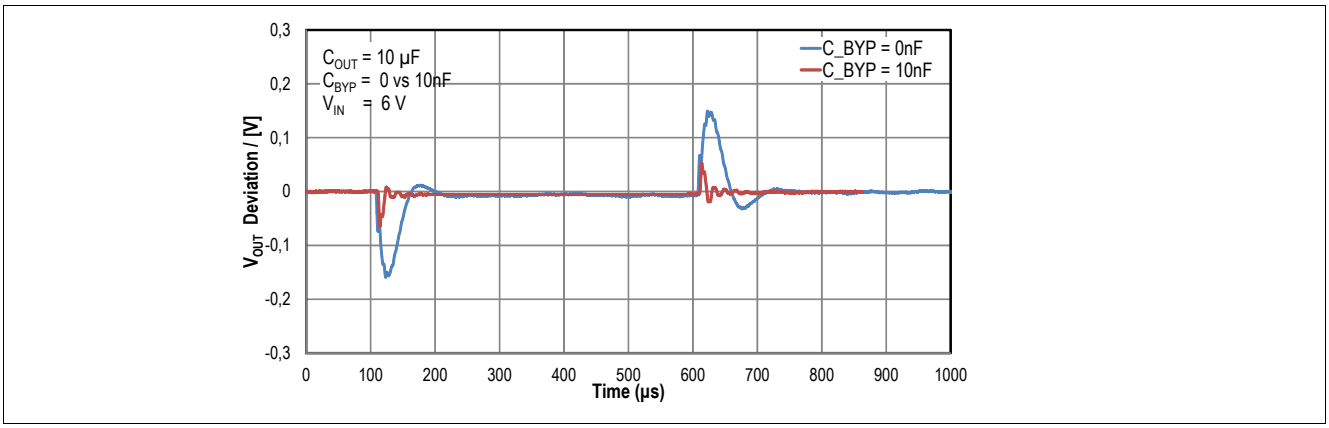


Figure 8 Influence of C_{BYP}: example of transient response to one and the same load step with and without C_{BYP} of 10 nF (I_{OUT} 100 mA to 300 mA, IFX54441EJV33)

7.5 Protection Features

The IFX54441 regulators incorporate several protection features which make them ideal for usage in battery-powered circuits. In addition to normal protection features associated with monolithic regulators like current limiting and thermal limiting the device is protected against reverse input voltage, reverse output voltage and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation the junction temperature must not exceed 125°C.

The input of the device will withstand reverse voltages of 20 V. Current flowing into the device will be limited to less than 1 mA (typically less than 100 µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries being plugged backwards.

The output of the IFX54441 can be pulled below ground without damaging the device. If the input is left open-circuit or grounded, the output can be pulled below ground by 20 V. Under such conditions the output of the device by itself behaves like an open circuit with practically no current flowing out of the pin[1]. In more application relevant cases however where the output is either connected to the SENSE pin (fix voltage variant) or tied either via an external voltage divider or directly to the ADJ pin (adjustable variant) a small current will be present from this origin. In the case of the fixed voltage version this current will typically be below 100 µA while for the adjustable version it depends on the magnitude of the top resistor of the external voltage divider [2]. If the input is powered by a voltage source the output will source the short circuit current of the device and will protect itself by thermal limiting. In this case grounding the EN pin will turn off the device and stop the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is grounded or left open-circuit, the ADJ pin will act inside this voltage range like a large resistor (typically 100 kΩ) when being pulled above ground and like a resistor (typically 5 kΩ) in series with a diode when being pulled below ground. In situations where the ADJ pin is at risk of being pulled outside its absolute maximum ratings ±7 V the ADJ pin current must be limited to 1 mA (e.g. in cases where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7 V clamp voltage). Let's consider for example the case where a resistor divider is used to provide a 1.5 V output from the 1.22 V reference and the output is forced to 20 V. The top resistor of the resistor divider must then be chosen to limit the current into the ADJ pin to 1 mA or less when the ADJ pin is at 7 V. The 13 V difference between output and ADJ pin divided by the 1 mA maximum current into the ADJ pin requires a minimum resistor value of 13 kΩ.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open-circuit. Current flow back into the output will follow the curve as shown in **Figure 9** below.

When the IN pin of the fixed voltage version is forced below the OUT pin, or the OUT pin is pulled above the IN pin, the input current will drop to very small values – typically down to less than 2 µA, once V_{OUT} exceeds V_{IN} by some 300 mV or more. This can happen if the input of the device is connected to a discharged battery and the output is held up by either a backup battery or a second regulator circuit. The state of the EN pin will have no effect on the reverse output current when the output is pulled above the input.

1) typically < 1 µA for the mentioned conditions, V_{OUT} being pulled below ground with other pins either grounded or open.
2) In case there is no external voltage divider applied i.e. the ADJ pin is directly connected to the output and the output is pulled below ground by 20 V the current flowing out of the ADJ pin will be typically ~ 4 mA. Please ensure in such cases that the absolute maximum ratings of the ADJ pin are respected.

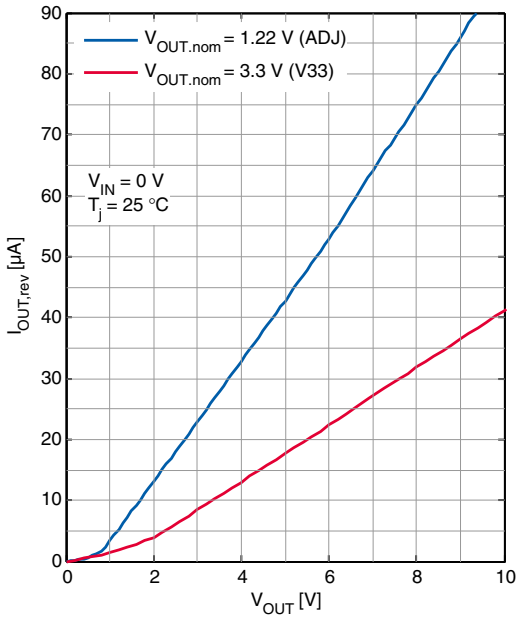


Figure 9 Reverse Output Current

8 Package Outlines

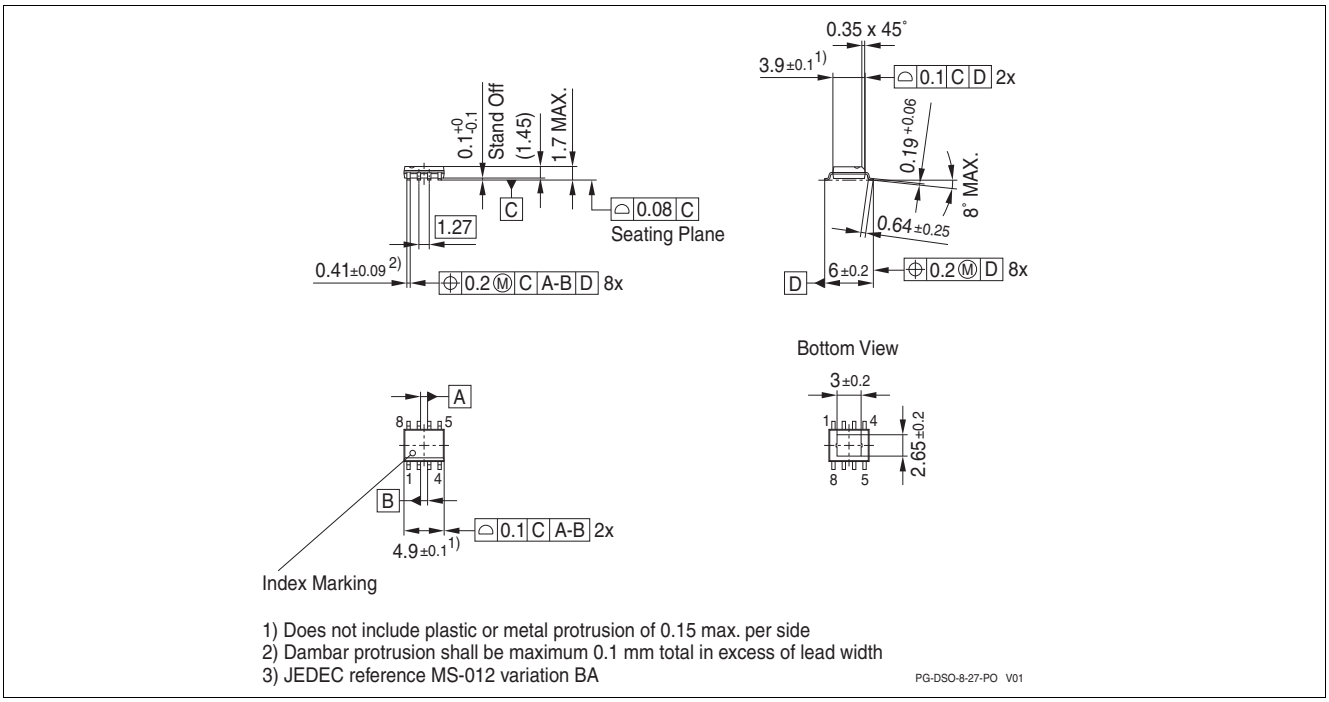


Figure 10 PG-DSO-8 Exposed Pad package outlines

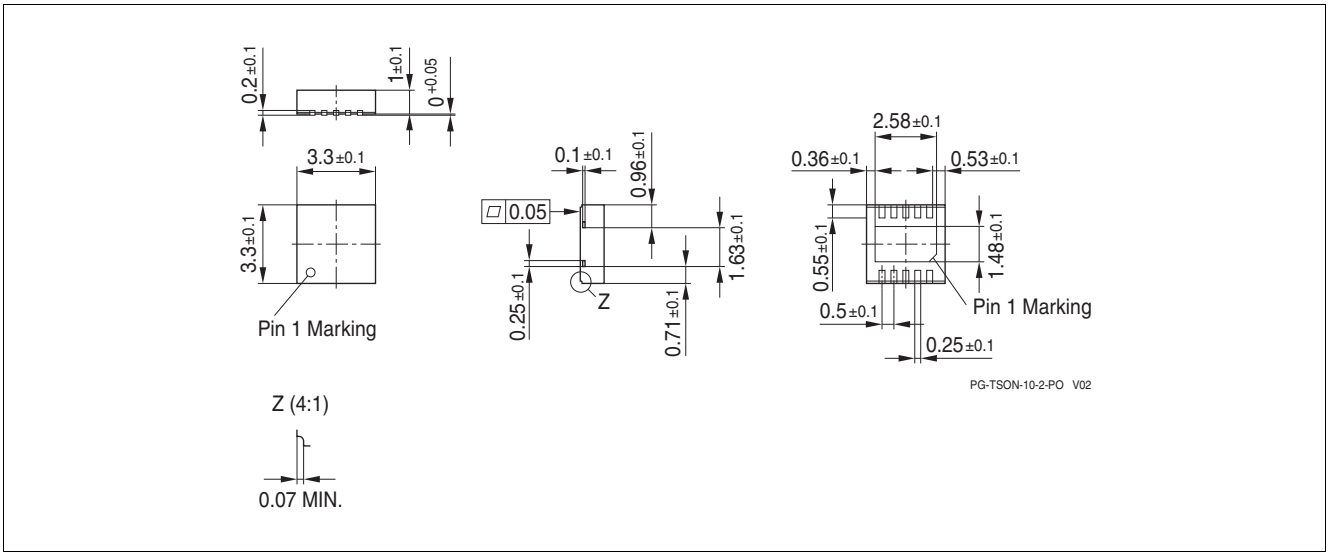


Figure 11 PG-TSON-10 Package Outlines

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision History

Revision	Date	Changes
1.1	2014-10-30	Updated Data Sheet including additional package type PG-TSON-10: • PG-TSON-10 package variants added: Product Overview, Pin Configuration Thermal Resistance, wording, etc, added / updated accordingly. • Footnote 7) on **Page 14** reworked. • Application Information updated: Clarification and correction of wording. Typical values updated and footnotes added. • Editorial changes throughout the document.
1.0	2014-03-12	Data Sheet - Initial Release

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