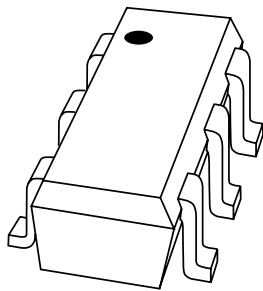


DATA SHEET



PUMD12 NPN/PNP resistor-equipped transistor

Product specification

1999 Apr 26

NPN/PNP resistor-equipped transistor

PUMD12

FEATURES

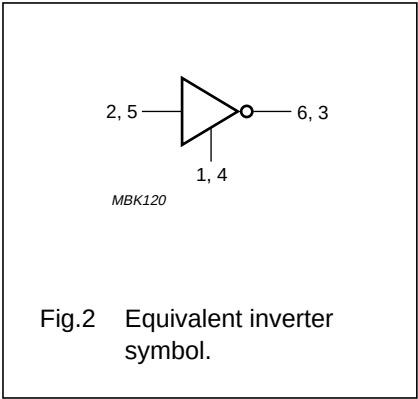
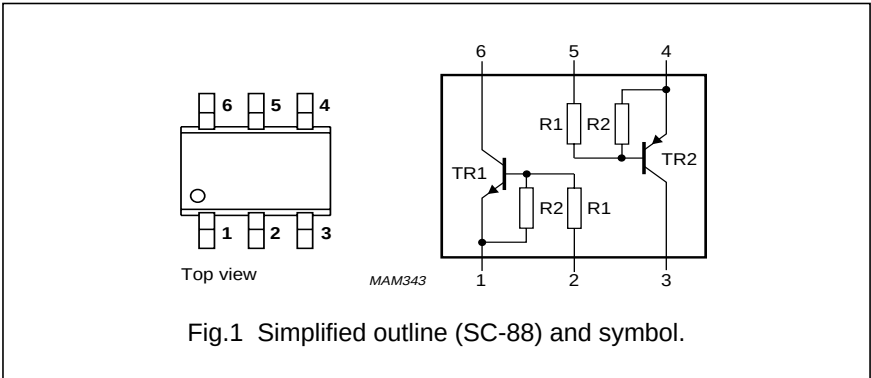
- Transistors with different polarity and built-in bias resistors R1 and R2 (typ. 47 kΩ each)
- No mutual interference between the transistors
- Simplification of circuit design
- Reduces number of components and board space.

APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

DESCRIPTION

NPN/PNP resistor-equipped transistors in an SC-88 plastic package.



PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2

MARKING

TYPE NUMBER	MARKING CODE
PUMD12	Dt1

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage positive negative		–	+40	V
			–	–10	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	–	300	mW

Note

1. Refer to SC-88 standard mounting conditions.

NPN/PNP resistor-equipped transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	416	K/W

Note

1. Refer to SC-88 standard mounting conditions.

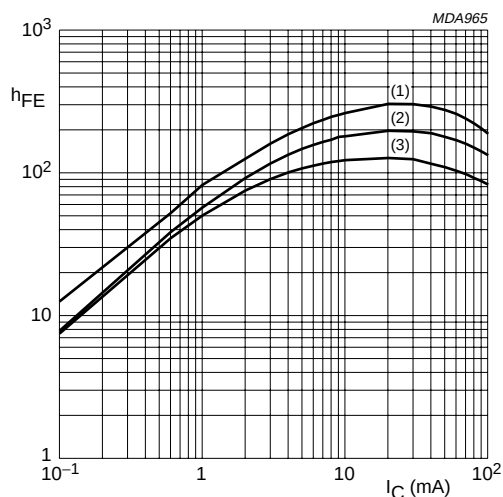
CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = 50\text{ V}$	–	–	100	nA
I_{CEO}	collector cut-off current	$I_B = 0; V_{CE} = 30\text{ V}$	–	–	1	μA
		$I_B = 0; V_{CE} = 30\text{ V}; T_j = 150\text{ °C}$	–	–	50	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	90	μA
h_{FE}	DC current gain	$I_C = 5\text{ mA}; V_{CE} = 5\text{ V}$	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	–	–	150	mV
$V_{i(off)}$	input-off voltage	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}$	–	1.2	0.8	V
$V_{i(on)}$	input-on voltage	$I_C = 2\text{ mA}; V_{CE} = 0.3\text{ V}$	3	1.6	–	V
R1	input resistor		33	47	61	k Ω
$\frac{R_2}{R_1}$	resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$				
	TR1		–	–	2.5	pF
	TR2		–	–	3	pF

NPN/PNP resistor-equipped transistor

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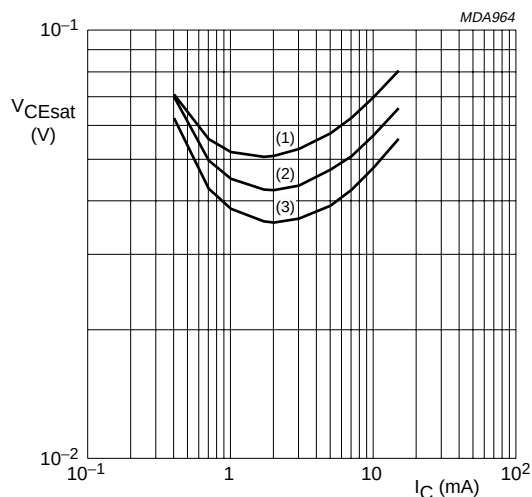
TR1 (NPN); $V_{CE} = 5 \text{ V}$.

(1) $T_{amb} = 150 \text{ }^{\circ}\text{C}$.

(2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

(3) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.

Fig.3 DC current gain as a function of collector current; typical values.



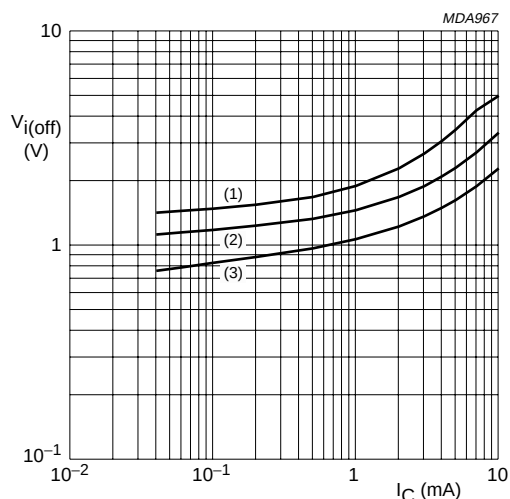
TR1 (NPN); $I_C/I_B = 20$.

(1) $T_{amb} = 100 \text{ }^{\circ}\text{C}$.

(2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

(3) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.

Fig.4 Collector-emitter saturation voltage as a function of collector current; typical values.



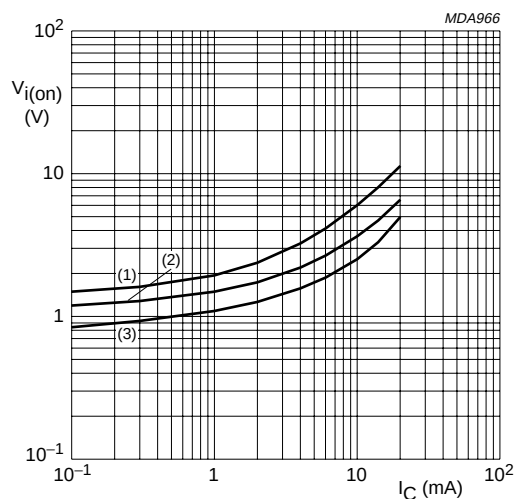
TR1 (NPN); $V_{CE} = 5 \text{ V}$.

(1) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.

(2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

(3) $T_{amb} = 100 \text{ }^{\circ}\text{C}$.

Fig.5 Input-off voltage as a function of collector current; typical values.



TR1 (NPN); $V_{CE} = 0.3 \text{ V}$.

(1) $T_{amb} = -40 \text{ }^{\circ}\text{C}$.

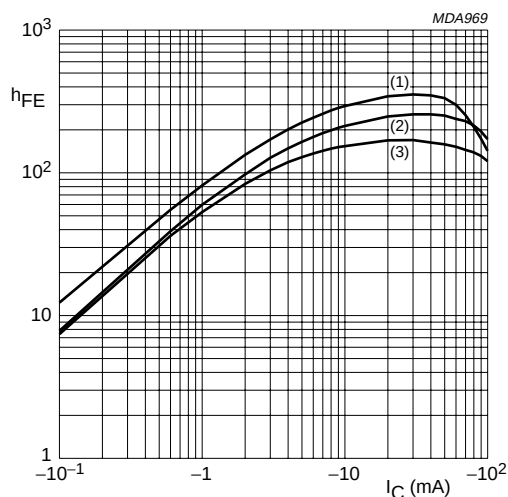
(2) $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

(3) $T_{amb} = 100 \text{ }^{\circ}\text{C}$.

Fig.6 Input-on voltage as a function of collector current; typical values.

NPN/PNP resistor-equipped transistor

PUMD12



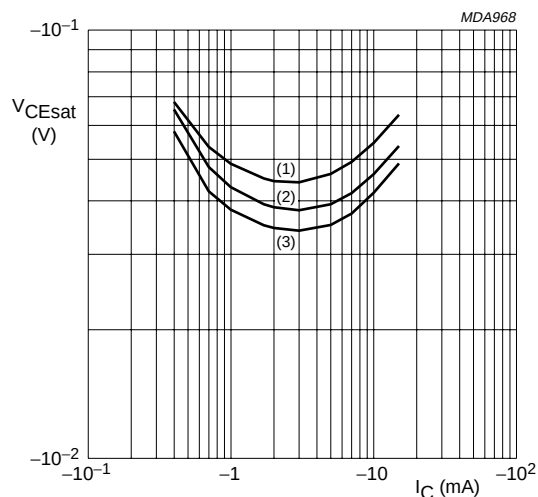
TR2 (PNP); $V_{CE} = -5$ V.

(1) $T_{amb} = 150$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = -40$ °C.

Fig.7 DC current gain as a function of collector current; typical values.



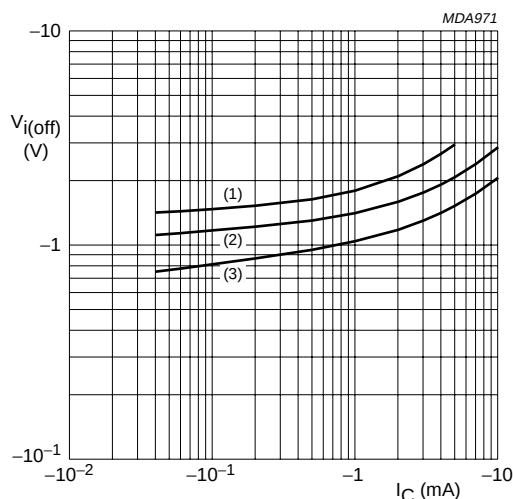
TR2 (PNP); $I_C/I_B = 20$.

(1) $T_{amb} = 100$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = -40$ °C.

Fig.8 Collector-emitter saturation voltage as a function of collector current; typical values.



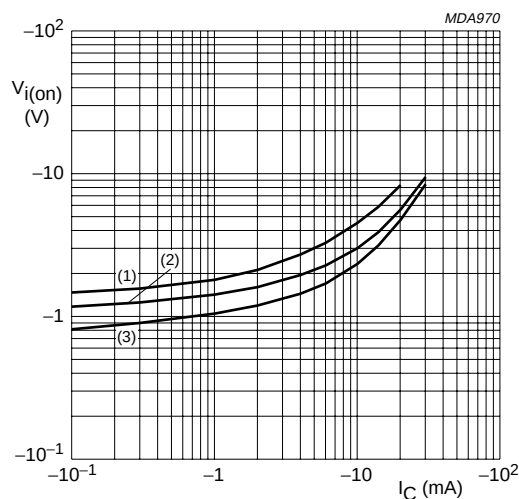
TR2 (PNP); $V_{CE} = -5$ V.

(1) $T_{amb} = -40$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 100$ °C.

Fig.9 Input-off voltage as a function of collector current; typical values.



TR2 (PNP); $V_{CE} = -0.3$ V.

(1) $T_{amb} = -40$ °C.

(2) $T_{amb} = 25$ °C.

(3) $T_{amb} = 100$ °C.

Fig.10 Input-on voltage as a function of collector current; typical values.

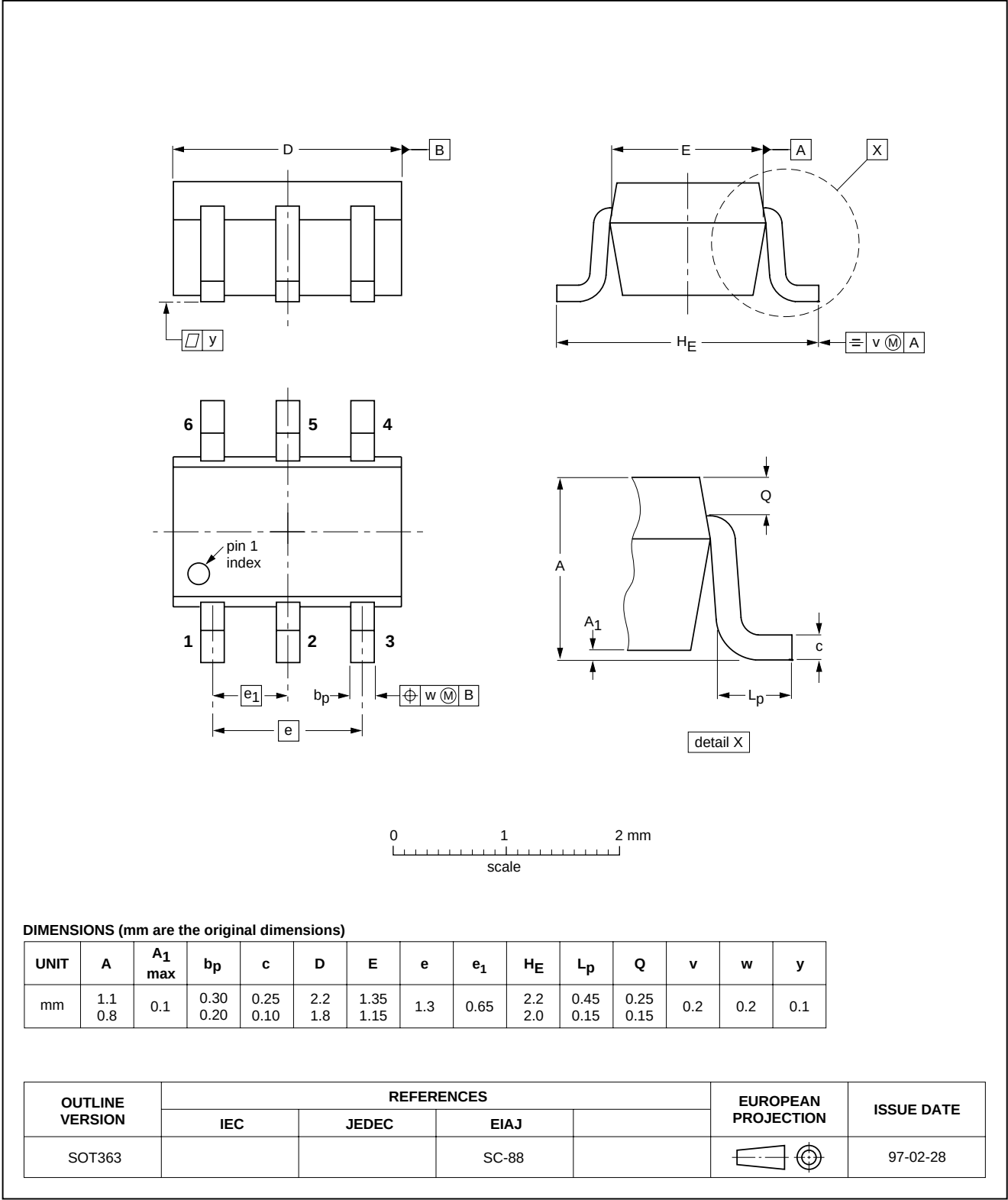
NPN/PNP resistor-equipped transistor

PUMD12

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



NPN/PNP resistor-equipped transistor

PUMD12

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

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Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
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Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

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Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
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United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

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