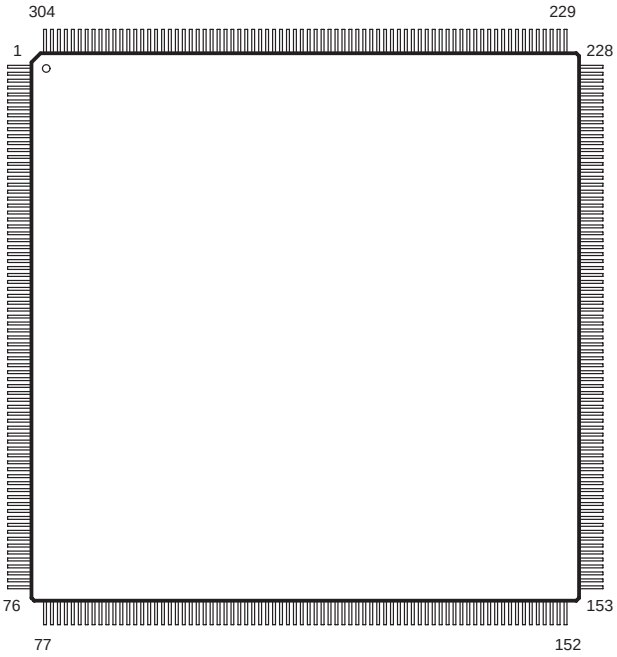
- **Highest Performance Floating-Point Digital Signal Processor (DSP)**
  - **TMS320C44-60: 33-ns Instruction Cycle Time, 330 MOPS, 60 MFLOPS, 30 MIPS, 336M Bytes/s**
  - **TMS320C44-50: 40-ns Instruction Cycle Time**
- **Four Communication Ports**
- **Six-Channel Direct Memory Address (DMA) Coprocessor**
- **Single-Cycle Conversion to and From IEEE-754 Floating-Point Format**
- **Single Cycle, 1/x, $1/\sqrt{x}$**
- **Source-Code Compatible With ’320C3x and ’320C4x**
- **Single-Cycle 40-Bit Floating-Point, 32-Bit Integer Multipliers**
- **Twelve 40-Bit Registers, Eight Auxiliary Registers, 14 Control Registers, and Two Timers**
- **IEEE-1149.1† (JTAG) Boundary-Scan Compatible**
- **Two Identical External Data and Address Buses Supporting Shared Memory Systems and High Data-Rate, Single-Cycle Transfers**
  - **High Port-Data Rate of 120M Bytes/s (TMS320C44-60) (Each Bus)**
  - **128M-Byte Program/Data/Peripheral Address Space**
  - **Memory-Access Request for Fast, Intelligent Bus Arbitration**
  - **Separate Address-Bus, Data-Bus, and Control-Enable Pins**
  - **Four Sets of Memory-Control Signals Support Different Speed Memories in Hardware**
- **304-Pin Plastic Quad Flatpack (PDB Suffix)**
- **Fabricated Using 0.72-μm Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**
- **Separate Internal Program-, Data-, and DMA-Coprocessor Buses for Support of Massive Concurrent I/O of Program and Data, Thereby Maximizing Sustained CPU Performance**

PDB PACKAGE
(TOP VIEW)‡



‡ See Pin Assignments table and Pin Functions table for location and description of all pins.

- **IDLE2 Clock-Stop Power-Down Mode**
- **Communication-Port-Direction Pin**
- **On-Chip Program Cache and Dual-Access/Single-Cycle RAM for Increased Memory-Access Performance**
  - **512-Byte Instruction Cache**
  - **8K Bytes of Single-Cycle Dual-Access Program or Data RAM**
  - **ROM-Based Boot Loader Supports Program Bootup Using 8-, 16-, or 32-Bit Memories or One of the Communication Ports**
- **Software-Communication-Port Reset**
- **$\overline{\text{NMI}}$ With Bus-Grant Feature**

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† IEEE Standard 1149.1–1990 Standard Test-Access Port and Boundary-Scan Architecture
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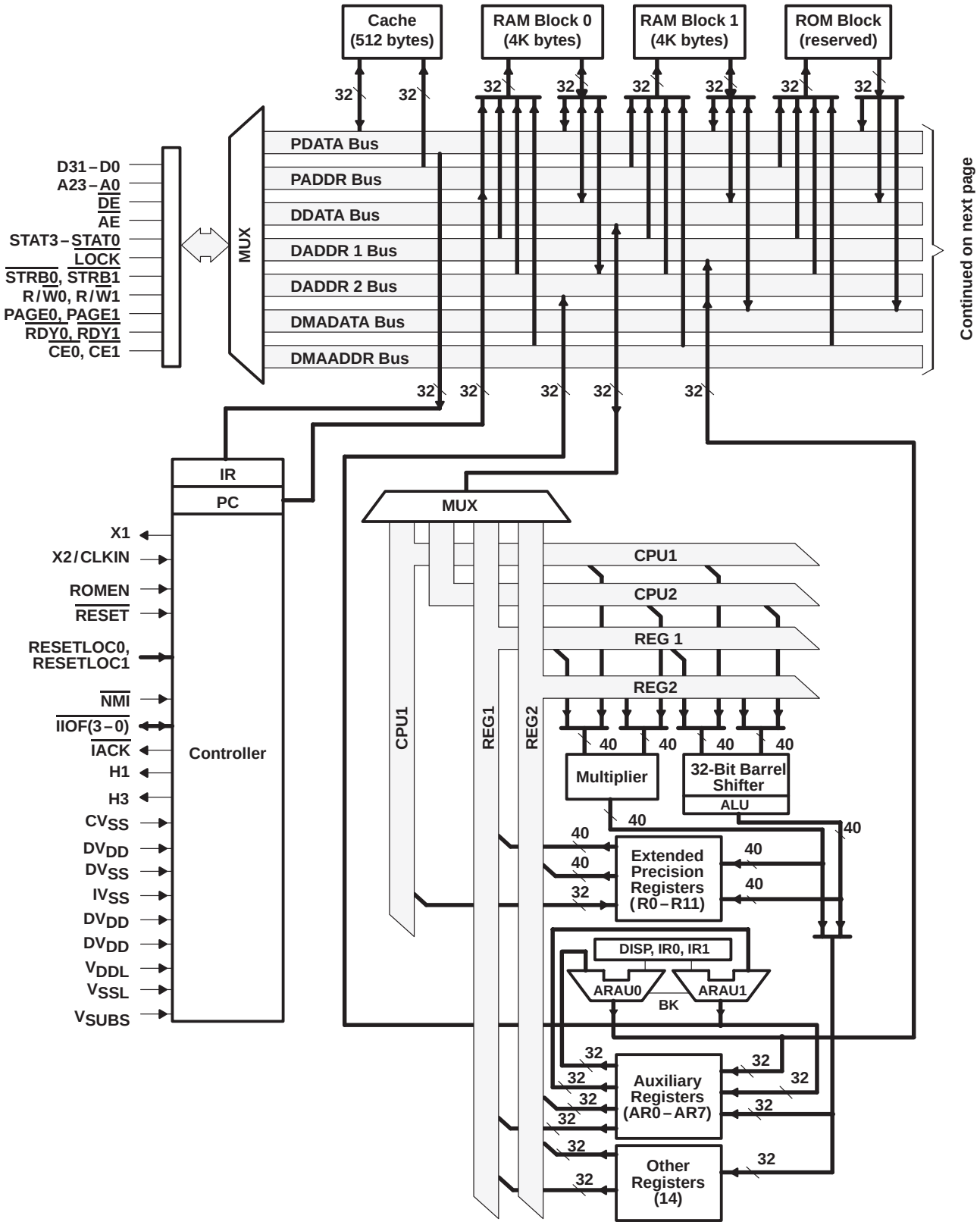
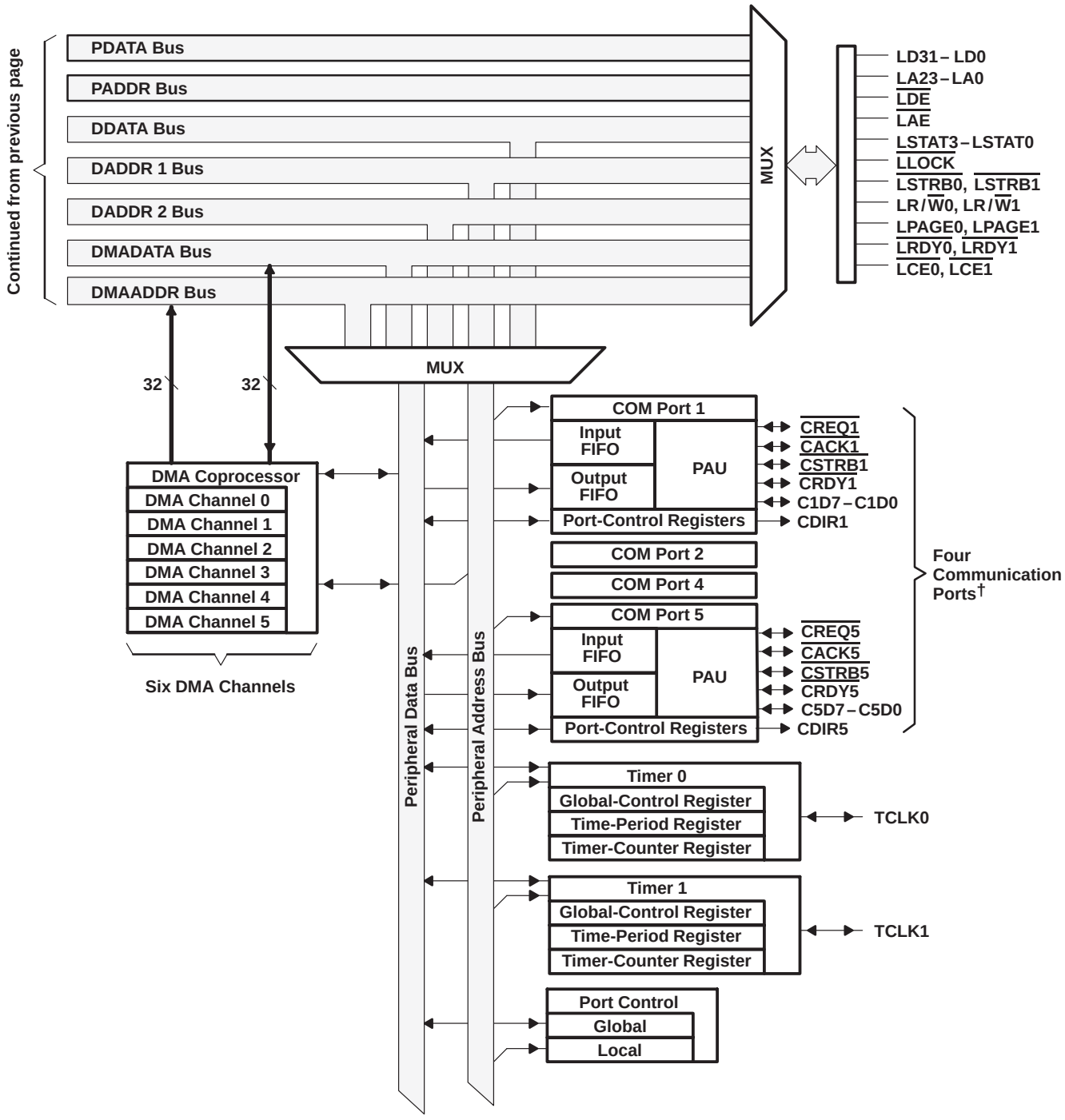
block diagram



block diagram (continued)



† Communication ports 0 and 3 are not connected.

functions

This section lists signal descriptions for the ’320C44 device: each signal, number of pins, operating mode(s) (that is, input, output, or high-impedance state as indicated by I, O, or Z, respectively), and function. The signals are grouped according to function.

Pin Functions

SIGNAL NAME	NO. OF PINS	TYPE†	DESCRIPTION
GLOBAL-BUS EXTERNAL INTERFACE (73 pins)			
D31–D0	32	I/O/Z	32-bit data port of the global-bus external interface
$\overline{\text{DE}}$	1	I	Data-bus-enable signal for the global-bus external interface
A23–A0	24	O/Z	24-bit address port of the global-bus external interface
$\overline{\text{AE}}$	1	I	Address-bus-enable signal for the global-bus external interface
STAT3–STAT0	4	O	Status signals for the global-bus external interface
$\overline{\text{LOCK}}$	1	O	Lock signal for the global-bus external interface
$\overline{\text{STRB0}}$‡	1	O/Z	Access strobe 0 for the global-bus external interface
R/$\overline{\text{W0}}$‡	1	O/Z	Read/write signal for $\overline{\text{STRB0}}$ accesses
PAGE0‡	1	O/Z	Page signal for $\overline{\text{STRB0}}$ accesses
$\overline{\text{RDY0}}$‡	1	I	Ready signal for $\overline{\text{STRB0}}$ accesses
$\overline{\text{CE0}}$‡	1	I	Control enable for the $\overline{\text{STRB0}}$, PAGE0, and R/$\overline{\text{W0}}$ signals
$\overline{\text{STRB1}}$‡	1	O/Z	Access strobe 1 for the global-bus external interface
R/$\overline{\text{W1}}$‡	1	O/Z	Read/write signal for $\overline{\text{STRB1}}$ accesses
PAGE1‡	1	O/Z	Page signal for $\overline{\text{STRB1}}$ accesses
$\overline{\text{RDY1}}$‡	1	I	Ready signal for $\overline{\text{STRB1}}$ accesses
$\overline{\text{CE1}}$‡	1	I	Control enable for the $\overline{\text{STRB1}}$, PAGE1, and R/$\overline{\text{W1}}$ signals
LOCAL-BUS EXTERNAL INTERFACE (73 pins)			
LD31–LD0	32	I/O/Z	32-bit data port of the local-bus external interface
$\overline{\text{LDE}}$	1	I	Data-bus-enable signal for the local-bus external interface
LA23–LA0	24	O/Z	24-bit address port of the local-bus external interface
$\overline{\text{LAE}}$	1	I	Address-bus-enable signal for the local-bus external interface
LSTAT3–LSTAT0	4	O	Status signals for the local-bus external interface
$\overline{\text{LLOCK}}$	1	O	Lock signal for the local-bus external interface
$\overline{\text{LSTRB0}}$‡	1	O/Z	Access strobe 0 for the local-bus external interface
LR/$\overline{\text{W0}}$	1	O/Z	Read/write signal for $\overline{\text{LSTRB0}}$ accesses
LPAGE0	1	O/Z	Page signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LRDY0}}$	1	I	Ready signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LCE0}}$	1	I	Control enable for the $\overline{\text{LSTRB0}}$, LPAGE0, and LR / $\overline{\text{W0}}$ signals
$\overline{\text{LSTRB1}}$‡	1	O/Z	Access strobe 1 for the local-bus external interface
LR/$\overline{\text{W1}}$	1	O/Z	Read/write signal for $\overline{\text{LSTRB1}}$ accesses
LPAGE1	1	O/Z	Page signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LRDY1}}$	1	I	Ready signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LCE1}}$	1	I	Control enable for the $\overline{\text{LSTRB1}}$, LPAGE1, and LR/$\overline{\text{W1}}$ signals

† I = input, O = output, Z = high impedance

‡ The effective address range is defined by the local/global $\overline{\text{STRB}}$ ACTIVE bits in the memory interface-control registers.

Pin Functions (Continued)

SIGNAL NAME	NO. OF PINS	TYPE†	DESCRIPTION
COMMUNICATION PORT 1 INTERFACE (13 pins)			
C1D7–C1D0	8	I/O	Communication port 1 data bus
$\overline{\text{CREQ1}}$	1	I/O	Communication port 1 token-request signal
$\overline{\text{CACK1}}$	1	I/O	Communication port 1 token-request-acknowledge signal
$\overline{\text{CSTRB1}}$	1	I/O	Communication port 1 data-strobe signal
$\overline{\text{CRDY1}}$	1	I/O	Communication port 1 data-ready signal
CDIR1	1	O	Communication port 1 direction signal
COMMUNICATION PORT 2 INTERFACE (13 pins)			
C2D7–C2D0	8	I/O	Communication port 2 data bus
$\overline{\text{CREQ2}}$	1	I/O	Communication port 2 token-request signal
$\overline{\text{CACK2}}$	1	I/O	Communication port 2 token-request-acknowledge signal
$\overline{\text{CSTRB2}}$	1	I/O	Communication port 2 data-strobe signal
$\overline{\text{CRDY2}}$	1	I/O	Communication port 2 data-ready signal
CDIR2	1	O	Communication port 2 direction signal
COMMUNICATION PORT 4 INTERFACE (13 pins)			
C4D7–C4D0	8	I/O	Communication port 4 data bus
$\overline{\text{CREQ4}}$	1	I/O	Communication port 4 token-request signal
$\overline{\text{CACK4}}$	1	I/O	Communication port 4 token-request-acknowledge signal
$\overline{\text{CSTRB4}}$	1	I/O	Communication port 4 data-strobe signal
$\overline{\text{CRDY4}}$	1	I/O	Communication port 4 data-ready signal
CDIR4	1	O	Communication port 4 direction signal
COMMUNICATION PORT 5 INTERFACE (13 pins)			
C5D7–C5D0	8	I/O	Communication port 5 data bus
$\overline{\text{CREQ5}}$	1	I/O	Communication port 5 token-request signal
$\overline{\text{CACK5}}$	1	I/O	Communication port 5 token-request-acknowledge signal
$\overline{\text{CSTRB5}}$	1	I/O	Communication port 5 data-strobe signal
$\overline{\text{CRDY5}}$	1	I/O	Communication port 5 data-ready signal
CDIR5	1	O	Communication port 5 direction signal
INTERRUPTS, I/O FLAGS, RESET, TIMER (12 pins)			
$\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$	4	I/O	Interrupt and I/O flags
$\overline{\text{NMI}}$	1	I	Nonmaskable interrupt. $\overline{\text{NMI}}$ is sensitive to a low-going edge.
$\overline{\text{IACK}}$	1	O	Interrupt acknowledge
$\overline{\text{RESET}}$	1	I	Reset signal
RESETLOC1 RESETLOC0	2	I	Reset-vector location
ROMEN	1	I	On-chip ROM enable (0 = disable, 1 = enable)
TCLK0	1	I/O	Timer 0
TCLK1	1	I/O	Timer 1

† I = input, O = output, Z = high impedance

Pin Functions (Continued)

SIGNAL NAME	NO. OF PINS	TYPE†	DESCRIPTION
CLOCK (4 pins)			
X1	1	O	Crystal
X2 / CLKIN	1	I	Crystal/oscillator
H1	1	O	H1 clock
H3	1	O	H3 clock
POWER (71 pins)			
CV_{SS}	17	I	Ground
DV_{SS}	17	I	Ground
IV_{SS}	6	I	Ground
DV_{DD}	22	I	5-V_{DC} supply
VSUBS	1	I	Substrate (tie to ground)
V_{DDL}	4	I	5-V_{DC} supply
V_{SSL}	4	I	Ground
EMULATION (7 pins)			
TCK	1	I	IEEE 1149.1 test port clock
TDI	1	I	IEEE 1149.1 test port data in
TDO	1	O/Z	IEEE 1149.1 test port data out
TMS	1	I	IEEE 1149.1 test port mode select
$\overline{TRST}$	1	I	IEEE 1149.1 test port reset
EMU0	1	I/O	Emulation pin 0
EMU1	1	I/O	Emulation pin 1

† I = input, O = output, Z = high impedance

PDB Package Pin Assignments — Alphabetical Listing

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
A0	149	C2D7	34	CV_{SS}	134	D24	137
A1	150	C4D0	87	CV_{SS}	117	D25	138
A2	151	C4D1	88	CV_{SS}	102	D26	140
A3	152	C4D2	90	CV_{SS}	78	D27	141
A4	154	C4D3	92	CV_{SS}	62	D28	142
A5	155	C4D4	94	CV_{SS}	44	D29	143
A6	156	C4D5	97	CV_{SS}	25	D30	144
A7	157	C4D6	99	CV_{SS}	7	D31	145
A8	158	C4D7	100	CV_{SS}	282	$\overline{DE}$	89
A9	159	C5D0	37	CV_{SS}	262	DV_{DD}	139
A10	160	C5D1	39	CV_{SS}	247	DV_{DD}	124
A11	162	C5D2	41	CV_{SS}	230	DV_{DD}	109
A12	165	C5D3	42	CV_{SS}	218	DV_{DD}	96
A13	166	C5D4	45	CV_{SS}	202	DV_{DD}	83
A14	167	C5D5	46	CV_{SS}	182	DV_{DD}	67
A15	168	C5D6	47	CV_{SS}	164	DV_{DD}	51
A16	169	C5D7	48	D0	104	DV_{DD}	40
A17	170	$\overline{CACK1}$	13	D1	105	DV_{DD}	28
A18	171	$\overline{CACK2}$	21	D2	106	DV_{DD}	17
A19	174	$\overline{CACK4}$	73	D3	107	DV_{DD}	302
A20	175	$\overline{CACK5}$	50	D4	108	DV_{DD}	288
A21	176	CDIR1	19	D5	110	DV_{DD}	272
A22	177	CDIR2	18	D6	111	DV_{DD}	256
A23	178	CDIR4	16	D7	112	DV_{DD}	244
$\overline{AE}$	57	CDIR5	15	D8	113	DV_{DD}	236
C1D0	269	$\overline{CE0}$	93	D9	114	DV_{DD}	223
C1D1	271	$\overline{CE1}$	101	D10	115	DV_{DD}	207
C1D2	274	$\overline{CRDY1}$	8	D11	118	DV_{DD}	188
C1D3	276	$\overline{CRDY2}$	23	D12	120	DV_{DD}	172
C1D4	278	$\overline{CRDY4}$	85	D13	122	DV_{DD}	161
C1D5	280	$\overline{CRDY5}$	53	D14	123	DV_{DD}	153
C1D6	283	$\overline{CREQ1}$	11	D15	125	DV_{SS}	147
C1D7	286	$\overline{CREQ2}$	20	D16	127	DV_{SS}	133
C2D0	26	$\overline{CREQ4}$	71	D17	128	DV_{SS}	116
C2D1	27	$\overline{CREQ5}$	49	D18	129	DV_{SS}	103
C2D2	29	$\overline{CSTRB1}$	14	D19	130	DV_{SS}	79
C2D3	30	$\overline{CSTRB2}$	22	D20	131	DV_{SS}	63
C2D4	31	$\overline{CSTRB4}$	84	D21	132	DV_{SS}	43
C2D5	32	$\overline{CSTRB5}$	52	D22	135	DV_{SS}	24
C2D6	33	CV_{SS}	148	D23	136	DV_{SS}	6

PDB Package Pin Assignments — Alphabetical Listing (Continued)

PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.
DV_{SS}	281	LA17	253	LD30	228	STAT0	68
DV_{SS}	261	LA18	254	LD31	229	STAT1	66
DV_{SS}	246	LA19	255	$\overline{LDE}$	291	STAT2	64
DV_{SS}	231	LA20	257	$\overline{LLOCK}$	284	STAT3	61
DV_{SS}	217	LA21	258	$\overline{LOCK}$	95	$\overline{STRB0}$	58
DV_{SS}	201	LA22	259	LPAGE0	299	$\overline{STRB1}$	69
DV_{SS}	179	LA23	260	LPAGE1	294	TCK	86
DV_{SS}	163	$\overline{LAE}$	287	$\overline{LRDY0}$	298	TCLK0	290
EMU0	75	$\overline{LCE0}$	297	$\overline{LRDY1}$	293	TCLK1	289
EMU1	74	$\overline{LCE1}$	292	LR/$\overline{W0}$	300	TDI	76
H1	266	LD0	183	LR/$\overline{W1}$	295	TDO	80
H3	268	LD1	184	LSTAT0	279	TMS	82
$\overline{IACK}$	270	LD2	185	LSTAT1	277	$\overline{TRST}$	81
$\overline{IIOF0}$	10	LD3	186	LSTAT2	275	V_{DDL}	38
$\overline{IIOF1}$	9	LD4	187	LSTAT3	273	V_{DDL}	121
$\overline{IIOF2}$	5	LD5	192	$\overline{LSTRB0}$	301	V_{DDL}	191
$\overline{IIOF3}$	4	LD6	194	$\overline{LSTRB1}$	296	V_{DDL}	267
IV_{SS}	126	LD7	195	NC	1	V_{SSL}	36
IV_{SS}	65	LD8	196	NC	77	V_{SSL}	119
IV_{SS}	35	LD9	197	NC	173	V_{SSL}	193
IV_{SS}	2	LD10	200	NC	180	V_{SSL}	265
IV_{SS}	285	LD11	203	NC	181	VSUBS	146
IV_{SS}	209	LD12	204	NC	189	X1	264
LA0	232	LD13	205	NC	190	X2/CLKIN	263
LA1	233	LD14	206	NC	198		
LA2	234	LD15	208	NC	199		
LA3	235	LD16	210	NC	214		
LA4	237	LD17	211	NC	303		
LA5	238	LD18	212	NC	304		
LA6	239	LD19	213	$\overline{NMI}$	3		
LA7	240	LD20	215	PAGE0	60		
LA8	241	LD21	216	PAGE1	72		
LA9	242	LD22	219	$\overline{RDY0}$	91		
LA10	243	LD23	220	$\overline{RDY1}$	98		
LA11	245	LD24	221	$\overline{RESET}$	54		
LA12	248	LD25	222	RESETLOC0	55		
LA13	249	LD26	224	RESETLOC1	56		
LA14	250	LD27	225	ROMEN	12		
LA15	251	LD28	226	R/$\overline{W0}$	59		
LA16	252	LD29	227	R/$\overline{W1}$	70		

PDB Package Pin Assignments — Numerical Listing

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	NC	41	C5D2	81	$\overline{\text{TRST}}$	121	V_{DDL}
2	IV_{SS}	42	C5D3	82	TMS	122	D13
3	$\overline{\text{NMI}}$	43	DV_{SS}	83	DV_{DD}	123	D14
4	$\overline{\text{IIOF3}}$	44	CV_{SS}	84	$\overline{\text{CSTRB4}}$	124	DV_{DD}
5	$\overline{\text{IIOF2}}$	45	C5D4	85	$\overline{\text{CRDY4}}$	125	D15
6	DV_{SS}	46	C5D5	86	TCK	126	IV_{SS}
7	CV_{SS}	47	C5D6	87	C4D0	127	D16
8	$\overline{\text{CRDY1}}$	48	C5D7	88	C4D1	128	D17
9	$\overline{\text{IIOF1}}$	49	$\overline{\text{CREQ5}}$	89	$\overline{\text{DE}}$	129	D18
10	$\overline{\text{IIOF0}}$	50	$\overline{\text{CACK5}}$	90	C4D2	130	D19
11	$\overline{\text{CREQ1}}$	51	DV_{DD}	91	$\overline{\text{RDY0}}$	131	D20
12	ROMEN	52	$\overline{\text{CSTRB5}}$	92	C4D3	132	D21
13	$\overline{\text{CACK1}}$	53	$\overline{\text{CRDY5}}$	93	$\overline{\text{CE0}}$	133	DV_{SS}
14	$\overline{\text{CSTRB1}}$	54	$\overline{\text{RESET}}$	94	C4D4	134	CV_{SS}
15	CDIR5	55	RESETLOC0	95	$\overline{\text{LOCK}}$	135	D22
16	CDIR4	56	RESETLOC1	96	DV_{DD}	136	D23
17	DV_{DD}	57	$\overline{\text{AE}}$	97	C4D5	137	D24
18	CDIR2	58	$\overline{\text{STRB0}}$	98	$\overline{\text{RDY1}}$	138	D25
19	CDIR1	59	R / $\overline{\text{W0}}$	99	C4D6	139	DV_{DD}
20	$\overline{\text{CREQ2}}$	60	PAGE0	100	C4D7	140	D26
21	$\overline{\text{CACK2}}$	61	STAT3	101	$\overline{\text{CE1}}$	141	D27
22	$\overline{\text{CSTRB2}}$	62	CV_{SS}	102	CV_{SS}	142	D28
23	$\overline{\text{CRDY2}}$	63	DV_{SS}	103	DV_{SS}	143	D29
24	DV_{SS}	64	STAT2	104	D0	144	D30
25	CV_{SS}	65	IV_{SS}	105	D1	145	D31
26	C2D0	66	STAT1	106	D2	146	VSUBS
27	C2D1	67	DV_{DD}	107	D3	147	DV_{SS}
28	DV_{DD}	68	STAT0	108	D4	148	CV_{SS}
29	C2D2	69	$\overline{\text{STRB1}}$	109	DV_{DD}	149	A0
30	C2D3	70	R / $\overline{\text{W1}}$	110	D5	150	A1
31	C2D4	71	$\overline{\text{CREQ4}}$	111	D6	151	A2
32	C2D5	72	PAGE1	112	D7	152	A3
33	C2D6	73	$\overline{\text{CACK4}}$	113	D8	153	DV_{DD}
34	C2D7	74	EMU1	114	D9	154	A4
35	IV_{SS}	75	EMU0	115	D10	155	A5
36	V_{SSL}	76	TDI	116	DV_{SS}	156	A6
37	C5D0	77	NC	117	CV_{SS}	157	A7
38	V_{DDL}	78	CV_{SS}	118	D11	158	A8
39	C5D1	79	DV_{SS}	119	V_{SSL}	159	A9
40	DV_{DD}	80	TDO	120	D12	160	A10

PDB Package Pin Assignments — Numerical Listing (Continued)

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
161	DV_{DD}	201	DV_{SS}	241	LA8	281	DV_{SS}
162	A11	202	CV_{SS}	242	LA9	282	CV_{SS}
163	DV_{SS}	203	LD11	243	LA10	283	C1D6
164	CV_{SS}	204	LD12	244	DV_{DD}	284	$\overline{\text{LLOCK}}$
165	A12	205	LD13	245	LA11	285	IV_{SS}
166	A13	206	LD14	246	DV_{SS}	286	C1D7
167	A14	207	DV_{DD}	247	CV_{SS}	287	$\overline{\text{LAE}}$
168	A15	208	LD15	248	LA12	288	DV_{DD}
169	A16	209	IV_{SS}	249	LA13	289	TCLK1
170	A17	210	LD16	250	LA14	290	TCLK0
171	A18	211	LD17	251	LA15	291	$\overline{\text{LDE}}$
172	DV_{DD}	212	LD18	252	LA16	292	$\overline{\text{LCE1}}$
173	NC	213	LD19	253	LA17	293	$\overline{\text{LRDY1}}$
174	A19	214	NC	254	LA18	294	LPAGE1
175	A20	215	LD20	255	LA19	295	LR / $\overline{\text{W1}}$
176	A21	216	LD21	256	DV_{DD}	296	$\overline{\text{LSTRB1}}$
177	A22	217	DV_{SS}	257	LA20	297	$\overline{\text{LCE0}}$
178	A23	218	CV_{SS}	258	LA21	298	$\overline{\text{LRDY0}}$
179	DV_{SS}	219	LD22	259	LA22	299	LPAGE0
180	NC	220	LD23	260	LA23	300	LR / $\overline{\text{W0}}$
181	NC	221	LD24	261	DV_{SS}	301	$\overline{\text{LSTRB0}}$
182	CV_{SS}	222	LD25	262	CV_{SS}	302	DV_{DD}
183	LD0	223	DV_{DD}	263	X2 / CLKIN	303	NC
184	LD1	224	LD26	264	X1	304	NC
185	LD2	225	LD27	265	V_{SSL}		
186	LD3	226	LD28	266	H1		
187	LD4	227	LD29	267	V_{DDL}		
188	DV_{DD}	228	LD30	268	H3		
189	NC	229	LD31	269	C1D0		
190	NC	230	CV_{SS}	270	$\overline{\text{IACK}}$		
191	V_{DDL}	231	DV_{SS}	271	C1D1		
192	LD5	232	LA0	272	DV_{DD}		
193	V_{SSL}	233	LA1	273	LSTAT3		
194	LD6	234	LA2	274	C1D2		
195	LD7	235	LA3	275	LSTAT2		
196	LD8	236	DV_{DD}	276	C1D3		
197	LD9	237	LA4	277	LSTAT1		
198	NC	238	LA5	278	C1D4		
199	NC	239	LA6	279	LSTAT0		
200	LD10	240	LA7	280	C1D5		

memory map

Figure 1 shows the memory map for the ’320C44. Refer to the *TMS320C4x User’s Guide* (literature number SPRU063B) for a detailed description of this memory mapping.

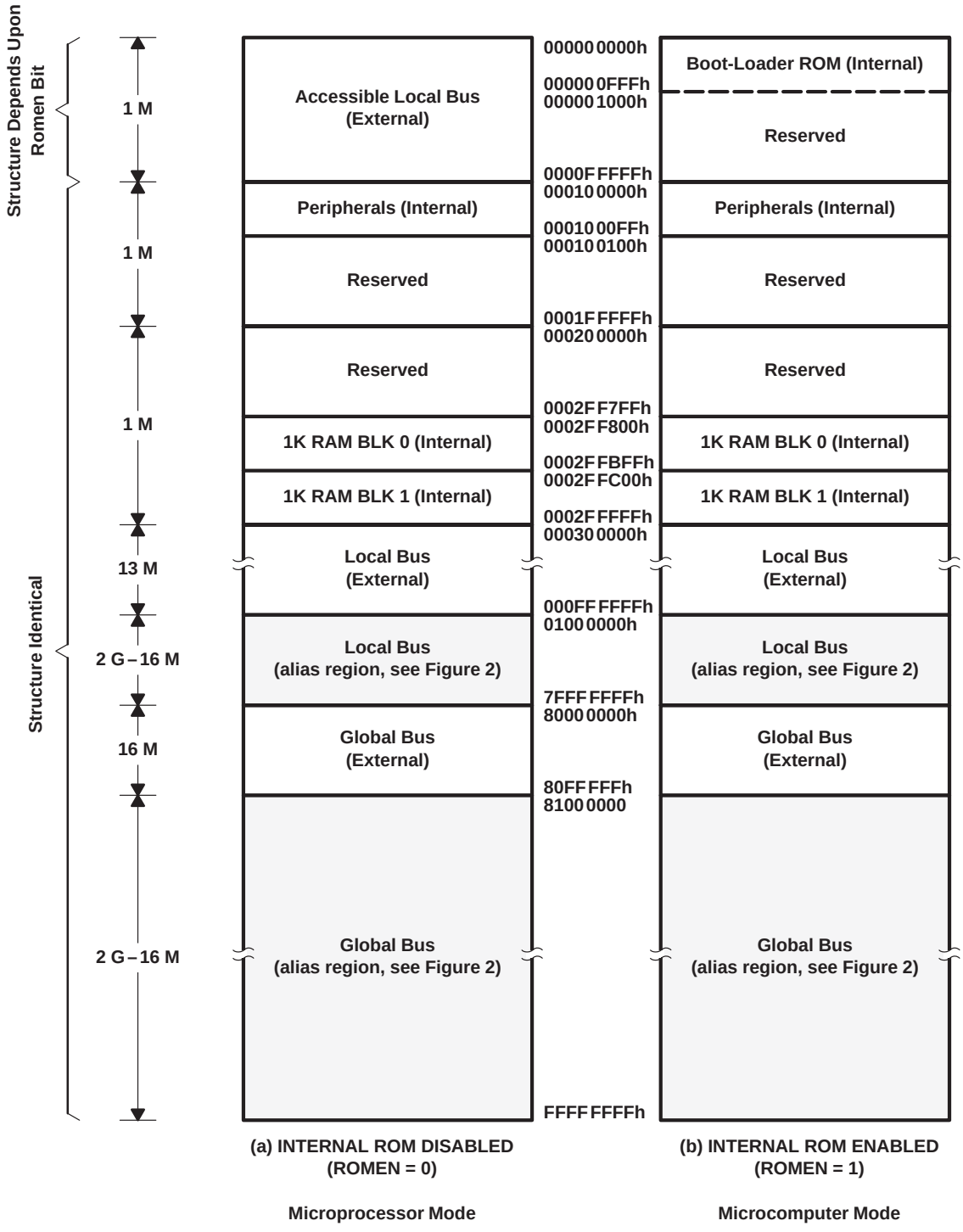


Figure 1. Memory Map for the ’320C44

description

The TMS320C44 DSP is a 32-bit, floating-point processor manufactured in 0.72-μm double-level-metal CMOS technology. The TMS320C44 is part of the TMS320C4x generation of DSPs from Texas Instruments. The on-chip parallel-processing capabilities of the ’C44 make the immense floating-point performance required by many applications achievable.

operation

The ’320C44 has four on-chip communication ports for processor-to-processor communication with no external hardware and simple communication software. This allows connectivity with no external-glue logic. The communication ports remove input/output bottlenecks, and the independent smart 6-channel DMA coprocessor is able to handle the CPU input/output burden.

To fit the ’320C40 into a 304-pin PQFP package (thermally enhanced plastic quad flatpack), two communication ports are removed and the external local and global address buses are reduced to 24 address lines each. In this case, both the bond pads and driver circuits are removed, decreasing die size and power consumption. Otherwise, functionality remains the same as the rest of the ’320C4x family.

The communication-port token and data-strobe control lines are internally connected to avoid spurious data, boot-up, and power consumption problems.

memory aliasing

The ’320C44 offers global and local addresses of A0–A23 and LA0–LA23, giving an external address reach of (2 buses) × (2^{24}) = 2^{25} words. Since the internal address span of the ’320C44 is 2^{32} words, reading or writing to memory outside of the base-address region causes memory aliasing. Figure 2 shows how the memory pages overlap each other.

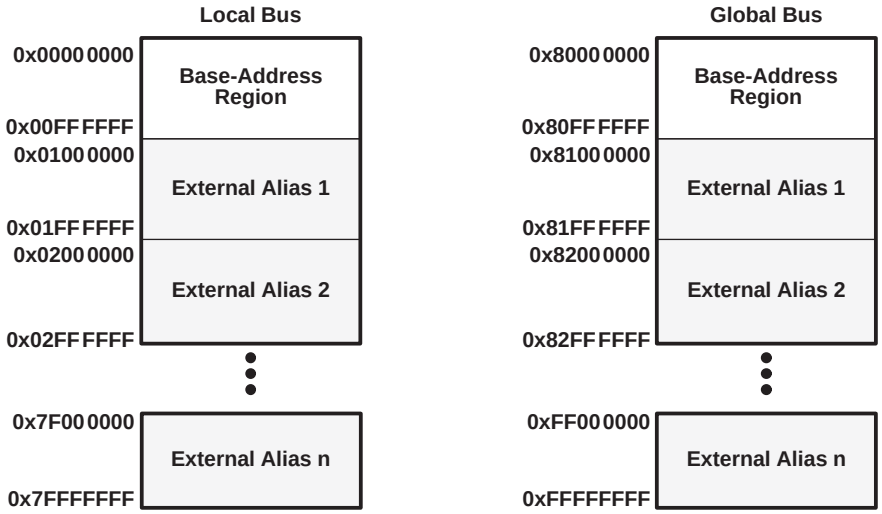


Figure 2. Memory Alias

central processing unit

The ’320C44 CPU is configured for high-speed internal parallelism for the highest sustained performance. The key features of the CPU are:

- Eight operations/cycle:
  - 40-/32-bit floating-point/integer multiply
  - 40-/32-bit floating-point/integer ALU operation
  - Two data accesses
  - Two address-register updates
- Floating-point conversion
- Divide and square-root support
- ’C3x and ’C4x assembly-language compatibility
- Byte and halfword accessibility

DMA coprocessor

The DMA coprocessor allows concurrent I/O and CPU processing for the highest sustained CPU performance. The key features of the DMA coprocessor are:

- Link pointers to allow DMA channels to autoinitialize without CPU intervention
- Parallel CPU operation and DMA transfers
- Six DMA channels to support memory-to-memory data transfers
- Split-mode operation which doubles the available channels to twelve when data transfers to and from a communication port are required

communication ports

The ’320C44 contains four identical high-speed communication ports, each of which provides a bidirectional-communication interface to other ’C4x devices and external peripherals. The key features of the communication ports are:

- Direct interprocessor communication and processor I/O
- 20M-byte/s bidirectional interface on each communication port for high-speed multiprocessor interface
- Port direction pin (CDIR) to ease interfacing
- Separate input and output 8-word-deep FIFO buffers for processor-to-processor communication and I/O
- Automatic arbitration and handshaking for direct processor-to-processor connection

communication-port direction pin

A port-direction pin (CDIR1, CDIR2, CDIR4, CDIR5) is available for each ’C44 communication port. When the communication port is in the output mode, CDIRx is driven low. When the communication port is in the input mode, CDIRx is driven high. The truth table for two ’320C44 devices is shown in Table 1. Communication port 1 of CPUA is connected to communication port 4 of CPUB.

Table 1. Truth Table for Two ’320C44 Devices

CDIR1	CDIR4	DESCRIPTION
0	0	Token error
0	1	CPUA is configured to transmit to CPUB.
1	0	CPUB is configured to transmit to CPUA.
1	1	Token exchange overlap, if > 1H then token error

communication-port-software reset

The input and output FIFO levels for a communication port can be flushed by writing at least two back-to-back values to its communication-port software-reset address as specified in Table 2. This software reset flushes any word or byte already present in the FIFOs, but it does not affect the status of the communication-port pins.

Table 2. Communication-Port Software-Reset Address

COMMUNICATION PORT	SOFTWARE-RESET ADDRESS
1	0x0100053
2	0x0100063
4	0x0100083
5	0x0100093

communication-port-software reset (continued)

When used in conjunction with the communication-port direction pins and $\overline{\text{NMI}}$ bus-grant, an effective method of error detection and correction can be achieved. A subroutine showing how to reset communication port 1 is given in Figure 3.

```
; ------------------------------------------------;
; RESET1:Flushes FIFOs data for communication port 1;
; ------------------------------------------------;
RESET1 push   AR0          ; Save registers
       push   R0           ;
       push   RC           ;
       ldhi   010h,AR0     ; Set AR0 to base address of COM 1
       or     050h,AR0     ;
FLUSH: rpts   1            ; Flush FIFO data with back-to-back write
       sti    R0,*+AR0(3)  ;
       rpts   10           ; Wait
       nop                 ;
       ldi    *+AR0(0),R0  ; Check for new data from other port
       and    01FE0h,R0    ;
       bnz    FLUSH        ;
       pop    RC           ; Restore registers
       pop    R0           ;
       pop    AR0          ;
       rets                ; Return
```

Figure 3. Example of Communication-Port-Software Reset

$\overline{\text{NMI}}$ with bus-grant feature

The ’320C44 devices have a software-configurable feature that allows forcing the internal-peripheral bus ready when the $\overline{\text{NMI}}$ signal is asserted. The $\overline{\text{NMI}}$ bus-grant feature is enabled when bits 19 and 18 of the status register (ST) are set to 10b. When enabled, a peripheral bus-grant signal is generated on the falling edge of $\overline{\text{NMI}}$. If $\overline{\text{NMI}}$ is asserted and this feature is not enabled, the CPU stalls on access to the peripheral bus if it is not ready. A stall condition occurs when writing to a full output FIFO or reading an empty input FIFO. This feature is useful in correcting communication-port errors when used in conjunction with the communication-port software-reset feature.

IDLE2 clock-stop power-down mode

The ’320C44 has a clock-stop mode, or power-down mode (IDLE2) to achieve extremely low power consumption. When an IDLE2 instruction is executed, the clocks are halted with H1 held high. (Exiting IDLE2 requires asserting one of the $\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$ pins configured as an external interrupt.) A macro showing how to generate the IDLE2 opcode is given in Figure 4. During this power-down mode:

- No instructions are executed.
- The CPU, peripherals, and internal memory retain their previous state.
- The external-bus outputs are idle. The address lines remain in their previous state; the data lines are in the high-impedance state; and the output-control signals are inactive.

IDLE2 clock-stop power-down mode (continued)

```
; ------------------------------------------------;
; IDLE2: Macro to generate idle2 opcode           ;
; ------------------------------------------------;
IDLE2     .macro
          .word     06000001h
          .endm
```

Figure 4. Example Software Subroutine Using IDLE2

IDLE2 is exited when one of the five external interrupts ($\overline{\text{NMI}}$ and $\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$) is asserted low for at least four input clocks (two H1 cycles). The clocks then start after a delay of two input clocks (one H1 cycle). The clocks can start in the opposite phase; that is, H1 can be high when H3 was high before the clocks were stopped. However, the H1 and H3 clocks remain 180 degrees out of phase with each other.

During IDLE2 operation, an external interrupt can be recognized and serviced by the CPU if it is enabled before entering IDLE2 and asserted for at least two H1 cycles. For the processor to recognize only one interrupt, the interrupt pin must be configured for edge-trigger mode or asserted less than three cycles in level-trigger mode. Any external interrupt pin can wake up the device from IDLE2, but for the CPU to recognize that interrupt, it must also be enabled. If an interrupt is recognized and executed by the CPU, the instruction following the IDLE2 instruction is not executed until after a return opcode is executed.

When the device is in emulation mode, the CPU executes an IDLE2 instruction as if it were an IDLE instruction. The clocks continue to run for correct operation of the emulator.

boot-loader mode selection

Table 3. Boot-Loader Mode Selection Using Pins $\overline{\text{IIOF3}}$–$\overline{\text{IIOF0}}$

EXTERNAL PIN				SOURCE PROGRAM LOCATION
$\overline{\text{IIOF3}}$	$\overline{\text{IIOF2}}$	$\overline{\text{IIOF1}}$	$\overline{\text{IIOF0}}$	
1	1	0	1	Load source program from address 0030 0000h
1	0	1	1	Load source program from address 4000 0000h (see Note 1)
1	0	0	1	Load source program from address 80 0000h
0	1	1	1	Load source program from address 8000 0000h (see Note 2)
0	1	0	1	Load source program from address 8040 0000h (see Note 3)
0	0	1	1	Load source program from address 8080 0000h (see Note 4)
0	0	0	1	Reserved (boot-loader program terminates)
1	1	1	1	Load source program from communication port

NOTES: 1. This selection cause the 'C44 to drive 0 in the 24 external local address pins and activates the $\overline{\text{LSTRB0}}$ signal.
2. This selection cause the 'C44 to drive 0 in the 24 external global address pins ando activates the $\overline{\text{STRB0}}$ signal.
3. This selection cause the 'C44 to drive 0x40 0000 in the 24 external global address pins and activates the $\overline{\text{STRB0}}$ signal.
4. This selection cause the 'C44 to drive 0x80 0000 in the 24 external global address pins and to activate the $\overline{\text{STRB0}}$ signal.

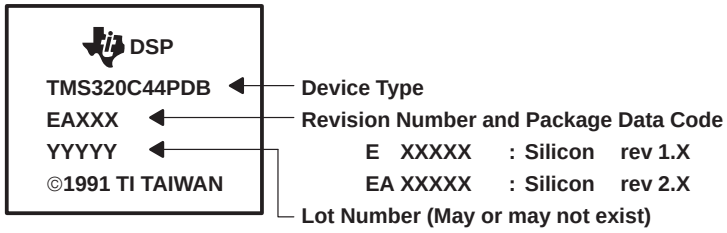
development tools

A key aspect to a parallel-processing implementation is the development tools available. The ’C44 is supported by a host of parallel-processing tools for developing and simulating code easily and for debugging parallel-processing systems. The code-generation tools include:

- An optimizing ANSI C compiler with a runtime-support library that supports use of communication ports and DMA
- Third party support for C, C++, and Ada compilers
- Several operating systems available for parallel-processing support as well as DMA and communication-port drivers
- Assembler and linker with support for mapping program and data to parallel processors

The simulation tools include a TI software-simulator with a high-level-language debugger interface for simulating a single processor. The hardware development and verification tools consist of the XDS510 (parallel-processor in-circuit emulator and high-level-language debugger).

silicon revision identification



absolute maximum ratings over specified temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 5) . . . . . – 0.3 V to 7 V
Input voltage range . . . . . – 0.3 V to 7 V
Output voltage range . . . . . – 0.3 V to 7 V
Operating case temperature range, T_C . . . . . 0°C to 85°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 5: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	TYP‡	MAX	UNIT
V_{DD}	Supply voltage (DDV_{DD}, etc.)		4.75	5	5.25	V
V_{IH}	High-level input voltage	X2 / CLKIN	2.6		V_{DD} + 0.3§	V
		$\overline{CSTRB}$ and $\overline{CRDY}$ pins	2.4		V_{DD} + 0.3§	
		All other pins	2		V_{DD} + 0.3§	
V_{IL}	Low-level input voltage		– 0.3§		0.8	V
I_{OH}	High-level output current				– 300	µA
I_{OL}	Low-level output current				2	mA
T_C	Operating case temperature		0		85	°C

‡ All typical values are at V_{DD} = 5 V, T_A (air temperature)= 25°C.
§ This parameter is characterized but not tested.

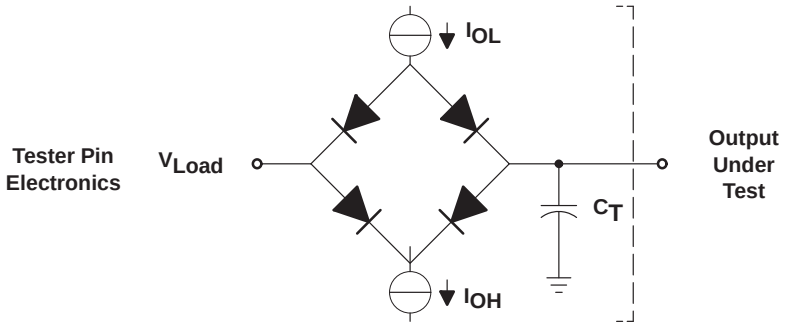
electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS¶		MIN	TYP#	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = MIN, I_{OH} = MAX		2.4	3		V
V_{OL}	Low-level output voltage		V_{DD} = MIN, I_{OL} = MAX			0.3	0.6	V
I_Z	High-impedance current		V_{DD} = MAX		–20		20	µA
I_I	Input current	X2/CLKIN only	V_I = V_{SS} to V_{DD}		–30		30	µA
		Inputs with internal pullups (see Note 6)			–400		20	
		All others			–10		10	
I_{CC}	Supply current		T_A = 25°C, V_{DD} = MAX, f_x = MAX (see Note 7)	’320C44-40 ’320C44-50		350	850	mA
				’320C44-60		350	950	
C_I	Input capacitance						15‖	pF
C_O	Output capacitance						15‖	pF

¶ For conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.
# All typical values are at V_{DD} = 3.3 V, T_A (air temperature) = 25°C.
‖ This parameter is specified by design but not tested.

NOTES: 6. Pins with internal pullup devices: TDI, TCK, TMS. Pin with internal pulldown device: $\overline{TRST}$.
7. f_x is the input clock frequency. The maximum value (max) for the ’320C44-40, ’320C44-50, and ’320C44-60 is 40, 50 and 60 MHz, respectively.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 2.15 V
C_T = 80 pF typical load-circuit capacitance

Figure 5. Test Load Circuit

signal transition levels

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows:

- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.
- For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.

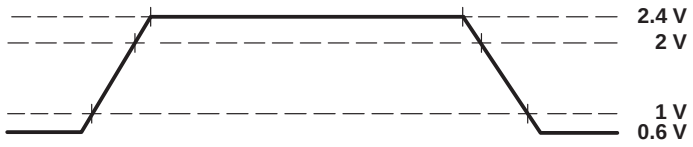


Figure 6. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows:

- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.92 V (10%) and the level at which the input is said to be high is 1.88 V (90%).
- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.88 V (90%) and the level at which the input is said to be low is 0.92 V (10%).

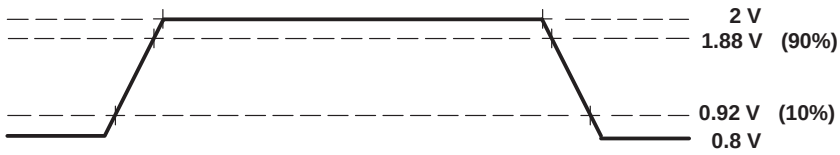


Figure 7. TTL-Level Inputs

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, pin names that have both global and local applications are generally represented with (L) immediately preceding the basic signal name (for example, (L)RDY represents both the global term RDY and local term LRDY). Other pin names and related terminology have been abbreviated as follows, unless otherwise noted:

A	(L)A23–(L)A0 or (L)Ax	IACK	$\overline{\text{IACK}}$
AE	$\overline{\text{(L)AE}}$	IF	$\overline{\text{IIOF(3–0)}}$ or $\overline{\text{IIOFx}}$
ASYNCH	Asynchronous reset signals in the high-impedance state	IIOF	$\overline{\text{IIOF(3–0)}}$ or $\overline{\text{IIOFx}}$
BYTE	Byte transfer	LOCK	$\overline{\text{(L)LOCK}}$
CA	$\overline{\text{CACK(1,2,4,5)}}$ or $\overline{\text{CACKx}}$	P	$t_{C(H)}$
CD	C(1,2,4,5)D7–C(1,2,4,5)D0 or CxDx	PAGE	(L)PAGE0 and (L)PAGE1 or (L)PAGEx
CDIR	CDIR(1,2,4,5) or CDIRx	RDY	$\overline{\text{(L)RDY0}}$, $\overline{\text{(L)RDY1}}$, or $\overline{\text{(L)RDYx}}$
CE	$\overline{\text{(L)CE0}}$, $\overline{\text{(L)CE1}}$, or $\overline{\text{(L)CEx}}$	RESET	$\overline{\text{RESET}}$
CI	CLKIN	RW	(L)R/$\overline{\text{W}}$0, (L)R/$\overline{\text{W}}$1, or (L)R/$\overline{\text{W}}$x
COMM	Asynchronous reset signals	S	$\overline{\text{(L)STRB0}}$, $\overline{\text{(L)STRB1}}$, or $\overline{\text{(L)STRBx}}$
CONTROL	Control signals	ST	(L)STAT3–(L)STAT0 or (L)STATx
CRQ	$\overline{\text{CREQ(1,2,4,5)}}$ or $\overline{\text{CREQx}}$	TCK	TCK
CRDY	$\overline{\text{CRDY(1,2,4,5)}}$ or $\overline{\text{CRDYx}}$	TCLK	TCLK0, TCLK1, or TCLKx
CS	$\overline{\text{CSTRB(1,2,4,5)}}$ or $\overline{\text{CSTRBx}}$	TDO	TDO
D	(L)D31–(L)D0 or (L)Dx	TMS	TMS/TDI
DE	$\overline{\text{(L)DE}}$	WORD	32-bit word transfer
H	H1, H3		

timing for X2/CLKIN, H1, H3 (see Figure 8 and Figure 9)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$	Fall time, CLKIN		5†		5†	ns
2	$t_{w(CIL)}$	Pulse duration, CLKIN low, $t_{c(CI)}$ = MIN	7		5		ns
3	$t_{w(CIH)}$	Pulse duration, CLKIN high, $t_{c(CI)}$ = MIN	7		5		ns
4	$t_{r(CI)}$	Rise time, CLKIN		5†		5†	ns
5	$t_{c(CI)}$	Cycle time, CLKIN	20	242.5	16.67	242.5	ns
6	$t_{f(H)}$	Fall time, H1 and H3		3		3	ns
7	$t_{w(HL)}$	Pulse duration, H1 and H3 low	$t_{c(CI)}-6$	$t_{c(CI)}+6$	$t_{c(CI)}-6$	$t_{c(CI)}+6$	ns
8	$t_{w(HH)}$	Pulse duration, H1 and H3 high	$t_{c(CI)}-6$	$t_{c(CI)}+6$	$t_{c(CI)}-6$	$t_{c(CI)}+6$	ns
9	$t_{r(H)}$	Rise time, H1 and H3		4		4	ns
9.1	$t_{d(HL-HH)}$	Delay time from H1 low to H3 high or from H3 low to H1 high	–1	4	–1	4	ns
10	$t_{c(H)}$	Cycle time, H1 and H3‡	40	485	33.3	485	ns

† This value is specified by design but not tested.
‡ Maximum cycle time is not limited during IDLE2 operation.

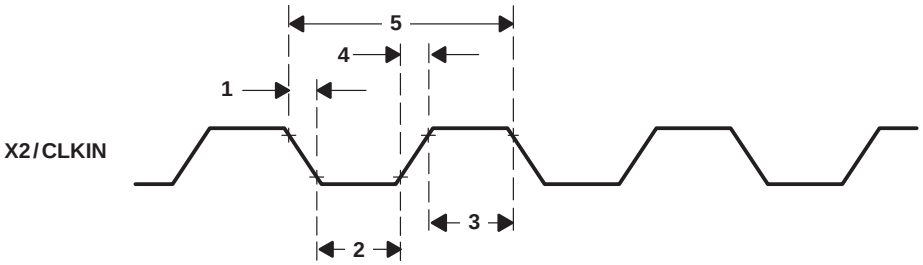


Figure 8. X2/CLKIN Timing

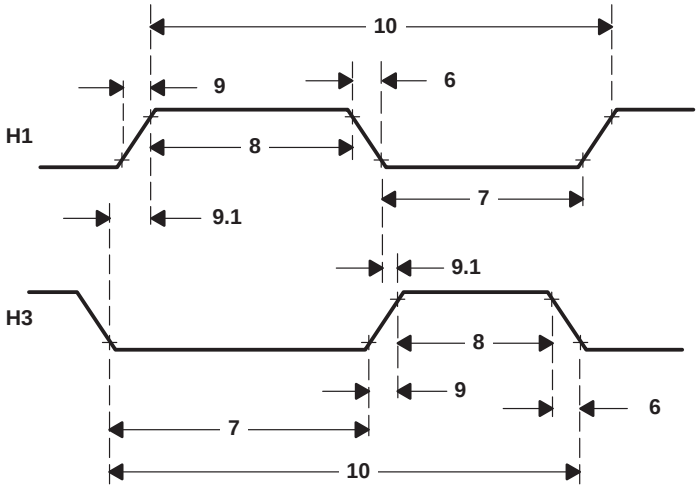


Figure 9. H1 and H3 Timings

memory-read-cycle and memory-write-cycle timing [$\overline{\text{(L)STRBx}}$ = 0] (see Note 8, Figure 10, and Figure 11)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(H1L-SL)}$	Delay time, H1 low to (L)$\overline{\text{STRBx}}$ low	0†	9	0†	8	ns
2	$t_{d(H1L-SH)}$	Delay time, H1 low to (L)$\overline{\text{STRBx}}$ high	0†	9	0†	8	ns
3	$t_{d(H1H-RWL)}$	Delay time, H1 high to (L)R/$\overline{\text{W}}$x low	0†	9	0†	8	ns
4	$t_{d(H1L-A)}$	Delay time, H1 low to (L)Ax valid	0†	9	0†	8	ns
5	$t_{su(D-H1L)R}$	Setup time, (L)Dx valid before H1 low (read)	10		9		ns
6	$t_{h(H1L-D)R}$	Hold time, (L)Dx after H1 low (read)	0		0		ns
7	$t_{su(RDY-H1L)}$	Setup time, (L)$\overline{\text{RDYx}}$ valid before H1 low	20‡		18†		ns
8	$t_{h(H1L-RDY)}$	Hold time, (L)$\overline{\text{RDYx}}$ after H1 low	0		0		ns
8.1	$t_{d(H1L-ST)}$	Delay time, H1 low to (L)STAT3–(L)STAT0 valid		8		8	ns
9	$t_{d(H1H-RWH)W}$	Delay time, H1 high to (L)R/$\overline{\text{W}}$x high (write)	0†	9	0†	8	ns
10	$t_{v(H1L-D)W}$	Valid time, (L)Dx after H1 low (write)		16		13	ns
11	$t_{h(H1H-D)W}$	Hold time, (L)Dx after H1 high (write)	0		0		ns
12	$t_{d(H1H-A)}$	Delay time, H1 high to address valid on back-to-back write cycles		9		8	ns

† This value is specified by design but not tested.
‡ If this setup time is not met, the read/write operation is not assured.
NOTE 8: For consecutive reads, (L)R/$\overline{\text{W}}$x stays high and (L)STRBx stays low.

memory-read-cycle and memory-write-cycle timing [$\overline{\text{(L)STRBx}}$ = 0] (continued)

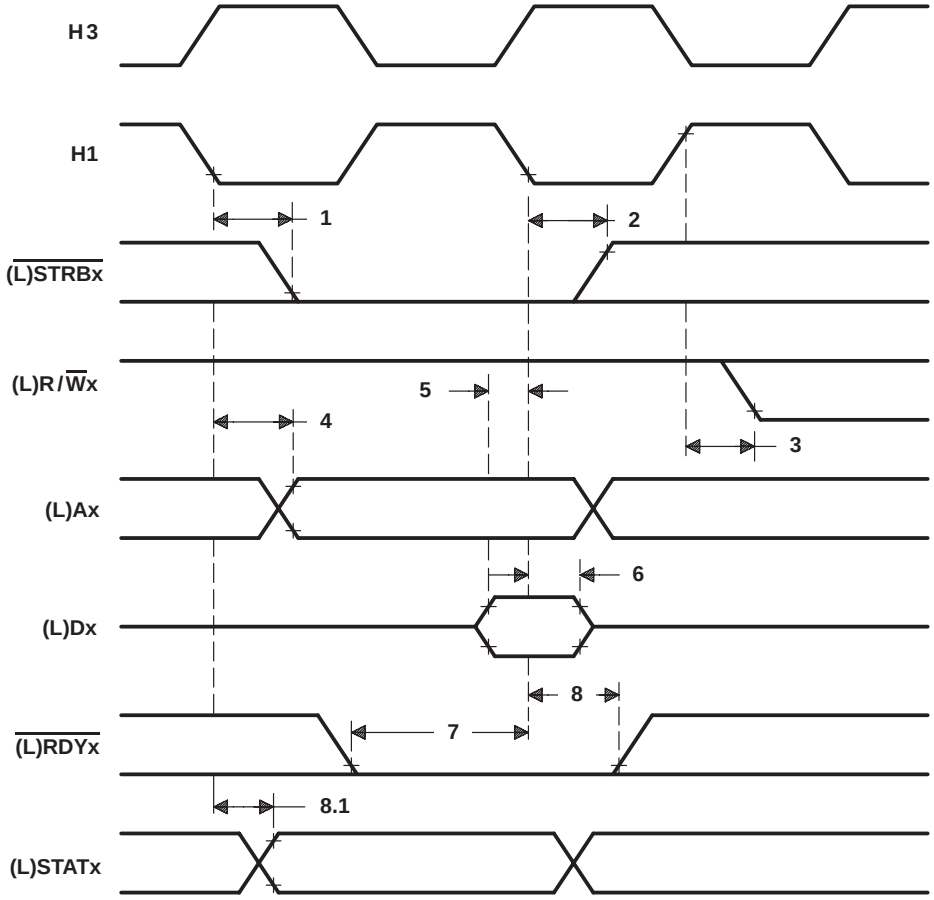


Figure 10. Memory-Read-Cycle Timing [$\overline{\text{(L)STRBx}}$ = 0]

memory-read-cycle and memory-write-cycle timing [$\overline{\text{(L)STRBx}}$ = 0] (continued)

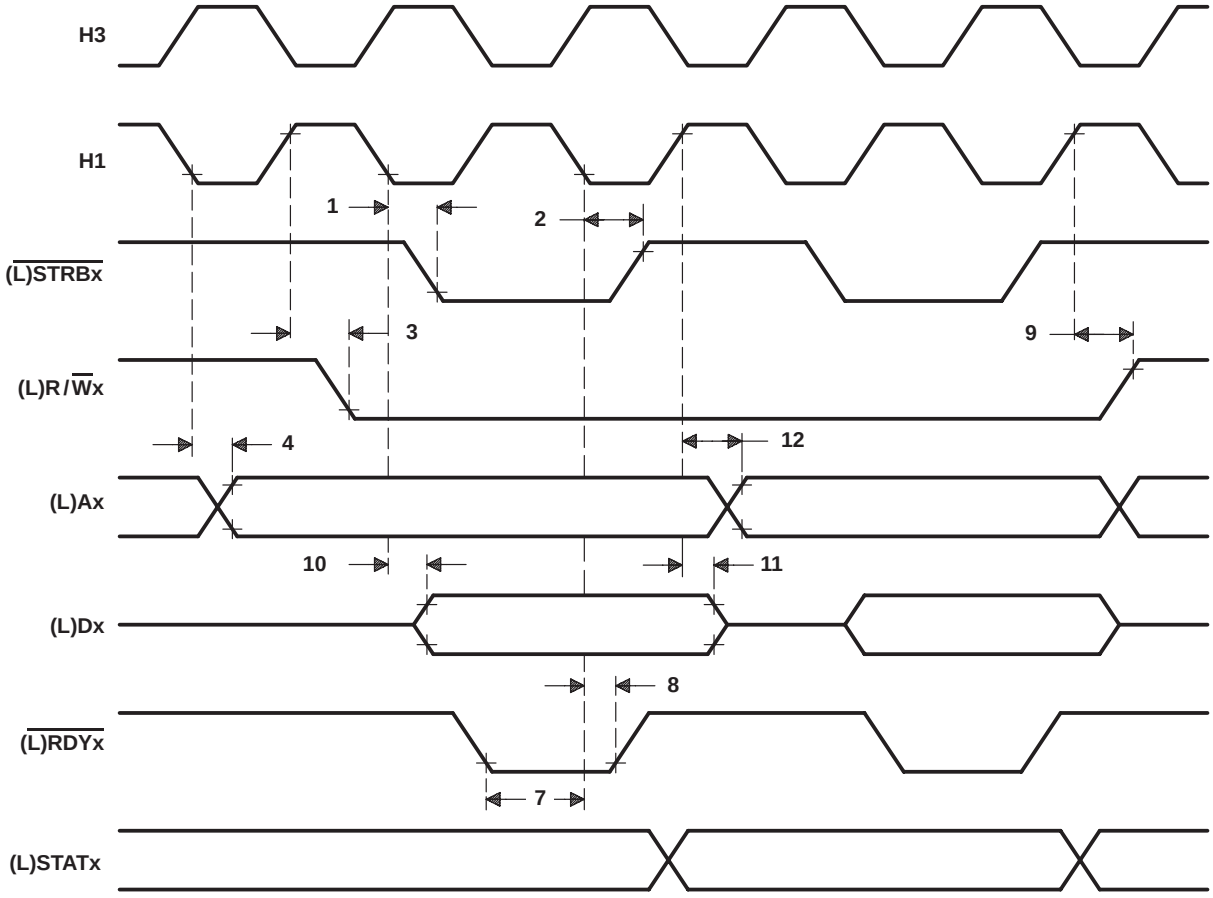


Figure 11. Memory-Write-Cycle Timing [$\overline{\text{(L)STRBx}}$ = 0]

(L)DE-, (L)AE-, and (L)CEx-enable timing (see Figure 12)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(DEH-DZ)}$	Delay time, (L)DE high to (L)D0–(L)D31 in the high-impedance state	0†	15‡	0†	15‡	ns
2	$t_{d(DEL-DV)}$	Delay time, (L)DE low to (L)D0–(L)D31 valid	0†	21	0†	16	ns
3	$t_{d(AEH-AZ)}$	Delay time, (L)AE high to (L)A0–(L)A23 in the high-impedance state	0†	15‡	0†	15‡	ns
4	$t_{d(AEL-AV)}$	Delay time, (L)AE low to (L)A0–(L)A23 valid	0†	18	0†	16	ns
5	$t_{d(CEH-RWZ)}$	Delay time, (L)CEx high to (L)R/W0, (L)R/W1 in the high-impedance state	0†	15‡	0†	15‡	ns
6	$t_{d(CEL-RWV)}$	Delay time, (L)CEx low to (L)R/W0, (L)R/W1 valid	0†	21	0†	16	ns
7	$t_{d(CEH-SZ)}$	Delay time, (L)CEx high to (L)STRB0, (L)STRB1 in the high-impedance state	0†	15‡	0†	15‡	ns
8	$t_{d(CEL-SV)}$	Delay time, (L)CEx low to (L)STRB0, (L)STRB1 valid	0†	21	0†	16	ns
9	$t_{d(CEH-PAGEZ)}$	Delay time, (L)CEx high to (L)PAGE0, (L)PAGE1 in the high-impedance state	0†	15‡	0†	15‡	ns
10	$t_{d(CEL-PAGEV)}$	Delay time, (L)CEx low to (L)PAGE0, (L)PAGE1 valid	0†	21	0†	16	ns

† This value is specified by design but not tested.
‡ This value is characterized but not tested.

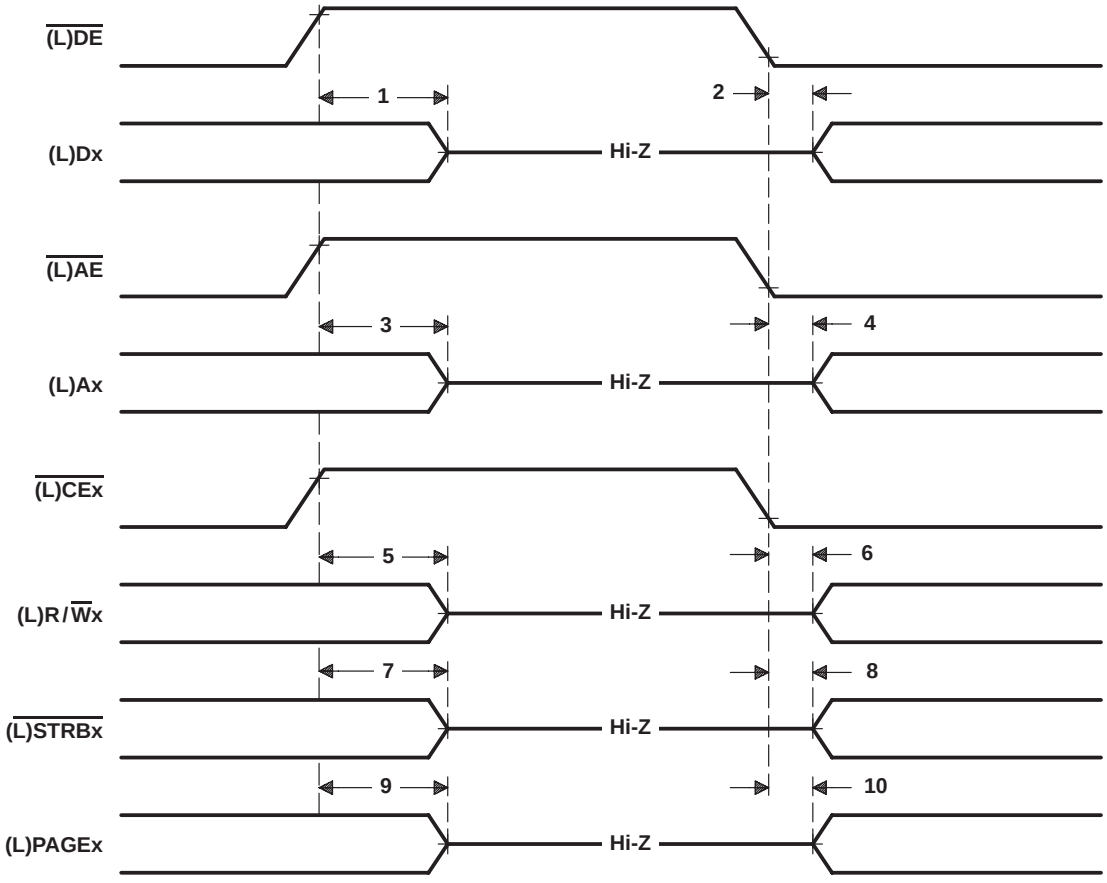


Figure 12. (L)DE-, (L)AE-, and (L)CEx-Enable Timing

timing for (L)$\overline{\text{LOCK}}$ when executing LDFI or LDII (see Figure 13)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(H1L-LOCKL)}$ Delay time, H1 low to (L)$\overline{\text{LOCK}}$ low		8		8	ns

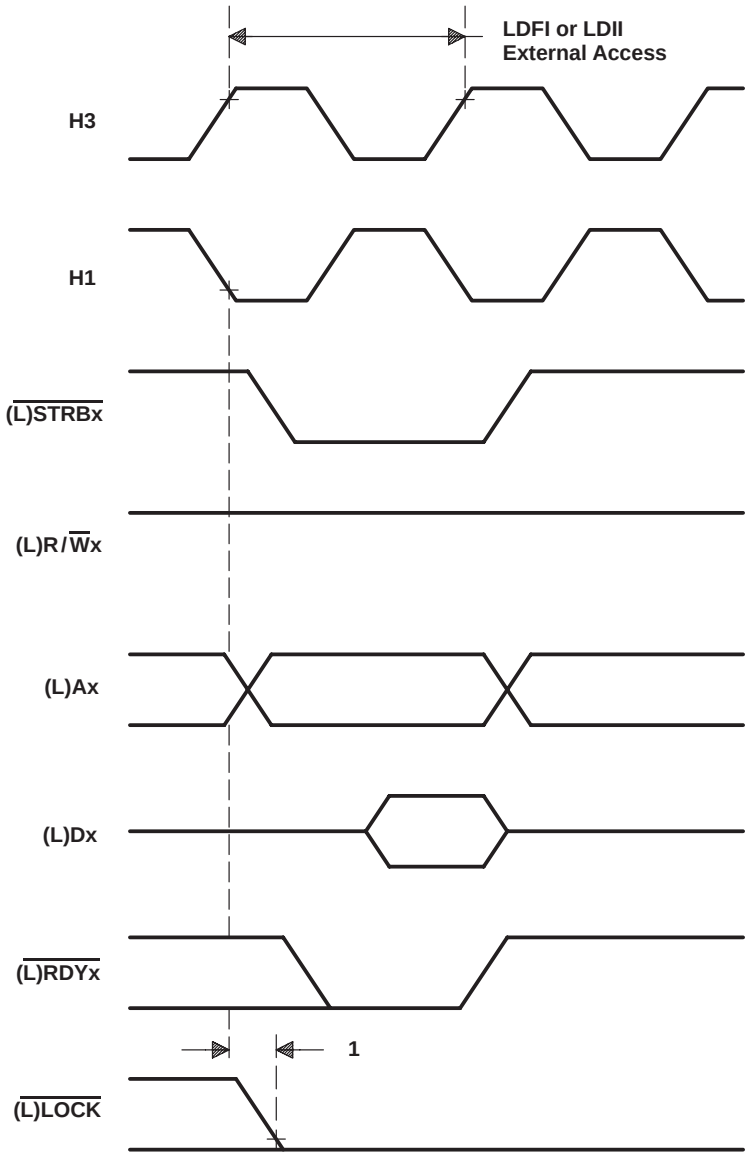


Figure 13. Timing for (L)$\overline{\text{LOCK}}$ When Executing LDFI or LDII

timing for $\overline{\text{(L)LOCK}}$ when executing STFI or STII (see Figure 14)

NO.		TMS320C44-50		TMS320C44-60		UNIT
		MIN	MAX	MIN	MAX	
1	$t_{d(H1L-LOCKH)}$ Delay time, H1 low to $\overline{\text{(L)LOCK}}$ high		8		8	ns

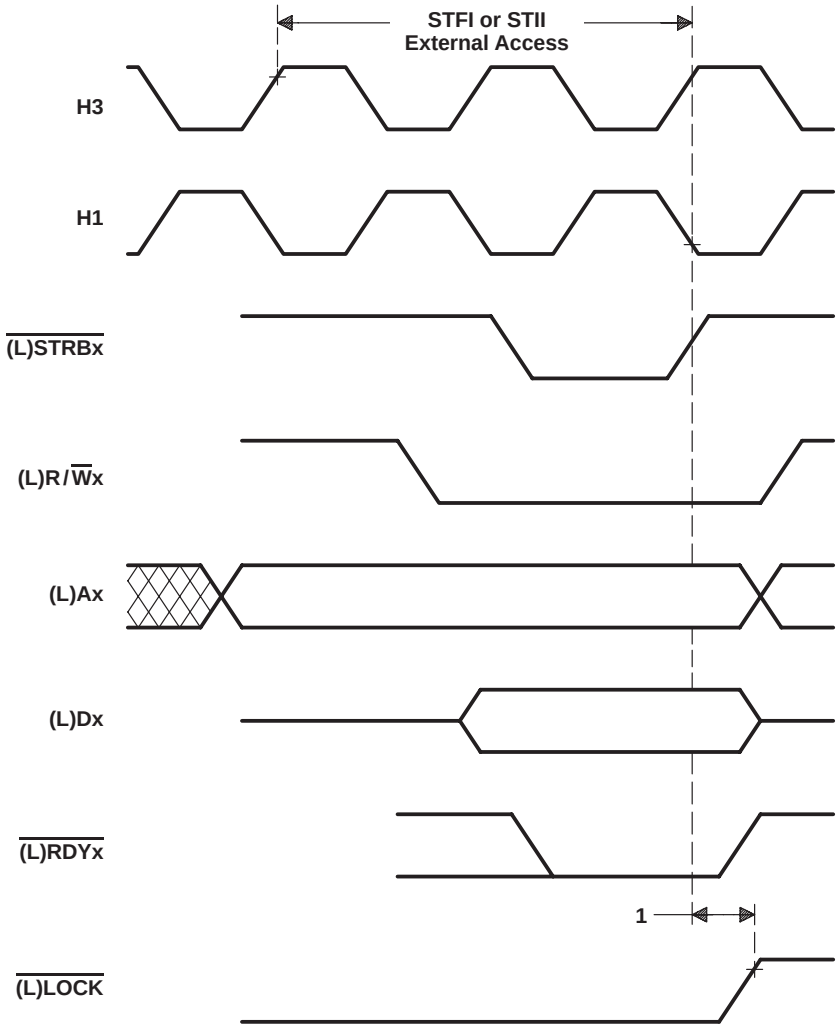


Figure 14. Timing for $\overline{\text{(L)LOCK}}$ When Executing STFI or STII

timing for $\overline{\text{(L)LOCK}}$ when executing SIGI (see Figure 15)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(H1L-LOCKL)}$	Delay time, H1 low to $\overline{\text{(L)LOCK}}$ low		8		8	ns
2	$t_{d(H1L-LOCKH)}$	Delay time, H1 low to $\overline{\text{(L)LOCK}}$ high		8		8	

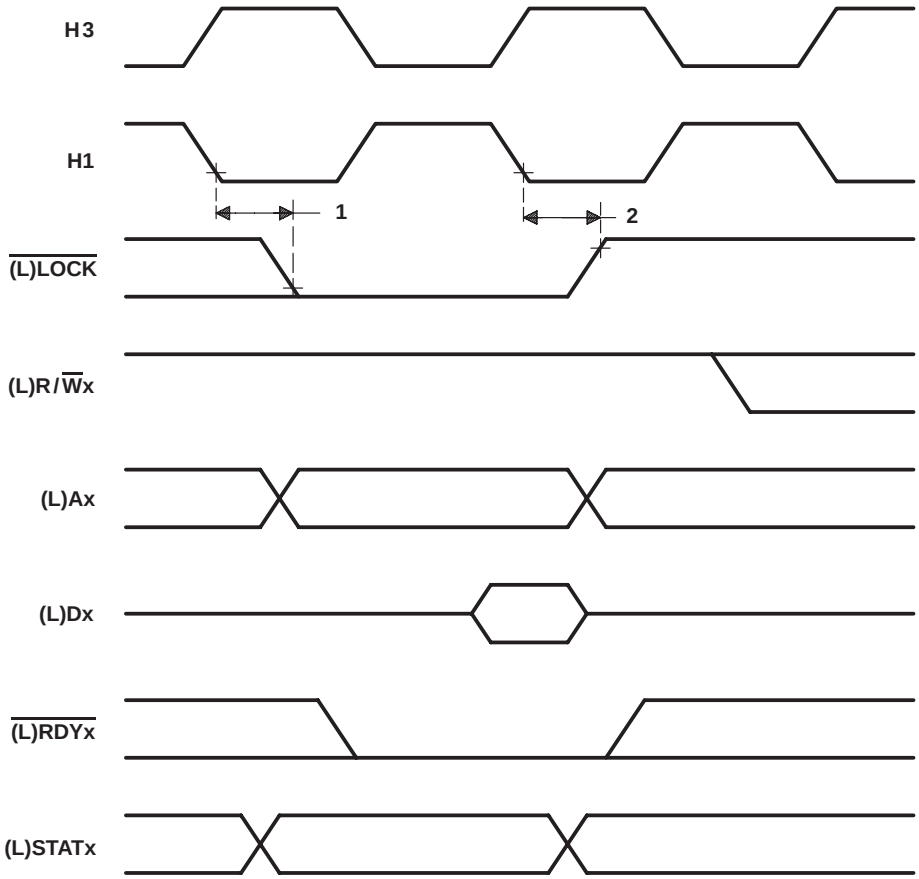


Figure 15. Timing for $\overline{\text{(L)LOCK}}$ When Executing SIGI

timing for (L)PAGE0, (L)PAGE1 during memory access to a different page (see Figure 16)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(H1L-PAGEH)}$	Delay time, H1 low to (L)PAGEx high for access to different page	0	9	0	8	ns
2	$t_{d(H1L-PAGEL)}$	Delay time, H1 low to (L)PAGEx low for access to different page	0	9	0	8	ns

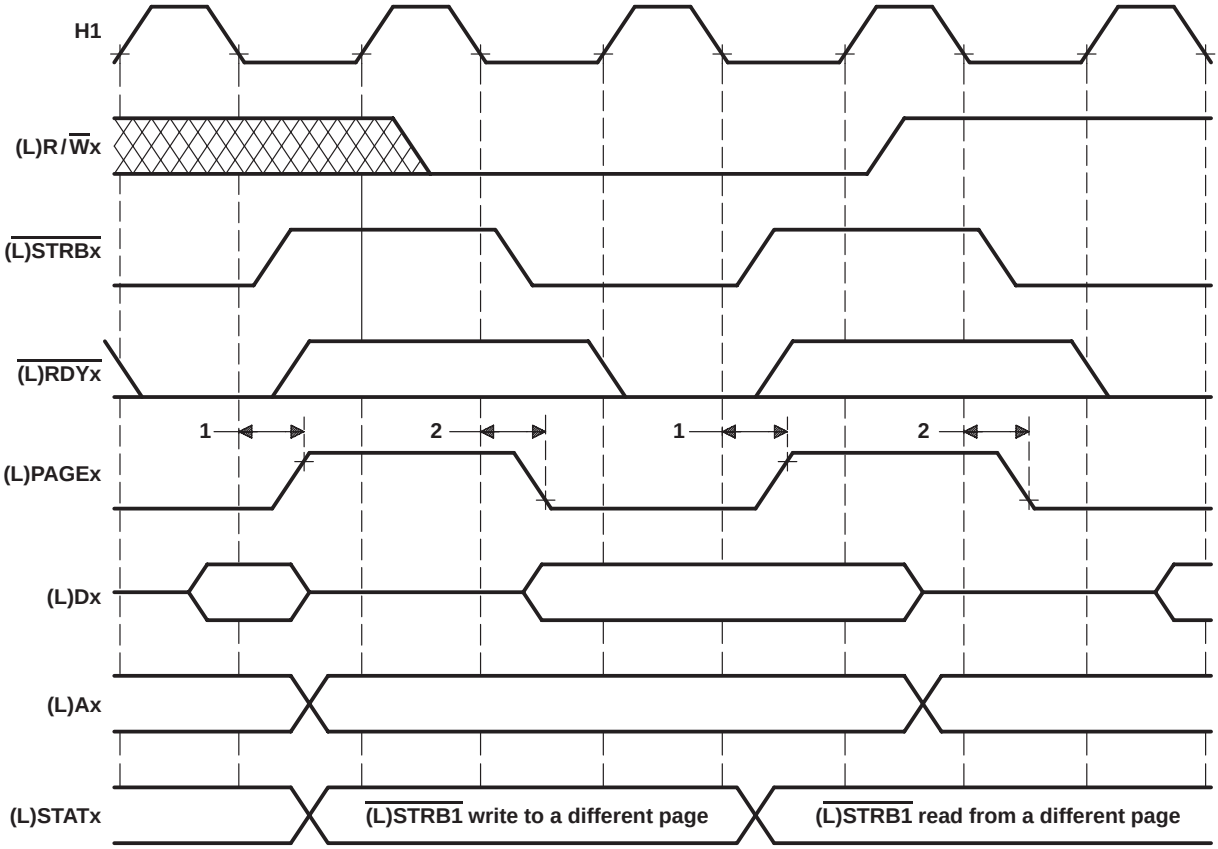


Figure 16. (L)PAGE0, (L)PAGE1 Timing Cycle, Memory Access to a Different Page

timing for the $\overline{\text{IIOFx}}$ when configured as an output (see Figure 17)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{v(H1L-IIOF)}$	H1 low to $\overline{\text{IIOFx}}$ valid		14		14	ns

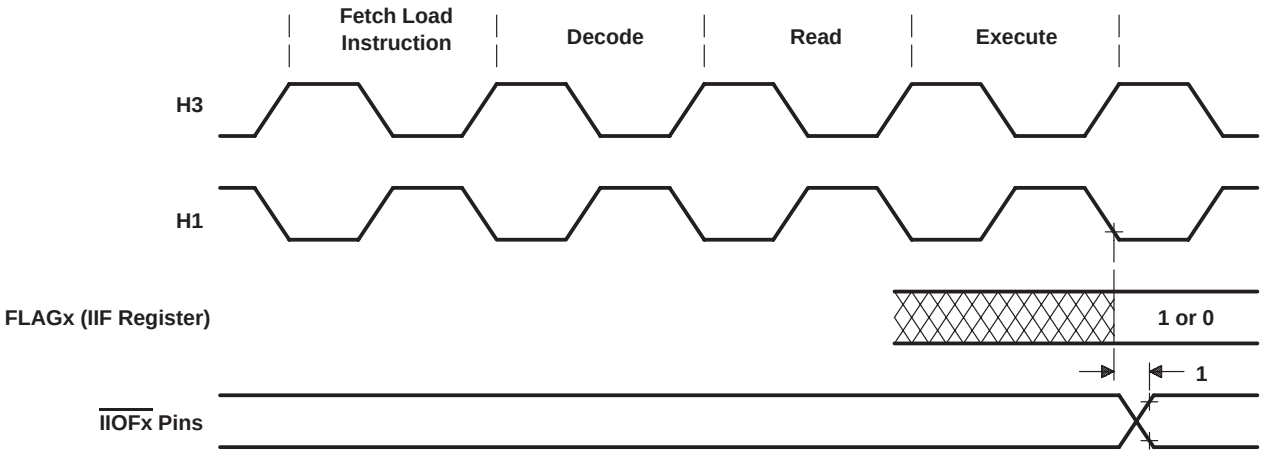


Figure 17. Timing for the $\overline{\text{IIOFx}}$ When Configured as an Output

timing of $\overline{\text{IIOFx}}$ changing from output to input mode (see Figure 18)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{h(H1L-IIOF)}$	Hold time, $\overline{\text{IIOFx}}$ after H1 low		14†		14†	ns
2	$t_{su(IIOF-H1L)}$	Setup time, $\overline{\text{IIOFx}}$ before H1 low	11		11		ns
3	$t_{h(H1L-IIOF)}$	Hold time, $\overline{\text{IIOFx}}$ after H1 low	0		0		ns

† This value is specified by design but not tested.

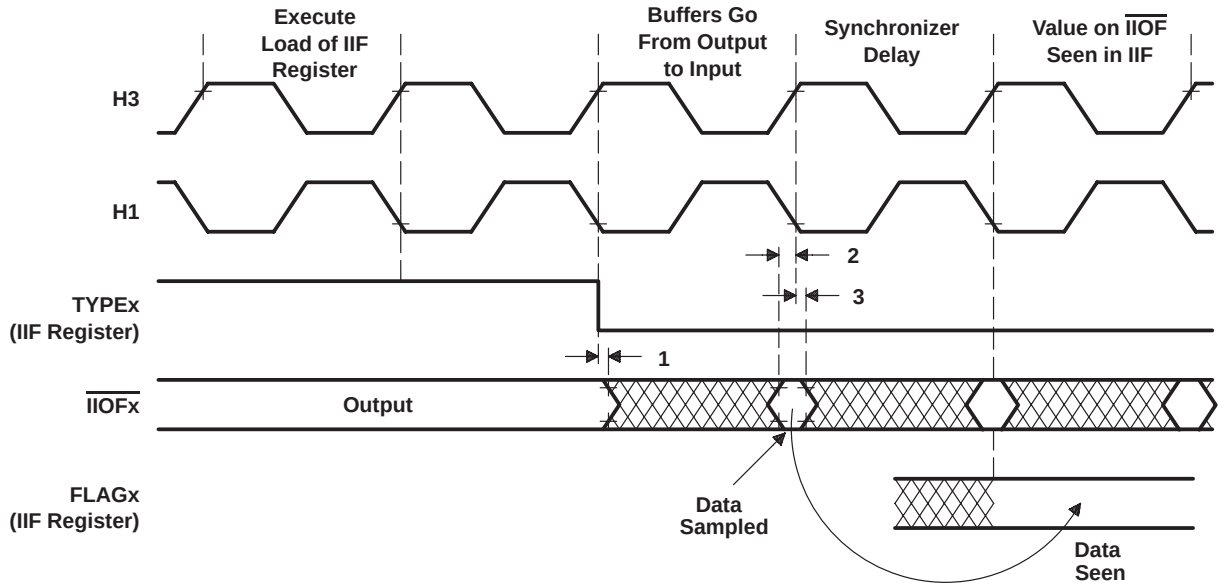


Figure 18. Change of $\overline{\text{IIOFx}}$ From Output to Input Mode

timing of $\overline{\text{IIOFx}}$ changing from input to output mode (see Figure 19)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(H1L-IFIO)}$	Delay time, H1 low to $\overline{\text{IIOFx}}$ switching from input to output		14		14	ns

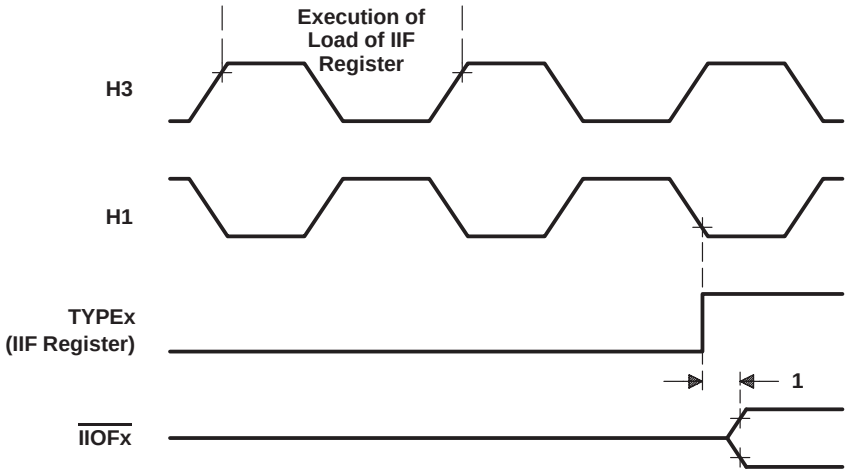
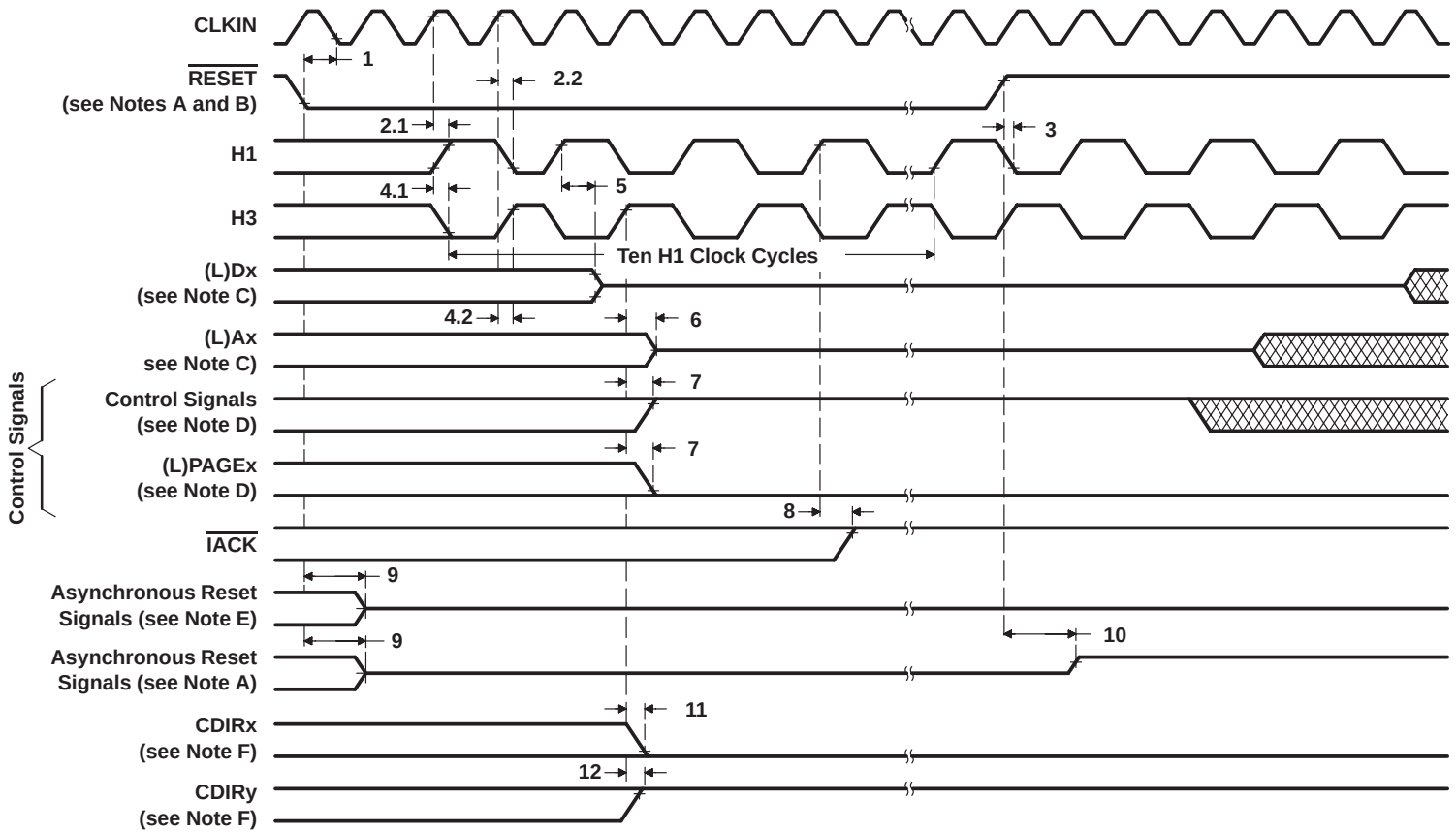


Figure 19. Change of $\overline{\text{IIOFx}}$ From Input to Output Mode

$\overline{\text{RESET}}$ timing (see Figure 20)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{su(RESET-C1L)}$	Setup time for $\overline{\text{RESET}}$ before CLKIN low	11	$t_{c(CI)}$	11	$t_{c(CI)}$	ns
2.1	$t_{d(CIH-H1H)}$	Delay time, CLKIN high to H1 high	2	10	2	10	ns
2.2	$t_{d(CIH-H1L)}$	Delay time, CLKIN high to H1 low	2	10	2	10	ns
3	$t_{su(RESETH-H1L)}$	Setup time for $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	13		13		ns
4.1	$t_{d(CIH-H3L)}$	Delay time, CLKIN high to H3 low	2	10	2	10	ns
4.2	$t_{d(CIH-H3H)}$	Delay time, CLKIN high to H3 high	2	10	2	10	ns
5	$t_{d(H1H-DZ)}$	Delay time, H1 high to (L)Dx in the high-impedance state		13†		13†	ns
6	$t_{d(H3H-AZ)}$	Delay time, H3 high to (L)Ax in the high-impedance state		9†		9†	ns
7	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high [low for (L)PAGE]		9†		9†	ns
8	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		9†		9†	ns
9	$t_{d(RESETL-ASYNCH)}$	Delay time, $\overline{\text{RESET}}$ low to asynchronous reset signals in the high-impedance state		21†		21†	ns
10	$t_{d(RESETH-COMMH)}$	Delay time, $\overline{\text{RESET}}$ high to asynchronous reset signals high		15†		15†	ns
11	$t_{d(H1H-CDIRL)}$	Delay time,		9		9	ns
12	$t_{d(H1H-CDIRH)}$	Delay time,		9		9	ns

† This value is characterized but not tested.



NOTES: A. Asynchronous reset signals that go to a high logic level after RESET returns to a high state include CREQy, CACKx, CSTRBx, and CRDYy (where x = 1 or 2 and y = 4 or 5).
B. RESET is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.
C. For this diagram, (L)Dx includes D31–D0, LD31–LD0, and CxD7–CxD0; (L)Ax includes LA(23–0) and A(23–0).
D. Control signals LSTRB0, LSTRB1, STRB0, STRB1, (L)STAT3–(L)STAT0, (L)LOCK, (L)R/W0, and (L)R/W1 go high while (L)PAGE0 and (L)PAGE1 go low.
E. Asynchronous reset signals that go into the high-impedance state after RESET goes low include TCLK0, TCLK1, IIOF3–IIOF0, and the communication-port control signals CREQx, CACKy, CSTRBy, and CRDYx (where x = 1 or 2, and y = 4 or 5). At reset, ports 1 and 2 become outputs, and ports 4 and 5 become inputs.
F. x = 1 or 2 and y = 4 or 5

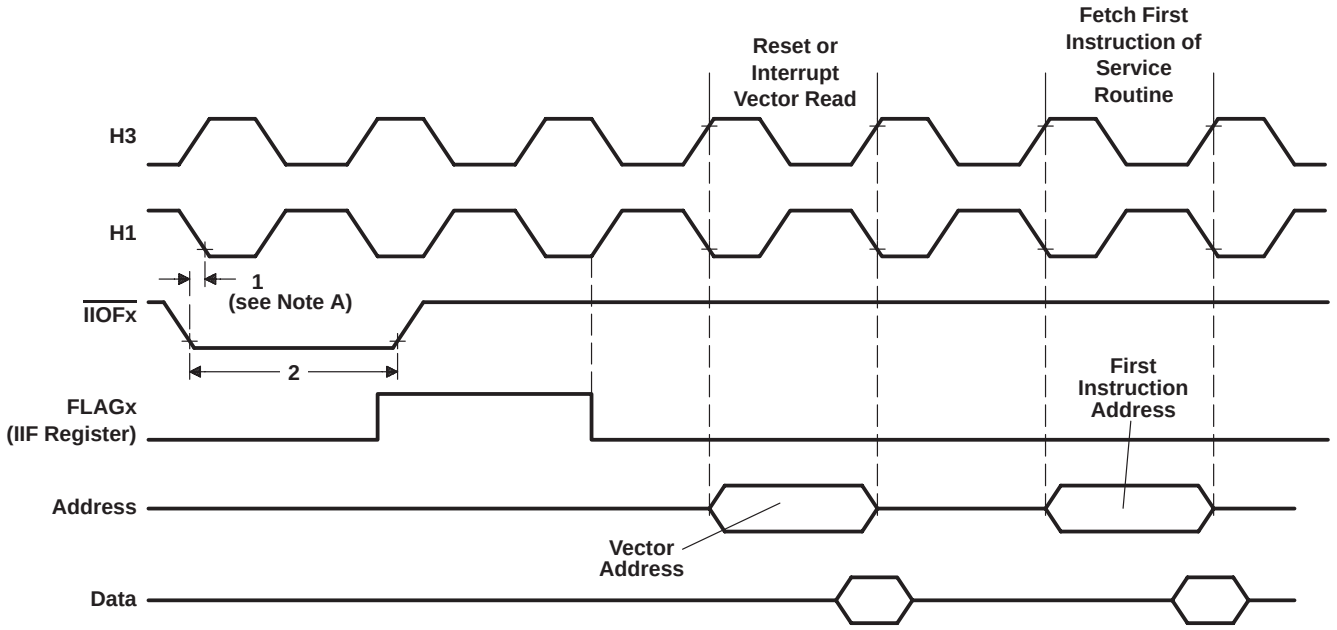
Figure 20. RESET Timing

timing for $\overline{\text{IIOFx}}$ interrupt response [P = $t_{C(H)}$] (see Notes 9 and 10 and Figure 21)

NO.			TMS320C44-50			TMS320C44-60			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
1	$t_{su(IIOF\text{-}H1L)}$	Setup time, $\overline{\text{IIOFx}}$ before H1 low	11†			11†			ns
2	$t_{w(INT)}$	Pulse duration, to assure one interrupt seen (see Note 11)	P	1.5P	< 2P‡	P	1.5P	< 2P‡	ns

† If this timing is not met, the interrupt is recognized in the next cycle.
‡ This value only applies to level-triggered interrupts and is specified by design but not tested.

NOTES: 9. $\overline{\text{IIOFx}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle can occur.
10. Edge-triggered interrupts require a setup of time (1) and a minimum duration of P. No maximum duration limit exists.
11. Level-triggered interrupts require interrupt-pulse duration of at least 1P wide (P = one H1 period) to assure it will be seen. It must be less than 2P wide to assure it will be responded to only once. Recommended pulse duration is 1.5P.



NOTE A: The 'C44 can accept an interrupt from the same source every two H1 clock cycles.

Figure 21. $\overline{\text{IIOFx}}$ Interrupt-Response Timing [P = $t_{C(H)}$]

timing for $\overline{\text{IACK}}$ (see Note 12 and Figure 22)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{d(H1L-IACKL)}$	Delay time, H1 low to $\overline{\text{IACK}}$ low		9		7	ns
2	$t_{d(H1L-IACKH)}$	Delay time, H1 low to $\overline{\text{IACK}}$ high during first cycle of IACK instruction data read		9		7	ns

NOTE 12: The $\overline{\text{IACK}}$ output is active for the entire duration of the bus cycle and is, therefore, extended if the bus cycle utilizes wait states.

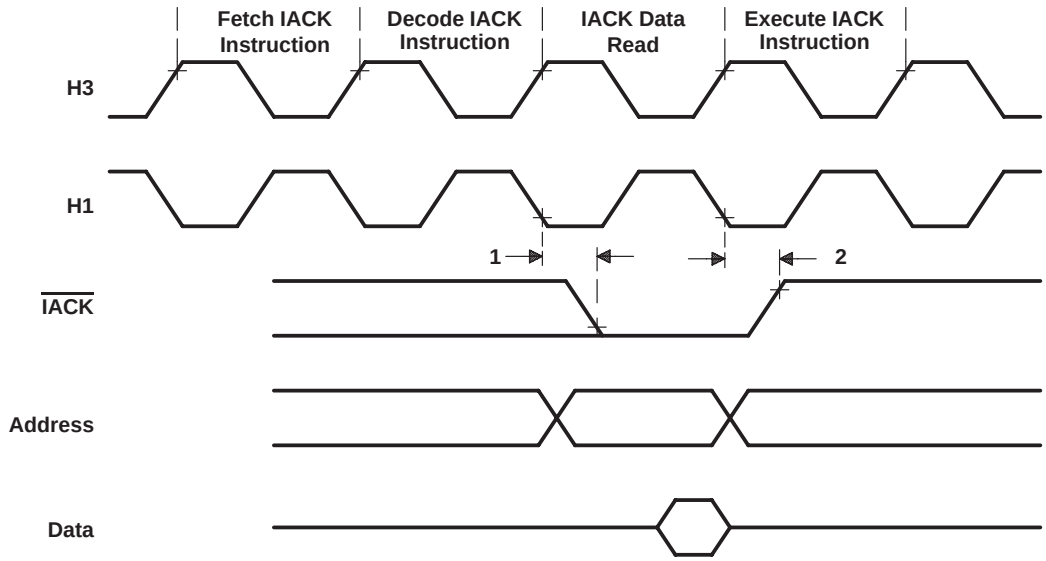
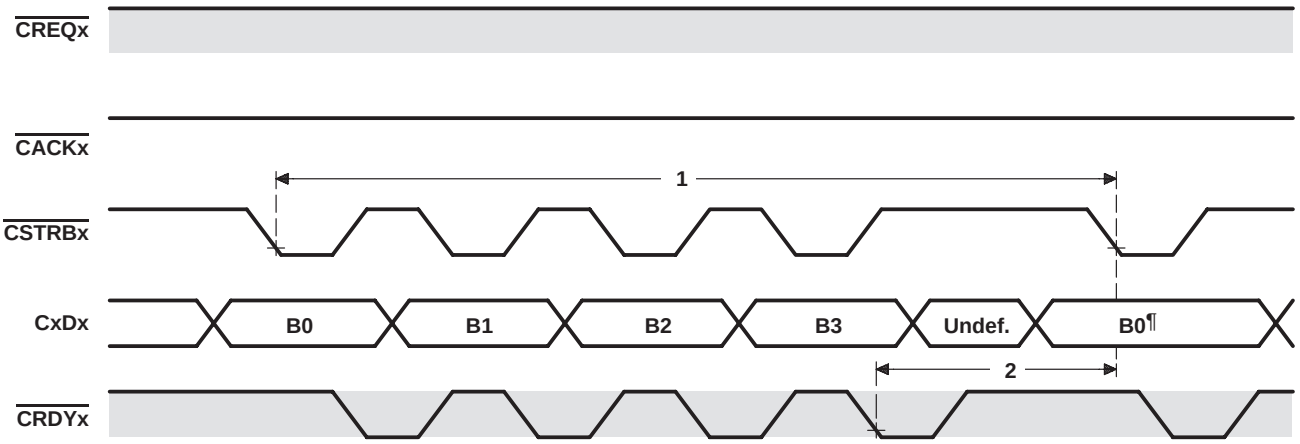


Figure 22. $\overline{\text{IACK}}$ Timing

communication-port word-transfer-cycle timing† [P = $t_{c(H)}$] (see Note 13 and Figure 23)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(WORD)}$‡§	Cycle time, word transfer (4 bytes = 1 word)	1.5P+7	2.5P+170	1.5P+7	2.5P+170	ns
2	$t_{d(CRDYL-CSL)W}$‡	Delay time, $\overline{CRDYx}$ low to $\overline{CSTRBx}$ low between back-to-back write cycles	1.5P+7	2.5P + 28	1.5P+7	2.5P+28	ns

† For these timing values, it is assumed that the 'C4x receiving data is ready to receive data. Line propagation delay is not considered.
‡ This value is characterized but not tested.
§ $t_{c(WORD)}$ max = 2.5P + 28 ns + the maximum summed values of $4 \times t_{d(CSL-CRDYL)R}$, $3 \times t_{d(CRDYL-CSH)}$, $3 \times t_{d(CSH-CRDYH)R}$, and $3 \times t_{d(CRDYH-CSL)W}$ as seen in Figure 24. This timing assumes two 'C4xs are connected.
NOTE 13: These timings apply only to two communicating 'C4xs. When a non-'C4x device communicates with a 'C44, timings can be longer. No restriction exists in this case on how slow the transfer could be except when using early silicon (C40 PG 1.x or 2.x). Refer to the $\overline{CSTRB}$ width restriction section of the *TMS320C4x User's Guide* (literature number SPRU063B).



= When signal is an input (clear = when signal is an output).

¶ Begins byte 0 of the next word.
NOTE A: For correct operation during token exchange, the two communicating 'C4xs must have CLKIN frequencies within a factor of 2 of each other (in other words, at most, one of the 'C4xs can be twice as fast as the other).

Figure 23. Communication-Port Word-Transfer-Cycle Timing [P = $t_{c(H)}$]

communication-port byte-cycle timing (write and read) (see Note 14 and Figure 24)

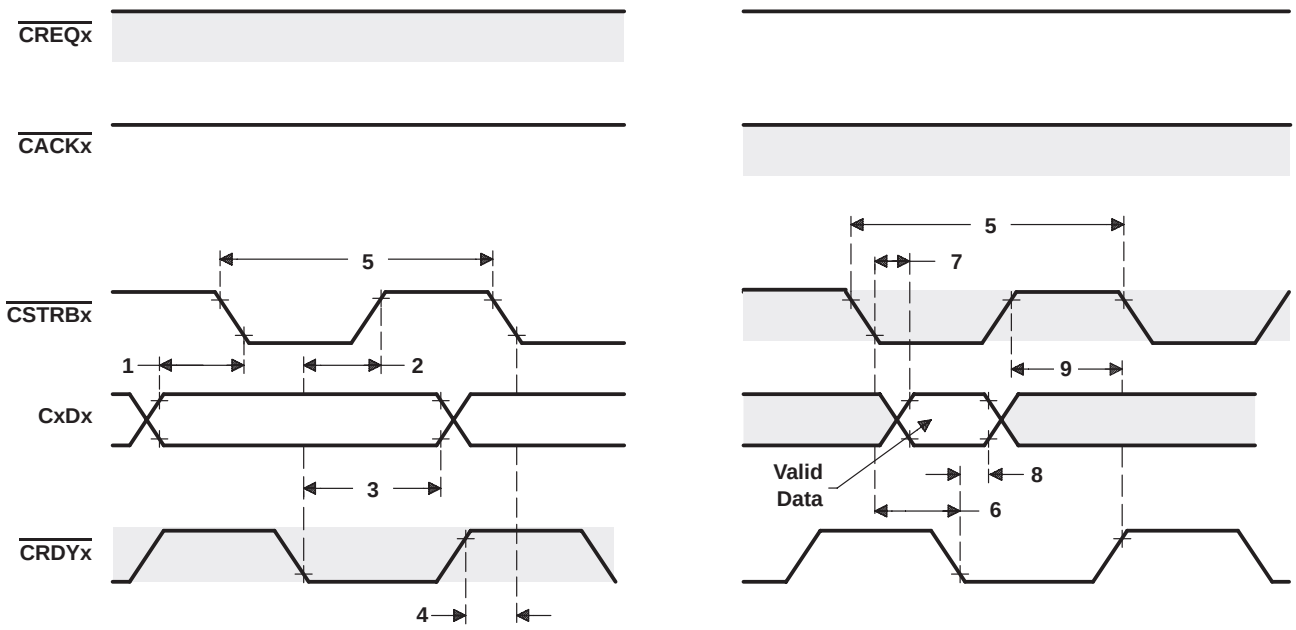
NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{su(CD-CSL)W}$	Setup time, CxDx valid before $\overline{CSTRBx}$ low (write)	2		2		ns
2	$t_{d(CRDYL-CSH)W}$	Delay time, $\overline{CRDYx}$ low to $\overline{CSTRBx}$ high (write)	0†	12	0†	12	ns
3	$t_{h(CRDYL-CD)W}$	Hold time, CxDx after $\overline{CRDYx}$ low (write)	2		2		ns
4	$t_{d(CRDYH-CSL)W}$	Delay time, $\overline{CRDYx}$ high to $\overline{CSTRBx}$ low for subsequent bytes (write)	0†	12	0†	12	ns
5	$t_{c(BYTE)}$‡	Cycle time, byte transfer		44§		44§	ns
6	$t_{d(CSL-CRDYL)R}$	Delay time, $\overline{CSTRBx}$ low to $\overline{CRDYx}$ low (read)	0†	10	0†	10	ns
7	$t_{su(CSL-CD)R}$	Setup time, CxDx valid after $\overline{CSTRBx}$ low (read)	0		0		ns
8	$t_{h(CRDYL-CD)R}$	Hold time, CxDx valid after $\overline{CRDYx}$ low (read)	2		2		ns
9	$t_{d(CSH-CRDYH)R}$	Delay time, $\overline{CSTRBx}$ high to $\overline{CRDYx}$ high (read)	0†	10	0†	10	ns

† This value is specified by design but not tested.

‡ $t_{c(BYTE)}$ max = summed maximum values of $t_{d(CRDY-CSH)}$, $t_{d(CSL-CRDYL)R}$, $t_{d(CSH-CRDYH)R}$, and $t_{d(CRDYH-CSL)W}$. This assumes two ’C4xs are connected.

§ This value is characterized but not tested.

NOTE 14: Communication port timing does not include line length delay.



(a) WRITE TIMING

(b) READ TIMING

= When signal is an input (clear = when signal is an output).

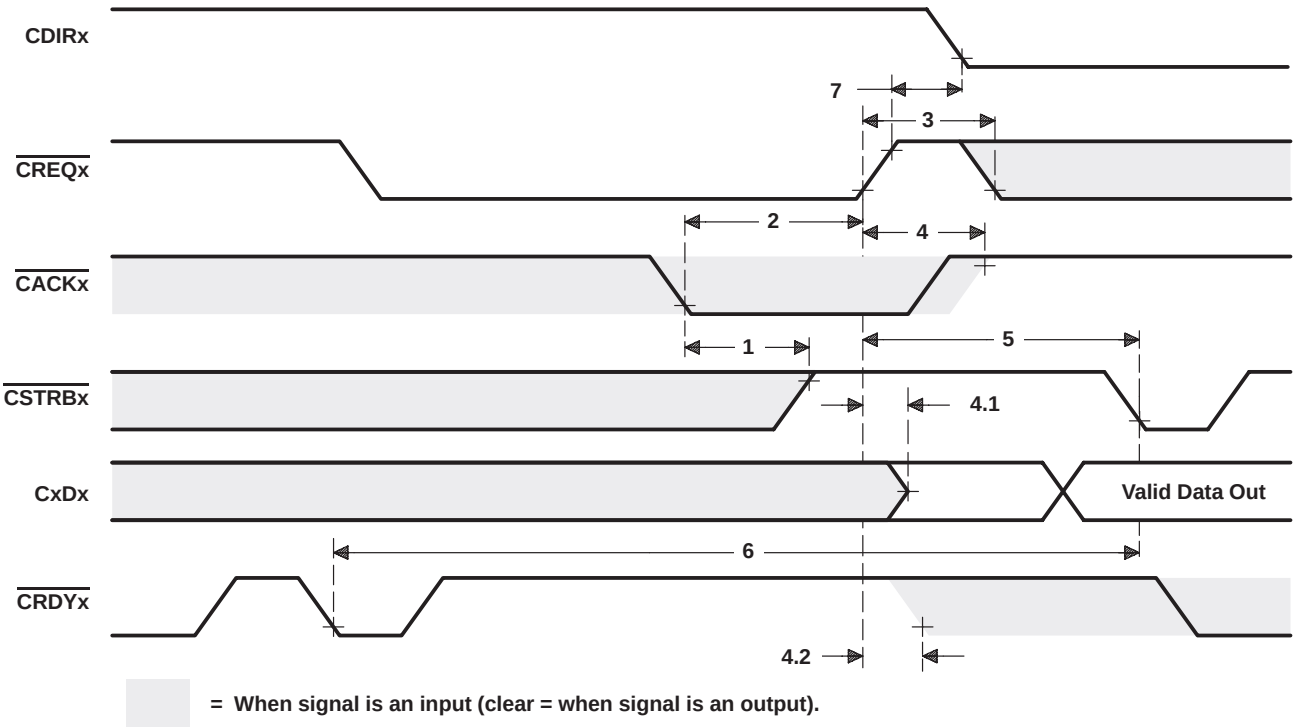
Figure 24. Communication-Port Byte-Cycle Timing (Write and Read)

timing for communication-token transfer sequence, input to an output port [P = $t_{C(H)}$] (see Figure 25)†

NO.			MIN	MAX	UNIT
1‡	$t_{d(CAL-CS)T}$	Delay time, $\overline{CACKx}$ low to $\overline{CSTRBx}$ change from input to a high-level output	0.5P+ 6	1.5P + 22	ns
2‡	$t_{d(CAL-CRQH)T}$	Delay time, $\overline{CACKx}$ low to start of $\overline{CREQx}$ going high for token-request acknowledge	P + 5	2P + 22	ns
3	$t_{d(CRQH-CRQ)T}$	Delay time, start of $\overline{CREQx}$ going high to $\overline{CREQx}$ change from output to an input	0.5P – 5	0.5P + 13	ns
4	$t_{d(CRQH-CA)T}$	Delay time, start of $\overline{CREQx}$ going high to $\overline{CACKx}$ change from an input- to an output-level high	0.5P – 5	0.5P + 13	ns
4.1	$t_{d(CRQH-CD)T}$	Delay time, start of $\overline{CREQx}$ going high to CxDx change from input-driven to output-driven	0.5P – 5	0.5P + 13	ns
4.2	$t_{d(CRQH-CRDY)T}$	Delay time, start of $\overline{CREQx}$ going high to $\overline{CRDYx}$ change from an output to an input	0.5P – 5	0.5P + 13	ns
5	$t_{d(CRQH-CSL)T}$	Delay time, start of $\overline{CREQx}$ going high to $\overline{CSTRBx}$ low for start of word-transfer out	1.5P – 8	1.5P + 9	ns
6	$t_{d(CRDYL-CSL)T}$	Delay time, $\overline{CRDYx}$ low at end of word-input to $\overline{CSTRBx}$ low for word-output	3.5P + 12	5.5P + 48	ns
7	$t_{d(CRQH-CDIRL)}$	Delay time, $\overline{CREQx}$ high to CDIRx low, change from input to output	0.5P – 5	0.5P + 13	ns

† These values are characterized but not tested.

‡ These timing parameters result from synchronizer delays and are referenced from the falling edge of H1. The inputs (that cause the output-signal pins to change values) are sampled on H1 falling. The minimum delay occurs when the input condition occurs just before H1 falling, and the maximum delay occurs when the input condition occurs just after H1 falling.



NOTE A: Before the token exchange, $\overline{CREQx}$ and $\overline{CRDYx}$ are output signals asserted by the ’320C44 receiving data. $\overline{CACKx}$, $\overline{CSTRBx}$, and CxD7 – CxD0 are input signals asserted by the device sending data to the ’C44; these are asynchronous with respect to the H1 clock of the receiving ’320C44. After token exchange, $\overline{CACKx}$, $\overline{CSTRBx}$, and CxD7 – CxD0 become output signals, and $\overline{CREQx}$ and $\overline{CRDYx}$ become inputs.

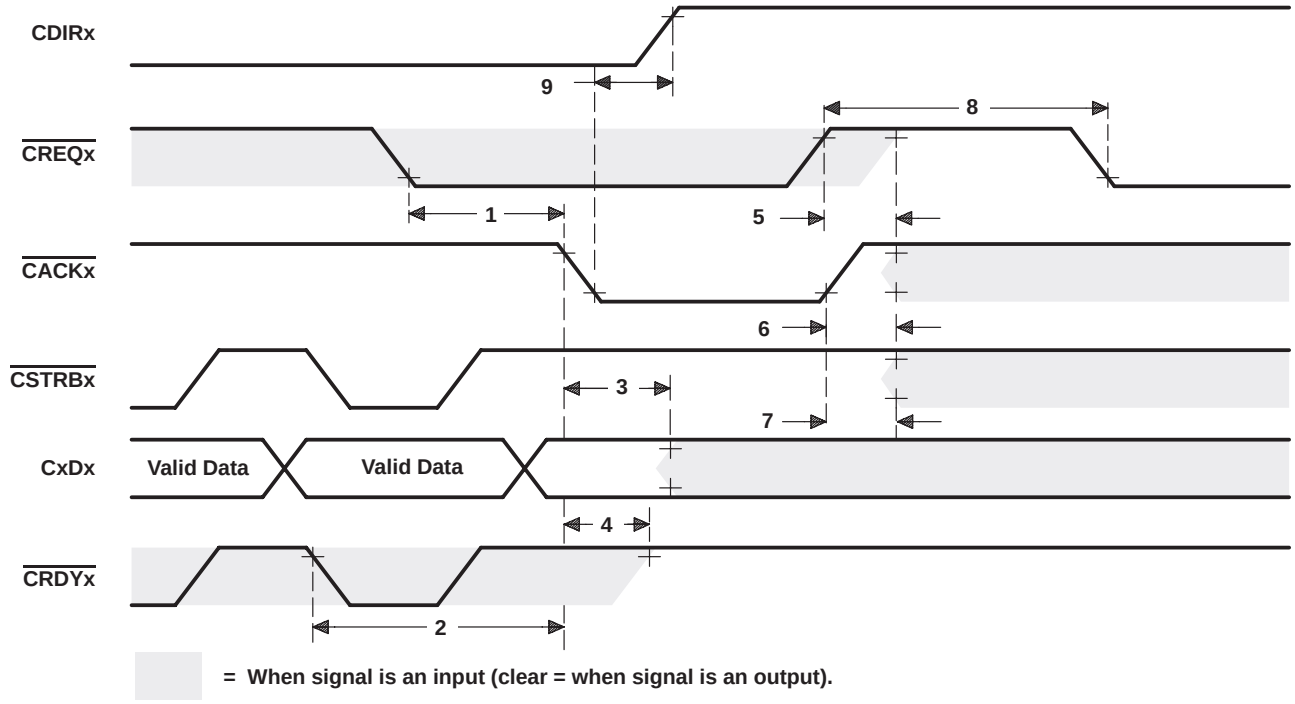
Figure 25. Communication-Token Transfer Sequence, Input to an Output Port [P = $t_{C(H)}$]

timing for communication-token transfer sequence, output to an input port [P = $t_{c(H)}$] (see Figure 26)†

NO.			MIN	MAX	UNIT
1‡	$t_{d(CRQL-CAL)T}$	Delay time, $\overline{CREQx}$ low to start of $\overline{CACKx}$ going low for token-request-acknowledge	P+5	2P+22	ns
2‡	$t_{d(CRDYL-CAL)T}$	Delay time, $\overline{CRDYx}$ low at end of word-transfer out to start of $\overline{CACKx}$ going low	P+6	2P+27	ns
3	$t_{d(CAL-CD)I}$	Delay time, start of $\overline{CACKx}$ going low to CxDx change from outputs to inputs	0.5P–8	0.5P+8	ns
4	$t_{d(CAL-CRDY)T}$	Delay time, start of $\overline{CACKx}$ going low to $\overline{CRDYx}$ change from an input to output, high level	0.5P–8	0.5P+8	ns
5‡	$t_{d(CRQH-CRQ)T}$	Delay time, $\overline{CREQx}$ high to $\overline{CREQx}$ change from an input to output, high level	4	22	ns
6‡	$t_{d(CRQH-CA)T}$	Delay time, $\overline{CREQx}$ high to $\overline{CACKx}$ change from output to an input	4	22	ns
7‡	$t_{d(CRQH-CS)T}$	Delay time, $\overline{CREQx}$ high to $\overline{CSTRBx}$ change from output to an input	4	22	ns
8‡	$t_{d(CRQH-CRQL)T}$	Delay time, $\overline{CREQx}$ high to $\overline{CREQx}$ low for the next token-request	P–4	2P+8	ns
9	$t_{d(CAL-CDIRH)}$	Delay time, $\overline{CACKx}$ low to CDIRx high, change from output to input	0.5P–8	0.5P+10	ns

† These values are characterized but not tested.

‡ These timing parameters result from synchronizer delays and are referenced from the falling edge of H1. The inputs (that cause the output-signal pins to change values) are sampled on H1 falling. The minimum delay occurs when the input condition occurs just before H1 falling, and the maximum delay occurs when the input condition occurs just after H1 falling.



NOTE A: Before the token exchange, $\overline{CACKx}$, $\overline{CSTRBx}$, and CxD7–CxD0 are asserted by the 'C44 sending data. $\overline{CREQx}$ and $\overline{CRDYx}$ are input signals asserted by the 'C44 receiving data and are asynchronous with respect to the H1 clock of the sending 'C44. After token exchange, $\overline{CREQx}$ and $\overline{CRDYx}$ become outputs, and $\overline{CSTRBx}$, $\overline{CACKx}$, and CxD7–CxD0 become inputs.

Figure 26. Communication-Token Transfer Sequence, Output to an Input Port [P = $t_{c(H)}$]

timer-pin timing (see Note 15 and Figure 27)

NO.			MIN	MAX	UNIT
1	$t_{su(TCLK-H1L)}$	Setup time, TCLKx before H1 low	10		ns
2	$t_{h(H1L-TCLK)}$	Hold time, TCLKx after H1 low	0		ns
3	$t_{d(H1H-TCLK)}$	Delay time, TCLKx valid after H1 high		13	ns

NOTE 15: Period and polarity are specified by contents of internal control registers.

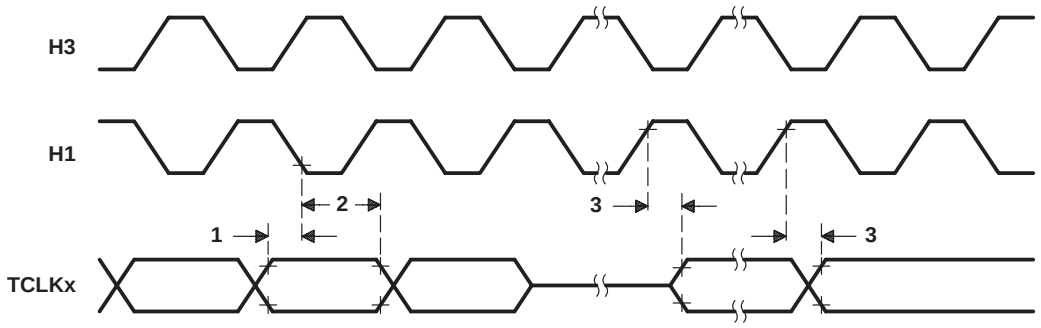


Figure 27. Timer-Pin Timing Cycle

timing for IEEE-1149.1 test access port (see Figure 28)

NO.			TMS320C44-50		TMS320C44-60		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{su(TMS-TCKH)}$	Setup time, TMS/TDI to TCK high	10		10		ns
2	$t_{h(TCKH-TMS)}$	Hold time, TMS/TDI from TCK high	5		5		ns
3	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid	0	15	0	12	ns

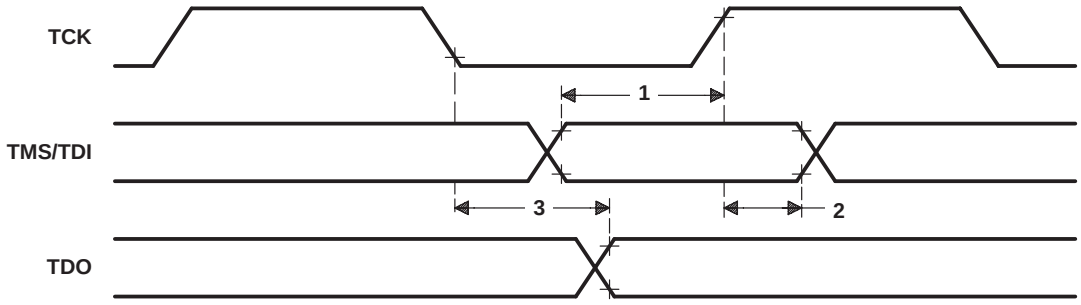
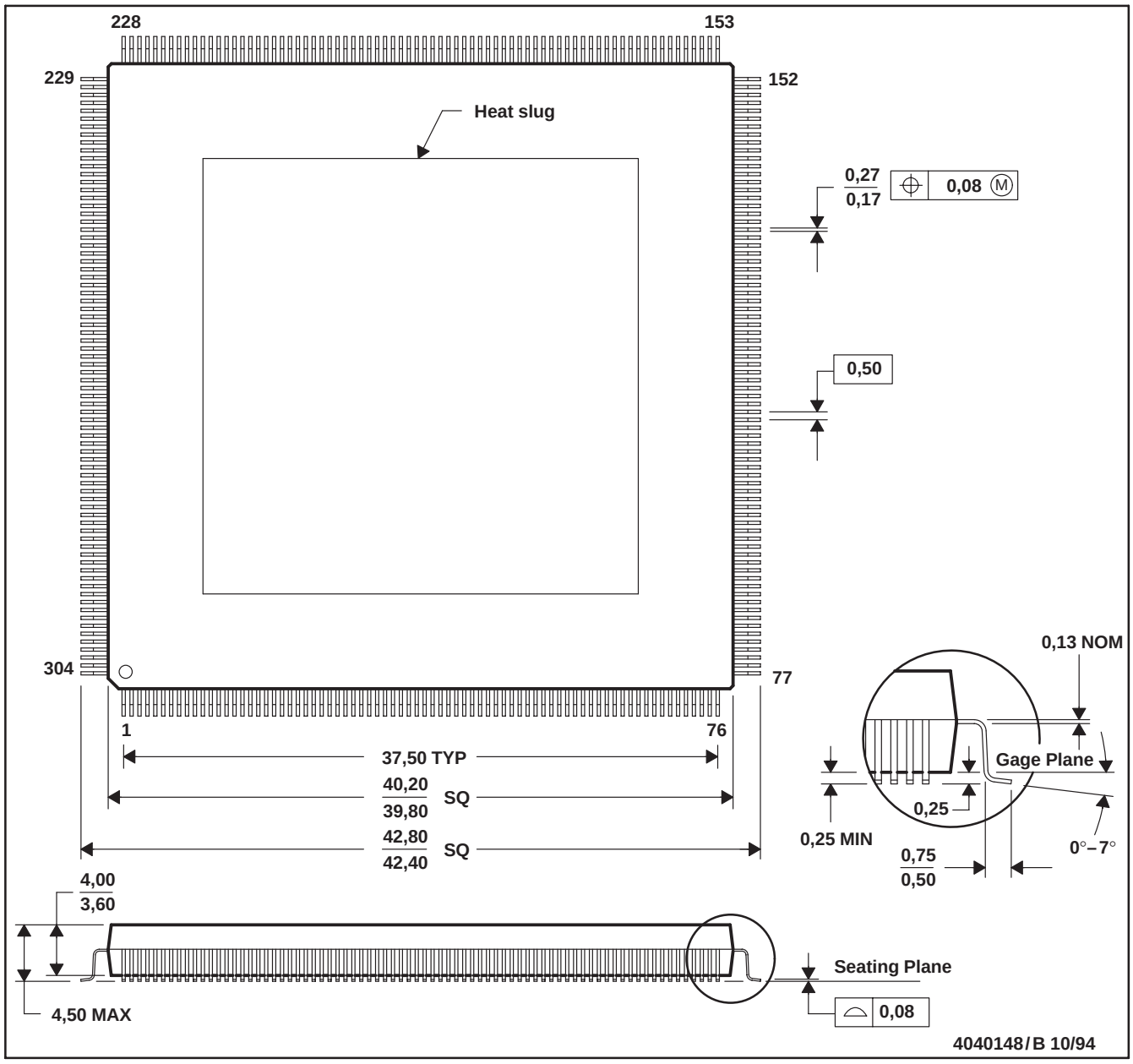


Figure 28. IEEE-1149.1 Test Access Port Timings

MECHANICAL DATA

PDB (S-PQFP-G304) **PLASTIC QUAD FLATPACK (DIE-DOWN)**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Thermally enhanced molded plastic package with a heat slug (HSL)
D. Falls within JEDEC MO-143

Thermal Resistance Characteristics					
Parameter	°C/W	Air Flow LFPM	Parameter	°C/W	Air Flow LFPM
$R\Theta_{JC}$	0.8	N/A	$R\Theta_{JA}$	12.1	250
$R\Theta_{JA}$	16.0	0	$R\Theta_{JA}$	10.0	500
$R\Theta_{JA}$	14.2	100			

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