Precision Sample and Hold Amplifier

FEATURES

- *Guaranteed* 6μs Max. Acquisition Time
- *Guaranteed* 0.005% Max. Gain Error
- *Guaranteed* 1mV Max. Offset Voltage
- *Guaranteed* 1mV Max. Hold Step
- Very Low Feedthrough 86dB Min.
- High Input Impedance under All Conditions
- Logic Inputs Compatible with All Logic Families

APPLICATIONS

- 12-Bit Data Acquisition Systems
- Ramp Generators
- Analog Switches
- Staircase Generators
- Sample and Difference Circuits

DESCRIPTION

The LF198 is a precision sample and hold amplifier which uses a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. A typical offset voltage of 1mV and gain error of 0.002% allow this sample and hold amplifier to be used in 12-bit systems. Dynamic performance can be optimized by proper selection of the external hold capacitor. Acquisition times can be as low as 4μs for small capacitors while hold step and droop errors can be held below 0.1mV and 30μV/sec respectively when using larger capacitors.

The LF198 is fixed at unity gain with $10^{10}\Omega$ input impedance independent of sample/hold mode. The logic inputs are high impedance differential to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The device will operate over a wide supply voltage range from ±5V to ±18V with very little change in performance, and key parameters are specified over this full supply range.

The LF198A version offers tightened electrical specifications for key parameters.

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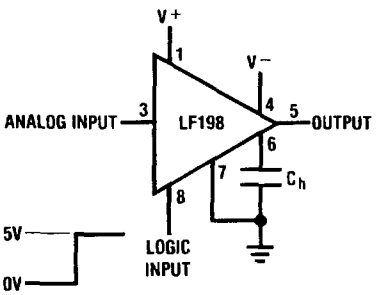
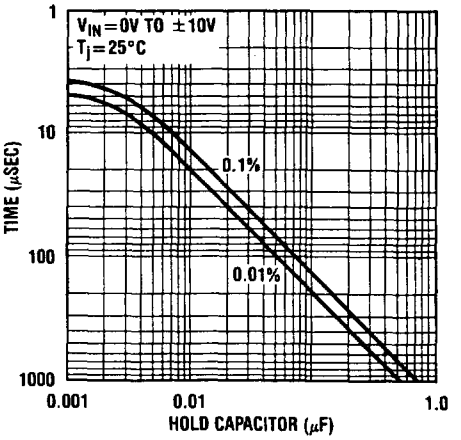
Basic Sample and Hold



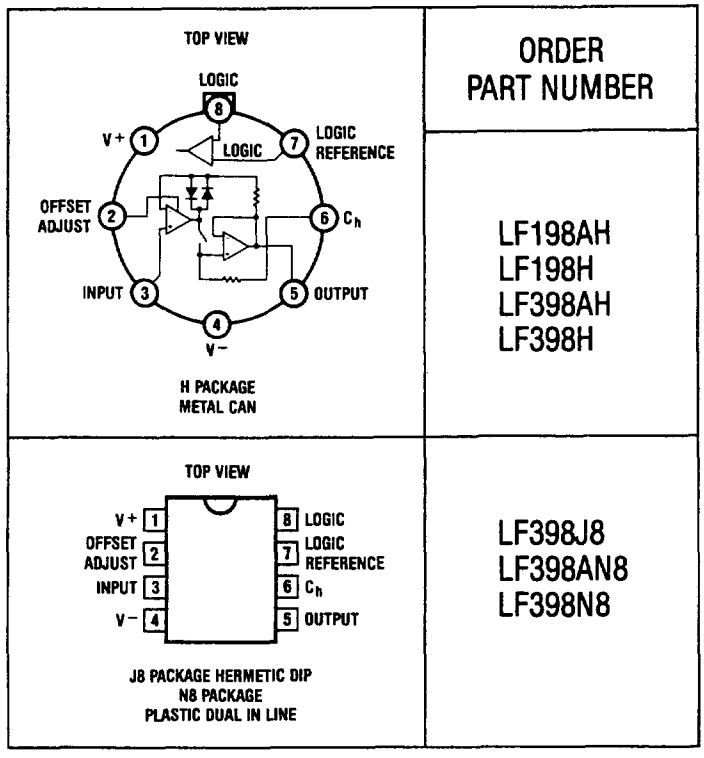
Acquisition Time



ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... Equal to Supply Voltage
Logic to Logic Reference Differential
Voltage (Note 2) ..... +30V, −30V
Output Short Circuit Duration ..... Indefinite
Hold Capacitor Short Circuit Duration ..... 10 sec
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Supply Voltage ..... ±18V
Power Dissipation (Package Limitation)
(Note 1) 500mW
Operating Temperature Range
LF198/LF198A ..... −55°C to 125°C
LF398/LF398A ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LF198AH LF198H LF398AH LF398H
LF398J8 LF398AN8 LF398N8

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LF198A MIN	LF198A TYP	LF198A MAX	LF398A MIN	LF398A TYP	LF398A MAX	UNITS
Input Offset Voltage (Note 6)		 •		0.5	1 2		1	2 3	mV mV
Input Bias Current (Note 6)		 •		5	25 75		10	25 50	nA nA
Input Impedance				10^{10}			10^{10}		Ω
Gain Error	$R_L = 10k$	 •		0.001	0.005 0.01		0.001	0.005 0.01	% %
Feedthrough Attenuation Ratio at 1kHz	$C_h = 0.01\mu F$		86	96		86	96		dB
Output Impedance	"HOLD" Mode	 •		0.5	1 4		0.5	1 6	Ω Ω
"HOLD" Step (Note 4)	$C_h = 0.01\mu F$, $V_{OUT} = 0$			0.25	1		0.25	1	mV
Supply Current (Note 6)	$T_j \geq 25°C$			4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current				2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)			10	100		10	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$			4 16	6 25		4 16	6 25	μs μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$			5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$		90	110		90	110		dB
Differential Logic Threshold			0.8	1.4	2.4	0.8	1.4	2.4	V

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LF198 MIN	LF198 TYP	LF198 MAX	LF398 MIN	LF398 TYP	LF398 MAX	UNITS
Input Offset Voltage (Note 6)				1	3		2	7	mV
		●			5			10	mV
Input Bias Current (Note 6)				5	25		10	50	nA
		●			75			100	nA
Input Impedance				10^{10}			10^{10}		Ω
Gain Error	$R_L = 10k$			0.002	0.005		0.004	0.01	%
		●			0.02			0.02	%
Feedthrough Attenuation Ratio at 1kHz	$C_h = 0.01\mu F$		86	96		80	96		dB
Output Impedance	"HOLD" Mode			0.5	2		0.5	4	Ω
		●			4			6	Ω
"HOLD" Step (Note 4)	$C_h = 0.01\mu F$, $V_{OUT} = 0$			0.5	2.0		0.5	2.5	mV
Supply Current (Note 6)	$T_j \geq 25°C$			4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current				2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)			30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$			4			4		μs
	$C_h = 0.01\mu F$			16			16		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$			5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$		80	110		80	110		dB
Differential Logic Threshold			0.8	1.4	2.4	0.8	1.4	2.4	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: T_j max for the LF198/LF198A is 150°C; T_j max for the LF398/LF398A is 100°C.

Note 2: The logic inputs are protected to ±30V differential as long as the voltage on both pins does not exceed the supply voltage. For proper operation, however, both logic and logic reference pins must be at least 2V below the positive supply and one of these pins must be at least 3V above the negative supply.

Note 3: Unless otherwise noted, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, $R_L = 10k\Omega$ and unit is in "sample" mode. Logic reference = 0V and logic voltage = 2.5V.

Note 4: The hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters are guaranteed over a supply voltage range of ±5V to ±18V.

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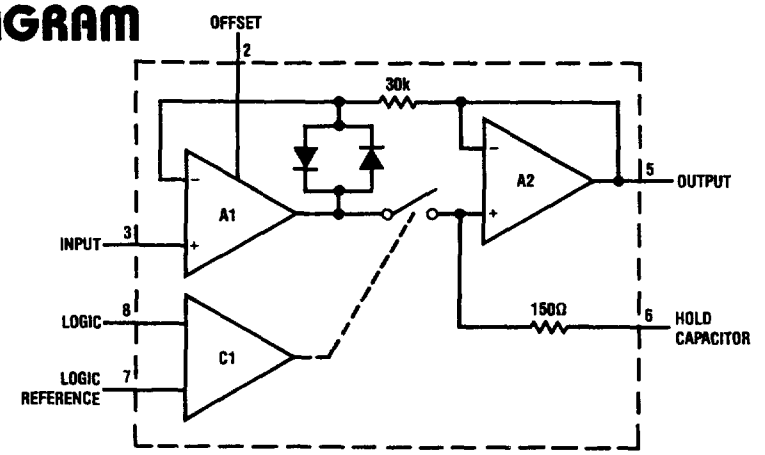
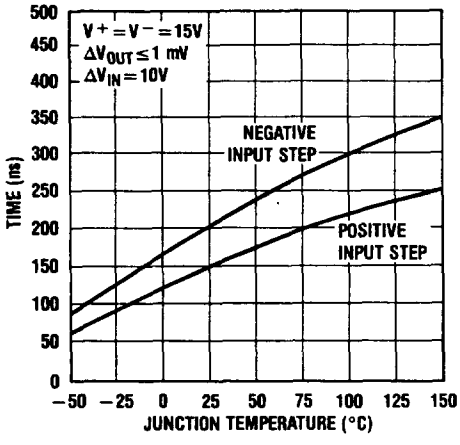
FUNCTIONAL DIAGRAM



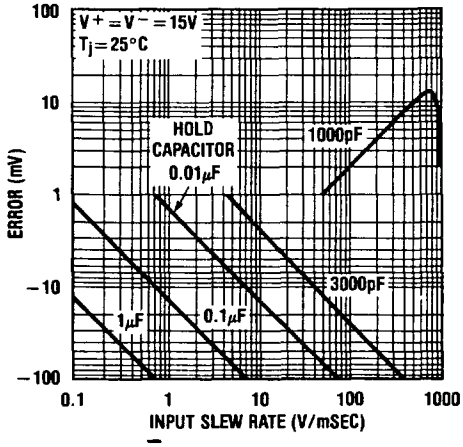
TYPICAL PERFORMANCE CHARACTERISTICS

Aperture Time*



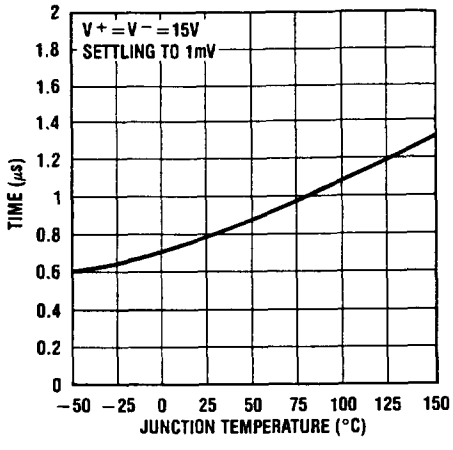
*See Definition of Terms

Dynamic Sampling Error*



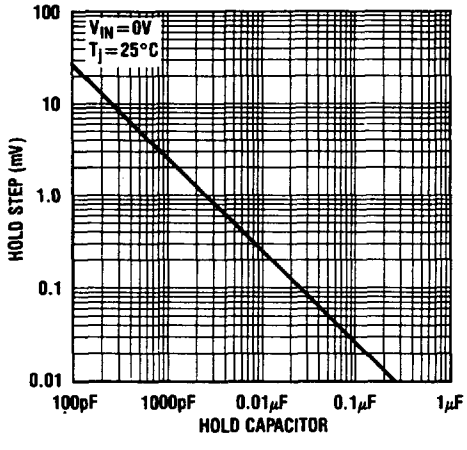
*See Definition of Terms

"Hold" Settling Time*

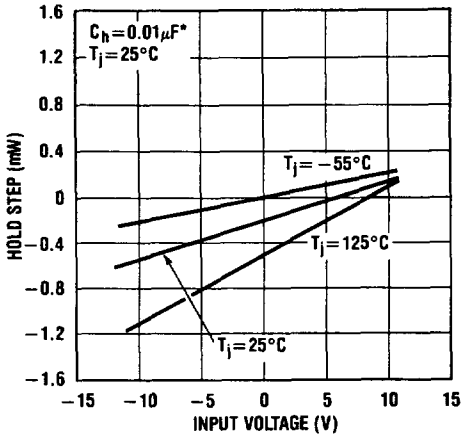


*See Definition of Terms

Hold Step

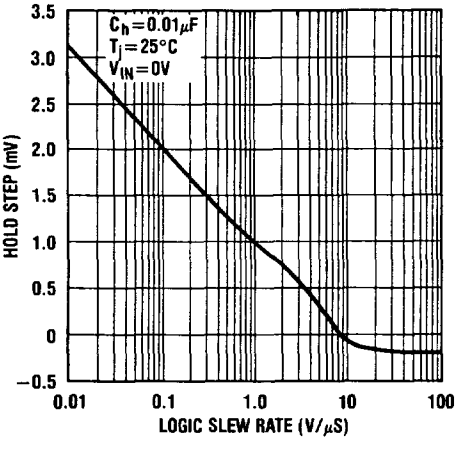


Hold Step vs Input Voltage

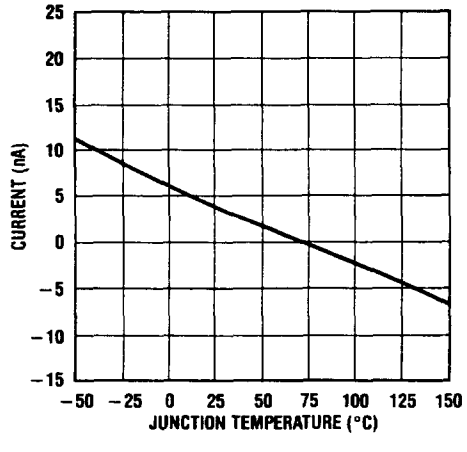


*Amplitude of hold step scales inversely with hold capacitor value

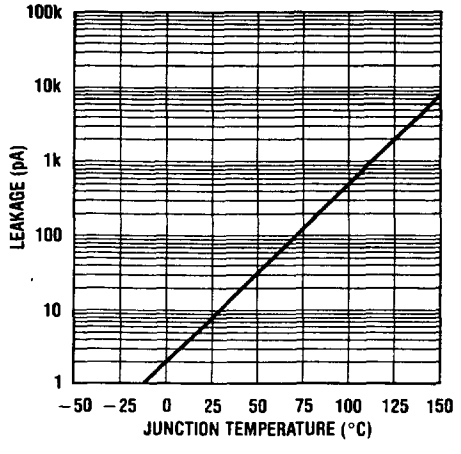
Hold Step vs Logic Slew Rate



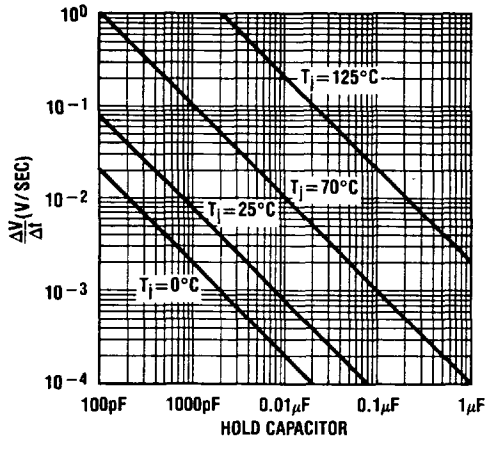
Input Bias Current



Capacitor Pin Leakage

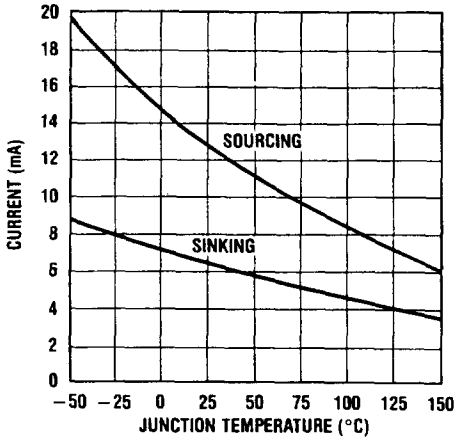


Output Droop Rate

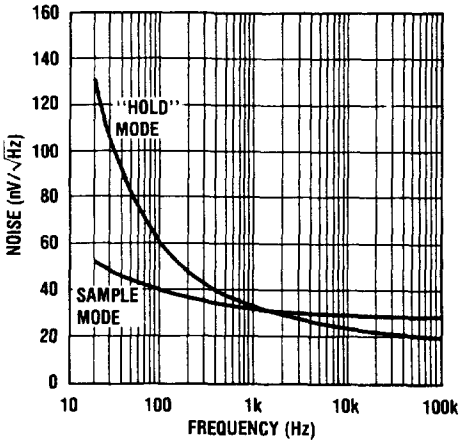


TYPICAL PERFORMANCE CHARACTERISTICS

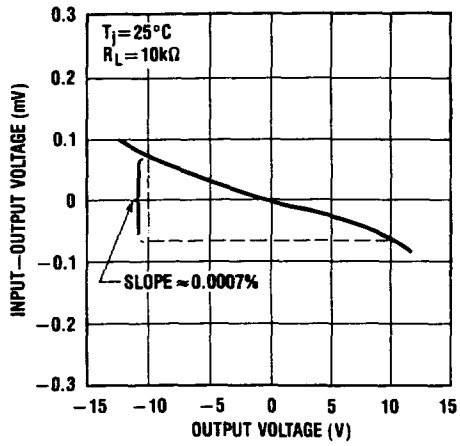
Output Short Circuit Current



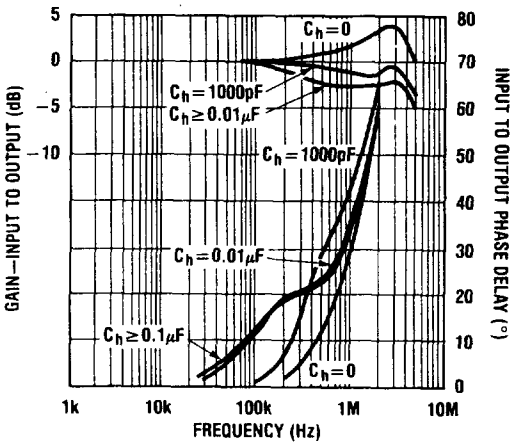
Output Noise



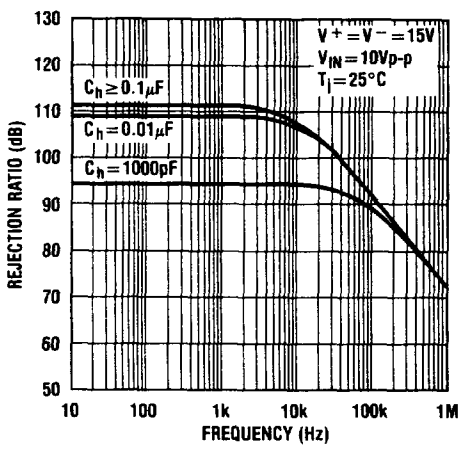
Gain Error



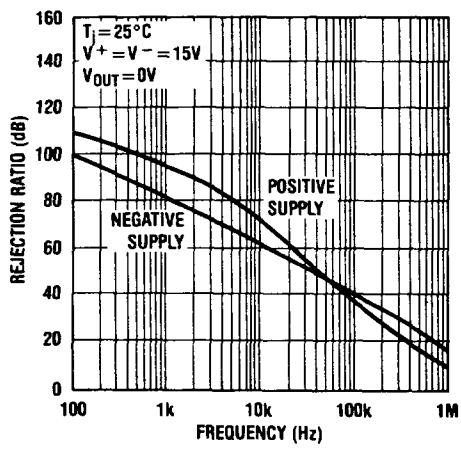
Phase and Gain (Input to Output, Small Signal)



Feedthrough Rejection Ratio



Power Supply Rejection



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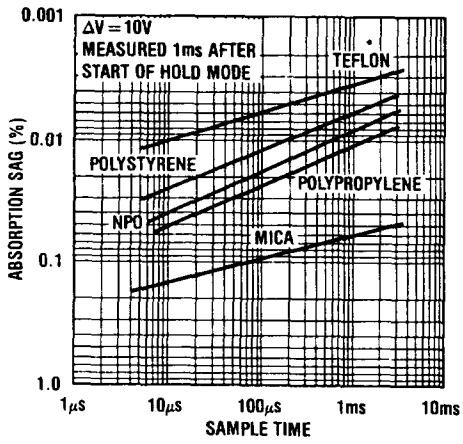
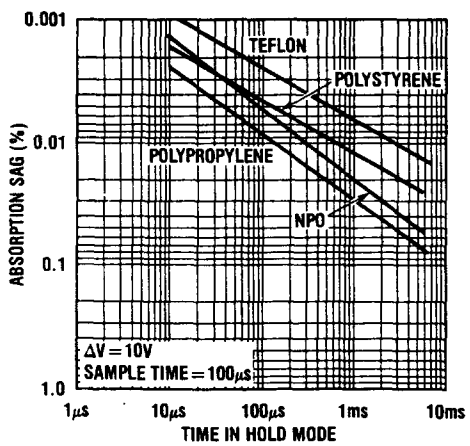
Capacitor Dielectric Absorption

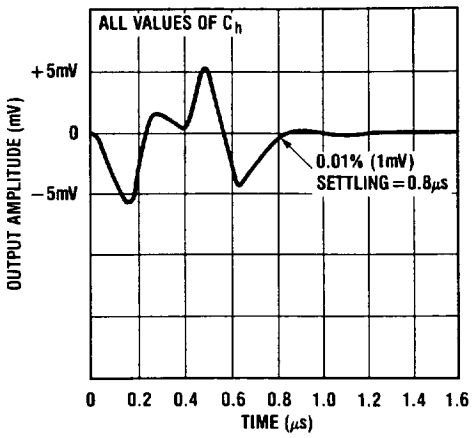


Capacitor Dielectric Absorption

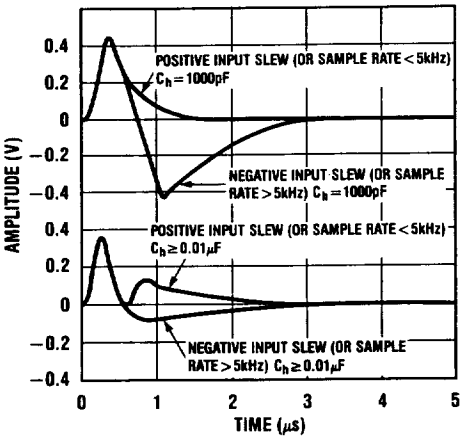


TYPICAL PERFORMANCE CHARACTERISTICS

Output Transient at Start of Hold Mode



Output Transient at Start of Sample Period



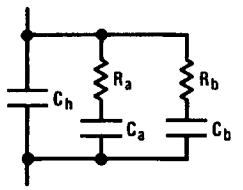
APPLICATIONS INFORMATION

Hold Capacitor

For fast sample and hold applications, the size of the hold capacitor is critical. A low value will give fast acquisition, but will also increase errors due to hold step, and droop caused by amplifier bias current. The capacitor should be made as large as possible, consistent with acquisition time and dynamic sampling error requirements. Capacitors larger than 0.1μF have an additional problem. They are generally not available in the low loss dielectrics like Teflon, Polystyrene, and NPO, at least not at a reasonable price and size. Mylar, even with its poor dielectric absorption properties, may be a reasonable choice where very long sample times are used and low droop rates are needed.

Dielectric absorption in the hold capacitor can often be the major source of error in a sample and hold. The equivalent "circuit" of a typical capacitor is shown below with parallel RC networks used to model dielectric absorption.

Typical Hold Capacitor Equivalent Circuit



C_a, $C_b \approx 0.01$ TO 0.1 C_h
R_a, R_b GENERATE TIME CONSTANTS OF 0.1-50 MILLISECONDS WITH C_a, C_b

One can see that rapid changes in capacitor voltage will not be tracked by the internal parasitic capacitors because of the resistance in series with them. This leads to a "sag" effect in the hold capacitor after a sudden change in voltage followed by rapid switch to the hold mode. The capacitor remembers its previous state via the charge on the internal parasitic capacitance and sags

APPLICATIONS INFORMATION

back slightly toward the previous voltage. The magnitude of the sag depends on the voltage change and the time spent sampling the new voltage. Several time constants are typically evident in the sag, although some capacitors tend to exhibit a single time constant, while others show a sag that indicates a blending of many time constants. The curves labeled CAPACITOR DIELECTRIC ABSORPTION show the amount of sag found after a 10V step with sample time at the new voltage and hold time at the new voltage as variables. It is obvious that sag problems are minimized by long sample times and short hold times. This is often in conflict with basic sampling requirements, but one point should be made: if at all possible, keep the sample and hold amplifier in the "tracking", or sampling, mode as much as possible to maximize the time the hold capacitor spends near the voltage at which it will eventually "hold".

The best capacitor for sample and hold applications is Teflon. It is clearly superior with regard to dielectric absorption and operates over the full −55°C to 125°C temperature range. If size or price becomes a problem, the second choice for full temperature range operation is "NPO", or "COG" ceramic units. Some care must be used here—not all NPO capacitors use the low dielectric constant ceramic necessary for low dielectric absorption. For lower temperatures ($\leq$70°C), Polystyrene has traditionally been the best hold capacitor. The best units are cylindrical and fairly large—there seems to be a strong correlation between small size and poorer dielectric performance. Polypropylene has nearly the same absorption properties as polystyrene and offers 85°C operation. It also tends to be smaller. Again, stay with cylindrically wrapped units. Other standard dielectrics such as mica, glass, mylar, and ordinary ceramic are much worse with regard to dielectric absorption. Mylar is sometimes used for large values when the ratio of sample to hold time is large and extremely low droop is required.

Dynamic Sampling Error

A significant sampling error can occur in any sample and hold if the input is moving when the unit is put into the hold mode. The two major causes for this error are digital delay in switch opening and analog delay across the hold capacitor. The switch opening delay is obvious and leads to a "held" output error of $(dv/dt) \times (T_d)$, where dv/dt is the slew rate of the input signal and T_d is switch delay. In the case of the LF198, T_d is approximately 150ns, giving a 4.5mV error when sampling the zero crossing of a 5V (peak) sine wave at 1kHz ($dv/dt = A \cdot 2\pi f = 5 \cdot 2\pi \cdot 10^3$). The analog delay is the difference between input signal and capacitor voltage. It is determined by the RC product of the hold capacitor and the effective series resistance, which in the case of the LF198 is about 150Ω. This analog delay with a 0.01μF hold capacitor is $R \cdot C = 150 \times 10^{-8} = 1.5\mu s$, or about ten times the delay of the switch. The sign of the analog delay is negative—the held output is related in time to the input voltage *before* the hold command was given. The overall dynamic sampling error is the sum of the digital and analog errors. The curve labeled *Dynamic Sampling Error* will be helpful in estimating these errors as a function of input slew rate and hold capacitor size.

Dynamic sampling error can be reduced by a factor of ten or more by inserting a delay in the logic input so that the "hold" command is delayed by an amount equal to the RC time constant of the LF198 and external hold capacitor. For a 0.01μF hold capacitor and the 150Ω resistor internal to the LF198, this is 1.5μs. A simple RC network can be used in front of the logic input for delays up to $\approx$1μs. Longer delays require the addition of a logic gate to speed up the rise time of the delayed signal. See LOGIC RISE TIME in this section for further details.

Hold Step

Hold step is the small voltage step (after settling) seen at the output of a sample and hold amplifier when it is switched from the sample mode to the hold mode with a steady DC input. Hold step is typically the result of, or can be modeled as, a fixed quantity of charge transferred to the hold capacitor as a result of the internal switching that occurs during the hold command. In the case of the LF198, that charge is about 5 picocoulombs, giving a hold step of 0.5mV for a 0.01μF hold capacitor and 5mV for a 1000pF hold capacitor. ($V = Q/C$.) Hold step is reasonably independent of logic amplitude if care is taken to minimize the stray capacitance between the logic input

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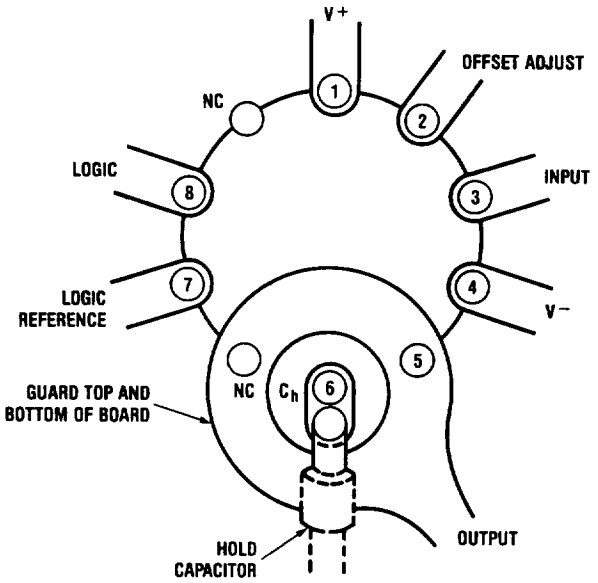
APPLICATIONS INFORMATION

and the hold capacitor. With thoughtful layout, including the guarding technique shown below, stray capacitance should be under 0.3pF, limiting charge variations to less than 0.3 picocoulombs per volt.

Guarding Technique



BOTTOM VIEW

Use 10-pin layout. Guard around C_h is tied to output.

Hold step varies slightly with analog input voltage (see curves). A typical unit will change at 0.4 picocoulombs per volt. This manifests itself as a gain error when the amplifier is switched to the hold mode. With a 0.01μF capacitor, the resulting gain error will be (0.4 PC/V)/0.01μF = 0.004%. This gain error is in the opposite direction of DC (sample mode) gain error. At high values of hold capacitor, DC gain error will dominate and gain will be slightly below unity (0.002%). For low value capacitors (< 0.01μF), hold step induced gain error will dominate and hold mode gain will be slightly above unity. Zeroing out hold step does not change the variation of hold step with regard to input voltage.

Offset Zeroing

A sample and hold amplifier has two distinct offset voltages. The first is just the DC offset of the amplifier while in the sample or "tracking" mode. It is identical to the input offset of any operational amplifier. The second offset voltage is the sum of the DC offset plus a dynamic term called hold step. Hold step is a change in output voltage when the amplifier is switched from sample mode to hold mode, with the input held steady. This second offset is often called hold mode offset. It can be less than or much greater than the DC offset, depending on the magnitude and sign of hold step.

A fairly accurate model for hold step is a fixed charge injected into the hold capacitor by the switch turn-off circuitry. The magnitude of the charge is reasonably independent of logic input amplitude. The resulting change in hold capacitor voltage is Q/C_h. The charge, Q, is typically 5 picocoulombs, giving a 0.5mV hold step with a 0.01μF hold capacitor. Since most sample and hold amplifiers are "used," i.e., have their outputs read by an A to D converter, etc., during the hold mode, hold mode offset is arguably much more important than sample mode DC offset.

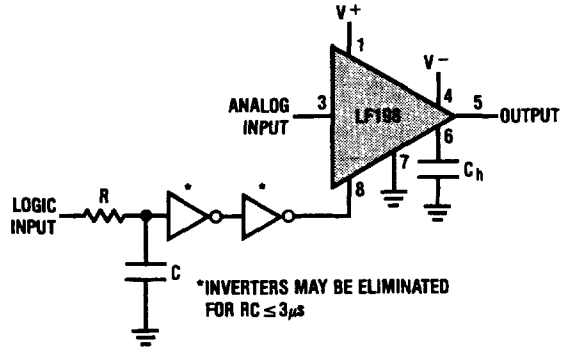
DC offset adjustment is accomplished with a 1k low TC cermet potentiometer tied to V^+ with 0.6mA flowing through it and the wiper tied to pin 2. This allows pin 2 to be moved ±300mV around its nominal voltage (0.3V below V^+). Offset adjustment range is ±9mV, and the adjustment procedure nominally improves offset drift when the DC offset is reduced to zero. This offset method *can* be used to zero out hold mode offset, but at the expense of some induced offset drift. Each millivolt of hold step offset that is corrected by this method introduces 3.3μV/°C drift. For 0.002μF or larger hold capacitors where hold step is a few millivolts or less, this is a practical solution to hold mode offset. In precision wide temperature range applications, or where C_h is less than 0.002μF, a separate hold mode zeroing method should be used. The circuit shown in the application section using a logic inverter and a 5pF capacitor is recommended (DC AND AC ZEROING).

APPLICATIONS INFORMATION

Logic Fall Time

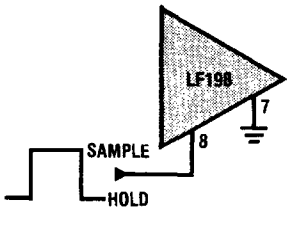
Hold step is independent of logic input fall time only for fall times faster than 10V/μs. For instance, as logic fall time changes from 10V/μs to 1V/μs, hold step with a 0.01μF hold capacitor will typically increase from 0.25mV to 1.0mV. See the curve labeled HOLD STEP vs LOGIC SLEW RATE for further data points. If logic slew rate is not constant, use the value at the threshold point (1.5V with respect to logic reference). An RC network will have a discharge slew rate of V_L/RC, where V_L is the logic threshold of the LF198. The delay generated by the network will be $RC \cdot \ln(V^+/V_L)$, where V^+ is logic amplitude. For a 1μs delay, with 5V logic, an RC time constant of 0.8μs is needed. This has a slew rate of 2V/μs at threshold, which will slightly degrade hold step. It is obvious that an RC delay network significantly longer then 1μs will have a large effect on hold step. If longer delays are required, they should be followed by several inverter stages or a Schmitt trigger to increase slew rate.

Adding Delay to Logic Input



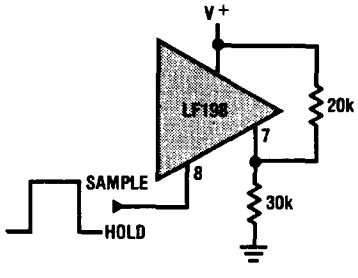
LOGIC INPUT CONFIGURATIONS*

TTL and CMOS
$3V \leq V_L$ (Hi State) $\leq 10V$



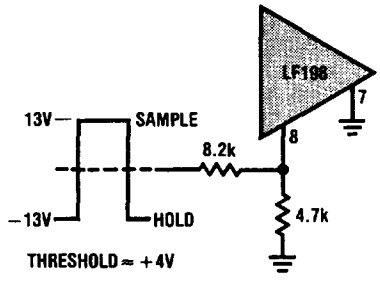
THRESHOLD = 1.4V

CMOS
$7V \leq V_L$ (Hi State) $\leq 15V$

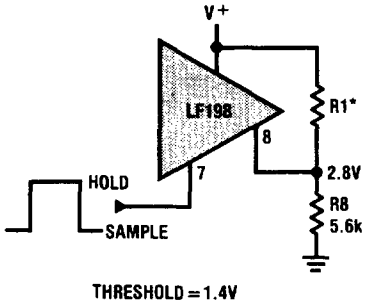


THRESHOLD = 0.6 (V+) + 1.4V

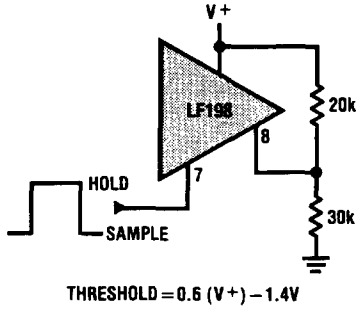
Op Amp Drive



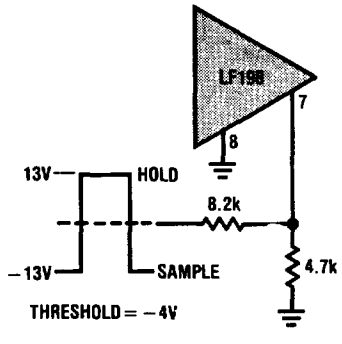
THRESHOLD ≈ +4V



THRESHOLD = 1.4V
*SELECT FOR 2.8V AT PIN 8



THRESHOLD = 0.6 (V+) − 1.4V



THRESHOLD = −4V

*The logic input signal high state must be at least 2V below the positive supply voltage of the LF198.

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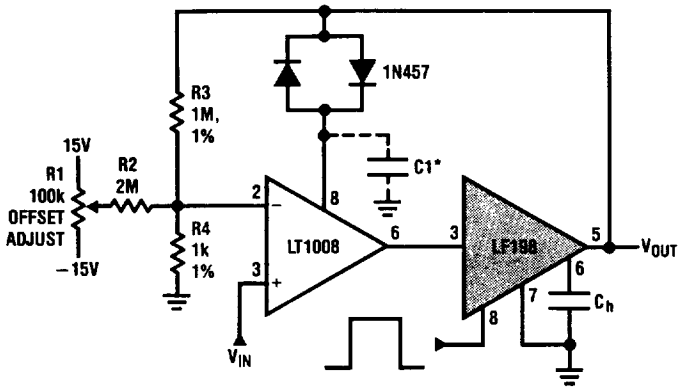
TYPICAL APPLICATIONS

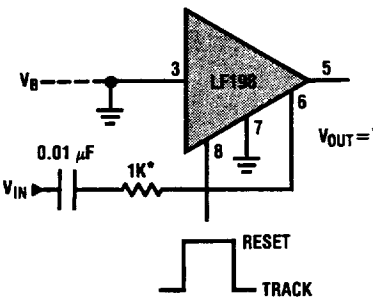
X1000 Sample and Hold



*FOR LOWER GAINS, THE LT1008 MUST BE FREQUENCY COMPENSATED

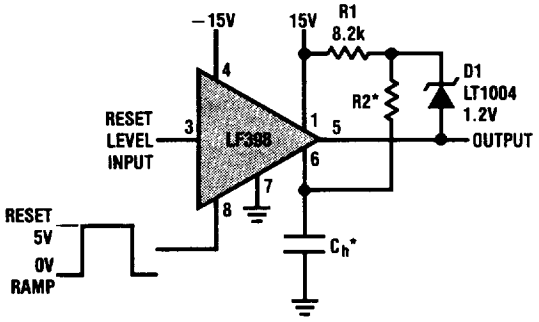
USE $\approx \frac{100}{A_V}$pF FROM COMP 2 TO GROUND

Sample and Difference Circuit (Output Follows Input in Hold Mode and Resets to V_B in Sample Mode)



*THIS RESISTOR PROTECTS INPUT FROM SURGE CURRENTS, BUT INCREASES SAMPLE TIME. IT CAN BE ELIMINATED IF INPUT IS OTHERWISE PROTECTED.

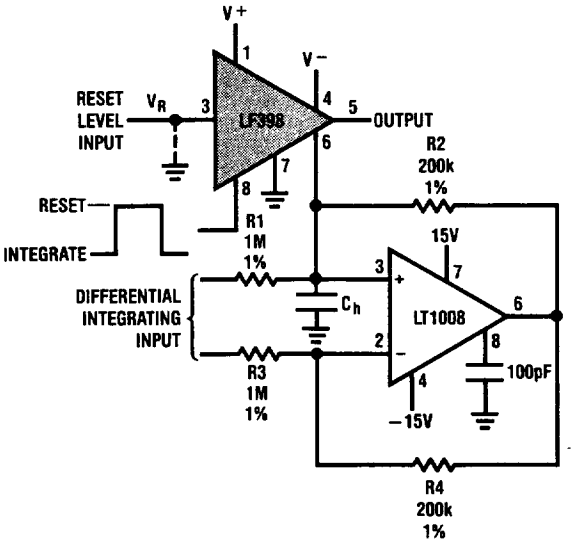
Ramp Generator with Variable Reset Level



*SELECT FOR RAMP RATE $\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)C_h)}$

$R \geq 10k$

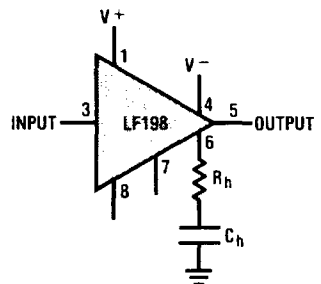
Integrator with Programmable Reset Level



V_{OUT} (HOLD MODE) $= \left[\frac{1}{(R1)C_h}\int_0^t V_{IN} dt\right] + \left[V_R\right]$

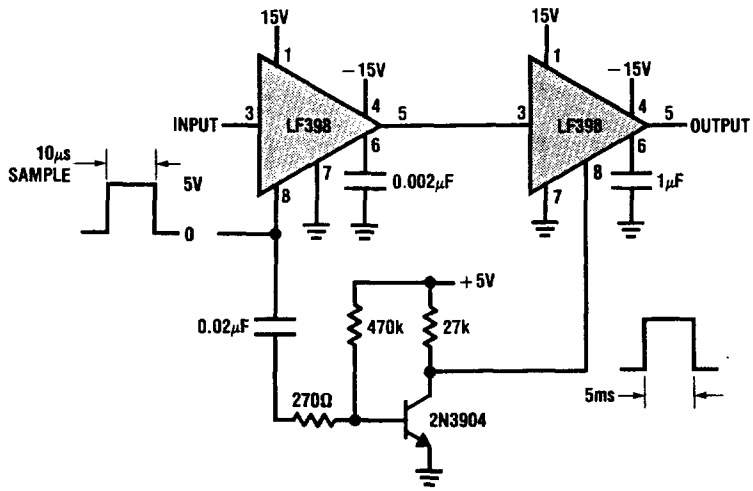
TYPICAL APPLICATIONS

Output Holds at Average of Sampled Input

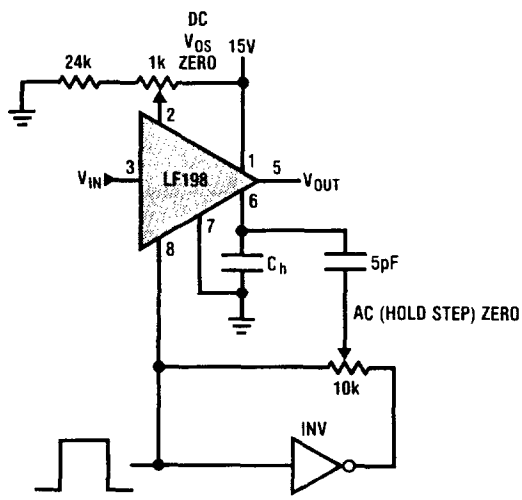


SELECT $(R_h)(C_h) >> \frac{1}{2\pi f_{IN}(Min)}$

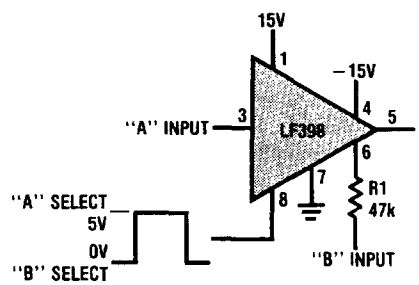
Fast Acquisition, Low Droop Sample and Hold



DC and AC Zeroing



2-Channel Switch



	A	B
Gain	1 ± 0.02%	1 ± 0.2%
Z_{IN}	$10^{10}\Omega$	47kΩ
BW	≃1MHz	≈400kHz
Crosstalk @1kHz	−90dB	−90dB
Offset	≤6mV	≤75mV

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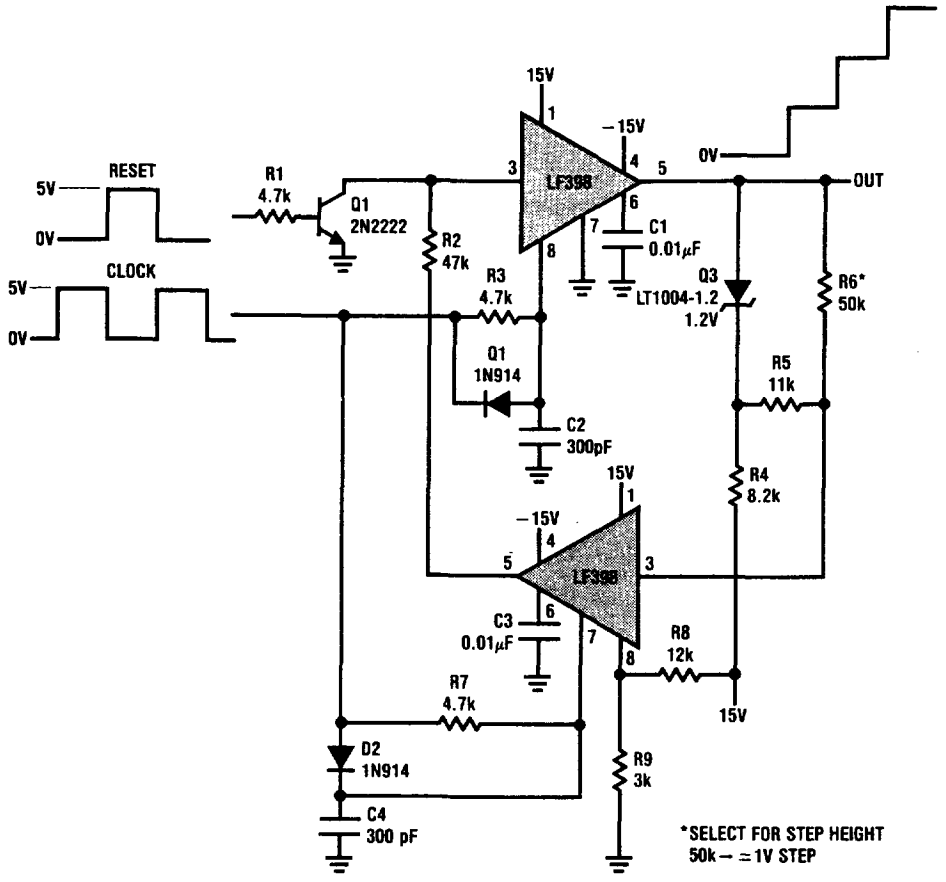
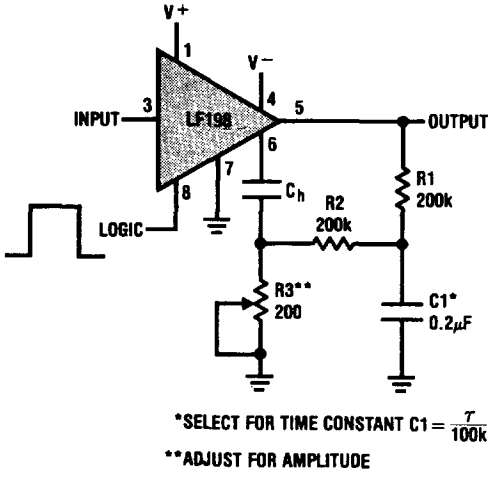
TYPICAL APPLICATIONS

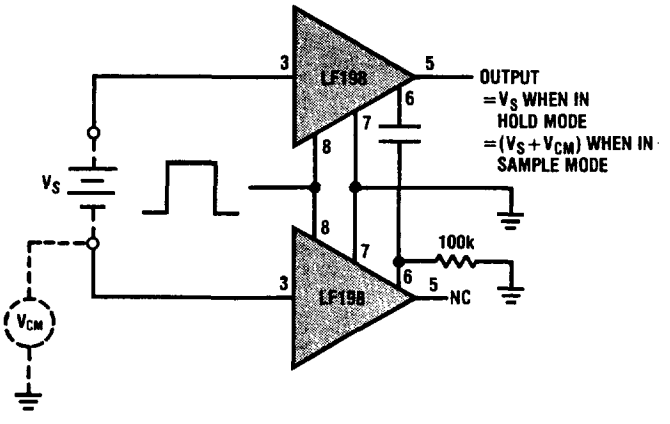
Staircase Generator



Capacitor Hysteresis Compensation

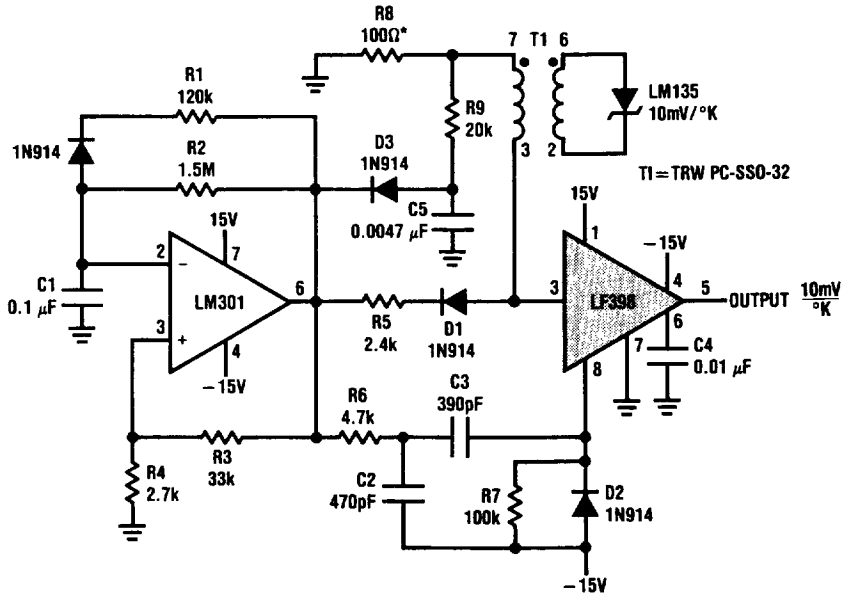


Differential Hold



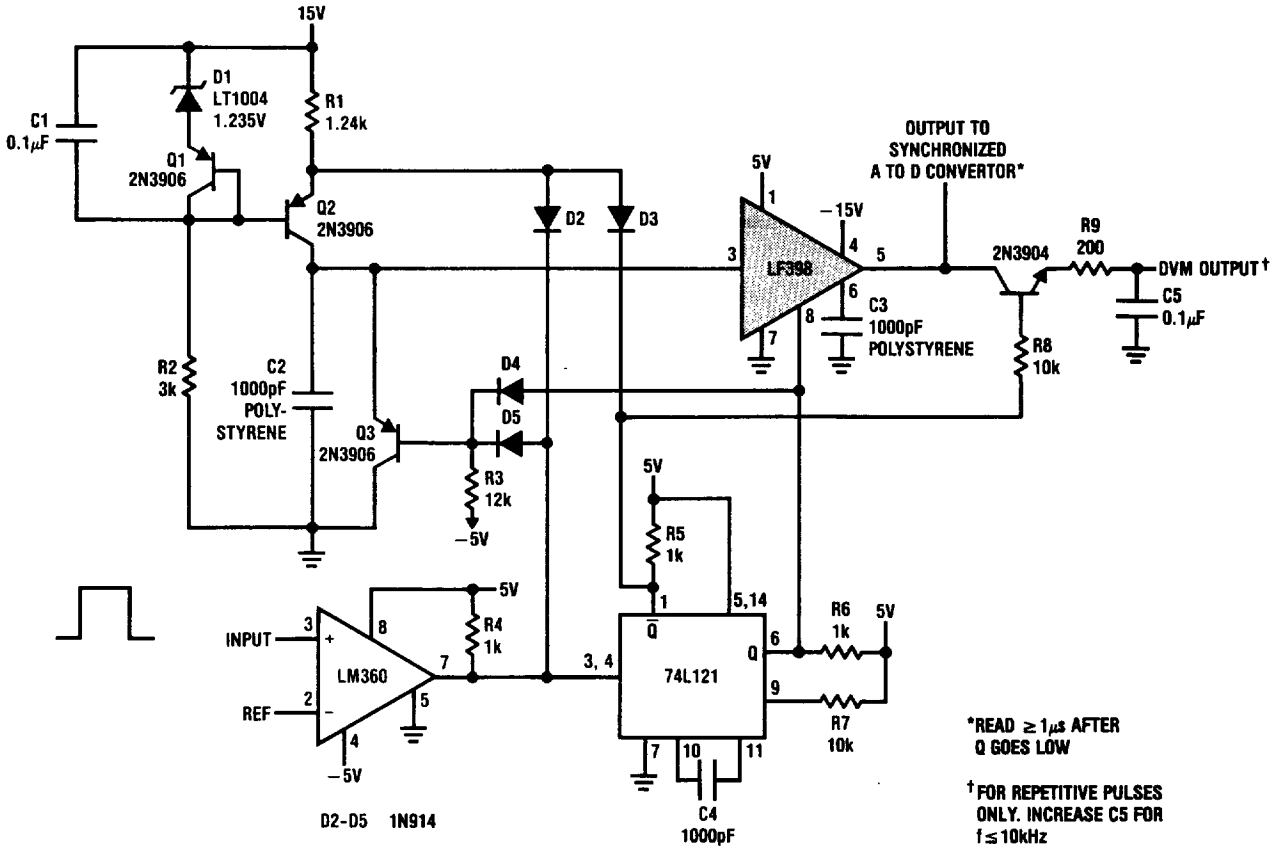
TYPICAL APPLICATIONS

Isolated Temperature Sensor



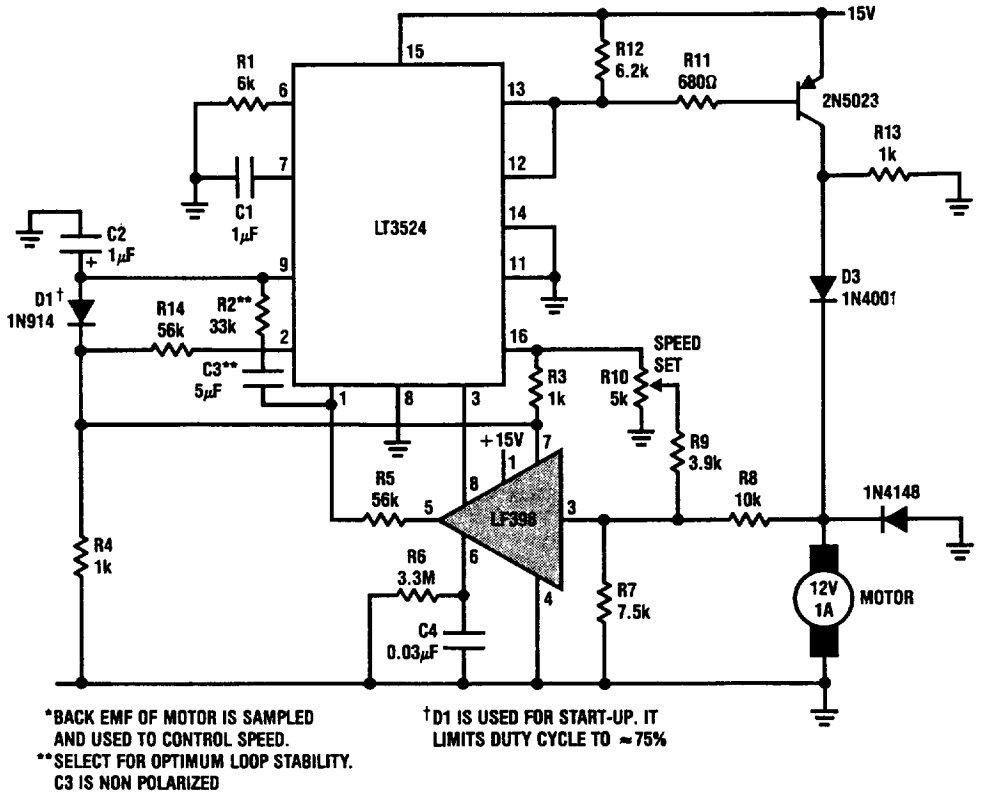
*COMPENSATES FOR TRANSFORMER RESISTANCE. SELECT FOR FLAT OUTPUT FROM LF198 WHILE IN SAMPLE MODE.

Pulse Width to Voltage Converter



TYPICAL APPLICATIONS

Motor Speed Controller Needs No Tachometer*



*BACK EMF OF MOTOR IS SAMPLED AND USED TO CONTROL SPEED.
**SELECT FOR OPTIMUM LOOP STABILITY. C3 IS NON POLARIZED

†D1 IS USED FOR START-UP. IT LIMITS DUTY CYCLE TO ≈75%

DEFINITION OF TERMS

Hold Step: The voltage step at the output of the amplifier when switching from sample mode to hold mode with a constant analog input voltage and a logic swing of 5V.

Acquisition Time: The time required to acquire, within a defined error, a new analog input voltage with an output change of 10V. Acquisition time includes output settling time and includes the time required for all internal nodes to settle so that the output is at the proper value when switched to the hold mode.

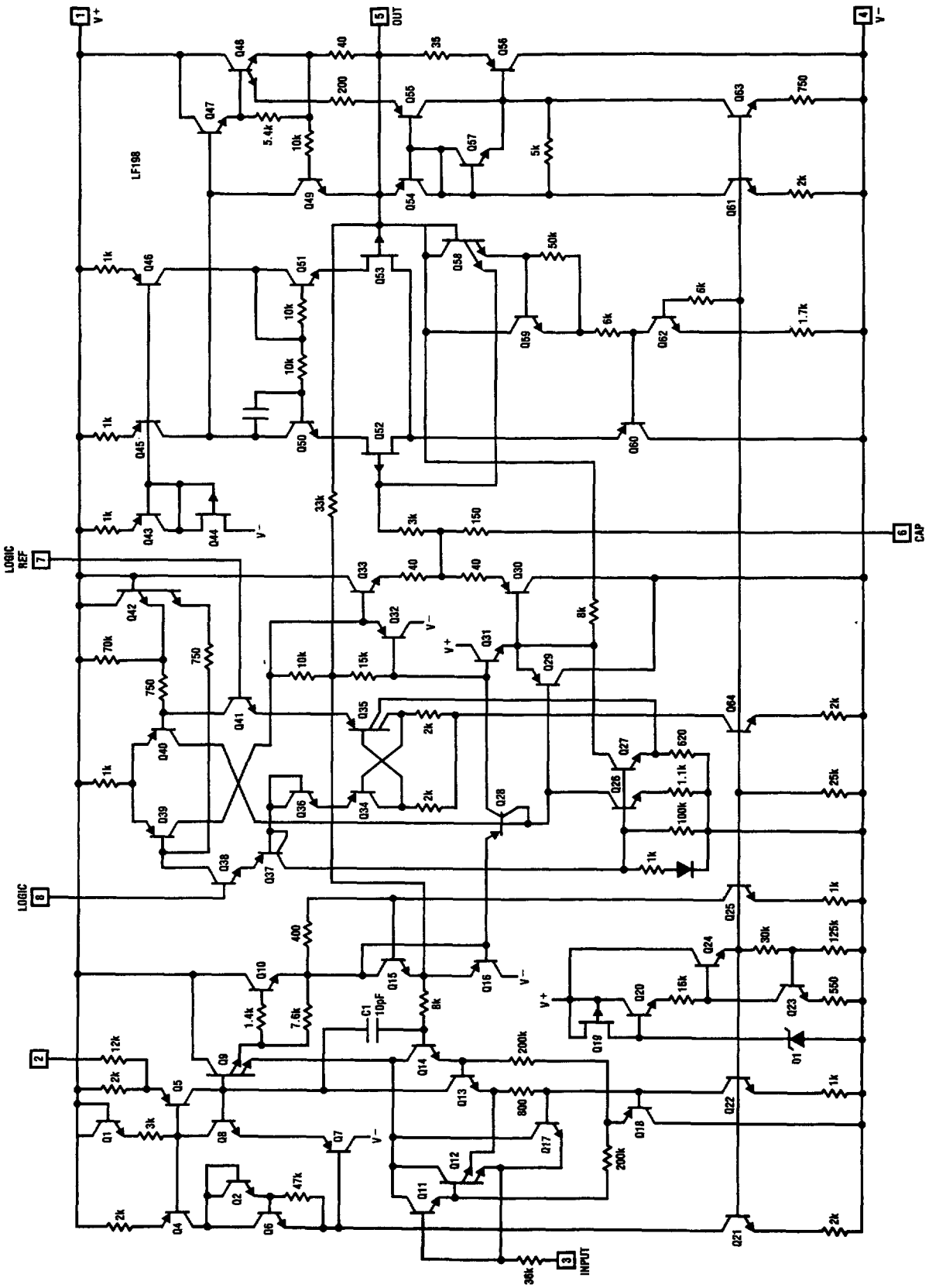
Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1mV of final value after a hold command is initiated.

Dynamic Sampling Error: The error introduced into the held output voltage due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

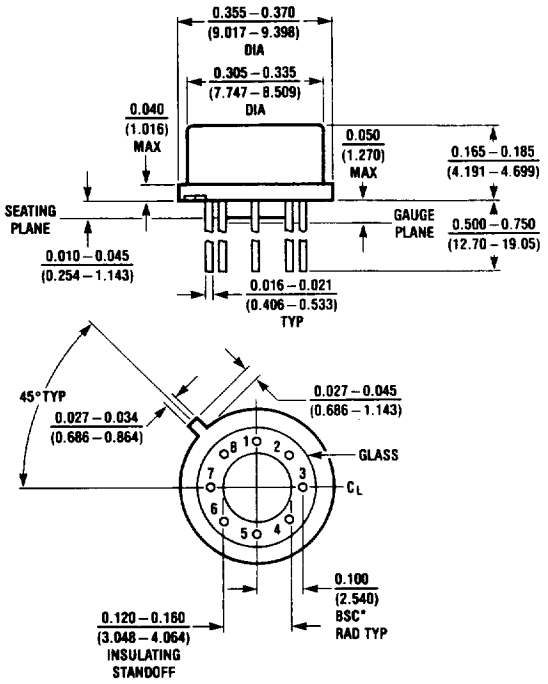
Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

SCHEMATIC DIAGRAM



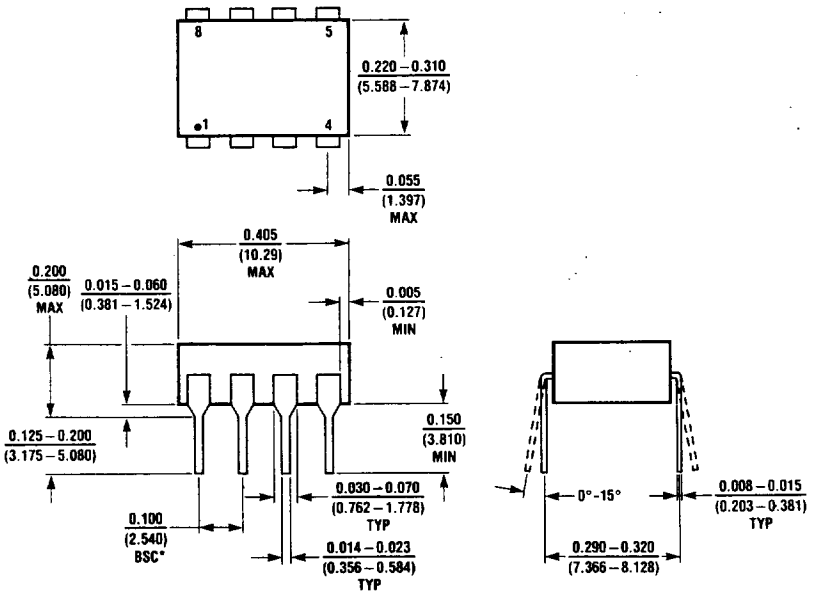
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
Metal Can



	$T_j$max	θ_{ja}	θ_{jc}
LF198/LF198A	150°C	150°C/W	45°C/W
LF398/LF398A	100°C	150°C/W	45°C/W

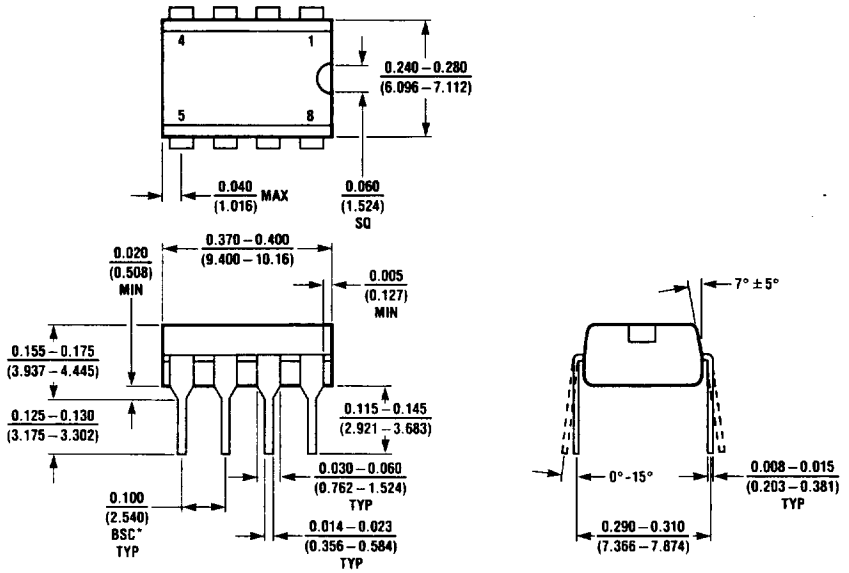
J8 Package
8 Lead Hermetic DIP



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

	$T_j$max	θ_{ja}
LF398	100°C	100°C/W

N8 Package
8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

	$T_j$max	θ_{ja}
LF398/LF398A	100°C	130°C/W