

STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **BD9882F, BD9882FV**

FUNCTION

- 1ch control with Push-Pull
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- Short circuit protection with over voltage
- Mode-selectable the operating or stand-by mode by stand-by pin
- Synchronous operating the other BD9882F or BD9882FV IC' s
- BURST mode controlled by PWM and DC input

○Absolute Maximum Ratings (Ta = 25°C)

| Parameter | Symbol | Limits | Unit |
|------------------------------|--------|-------------------------------------|------|
| Supply Voltage | Vcc | 15 | V |
| Operating Temperature Range | Topr | -40~+95 | °C |
| Storage Temperature Range | Tstg | -55~+125 | °C |
| Power Dissipation | Pd | 550*1 (BD9882F) 650*2 (BD9882FV) | mW |
| Maximum Junction Temperature | Tjmax | +125 | °C |

*1Pd derate at 5.5mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm × 70.0mm × 1.6mm)

*2Pd derate at 6.5mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm × 70.0mm × 1.6mm)

○Recommended operating condition

| Parameter | Symbol | Limits | Unit |
|---------------------------|--------|-----------|------|
| Supply voltage | Vcc | 5.0~14.0 | V |
| CT oscillation frequency | fCT | 20~150 | kHz |
| BCT oscillation frequency | fBCT | 0.10~0.50 | kHz |

Status of this document

The Japanese language version of this document shall be the official specification.

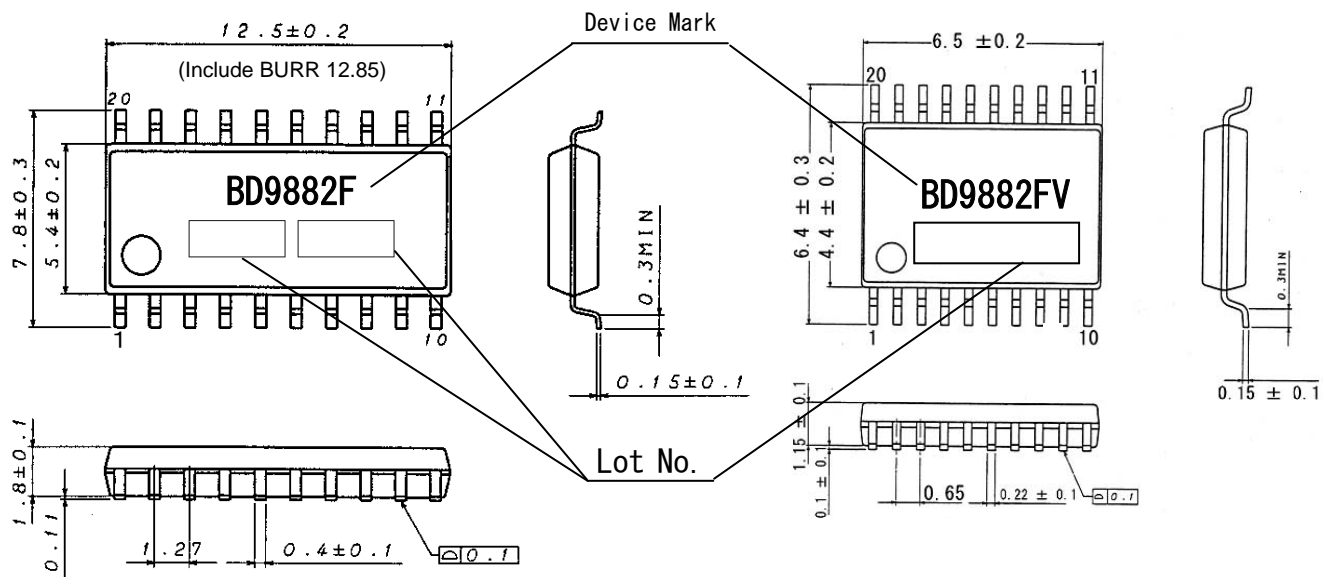
Any translation of this document shall be for reference only.

○Electric Characteristics (Ta=25°C, VCC=7V)

| Parameter | Symbol | Limits | | | Unit | Conditions |
|--------------------------------|----------------------|----------|---------|----------|------|----------------------------|
| | | MIN. | TYP. | MAX. | | |
| ((WHOLE DEVICE)) | | | | | | |
| Operating current | Icc1 | — | 8 | 16 | mA | CT=0.5V |
| Stand-by current | Icc2 | — | 2 | 10 | μA | |
| ((OVER VOLTAGE DETECT)) | | | | | | |
| FB over voltage detect voltage | Vovf | 2.20 | 2.40 | 2.60 | V | |
| ((STAND-BY CONTROL)) | | | | | | |
| Stand-by voltage H | VstH | 1.8 | — | VCC | V | System ON |
| Stand-by voltage L | VstL | -0.3 | — | 0.8 | V | System OFF |
| ((TIMER LATCH)) | | | | | | |
| Timer Latch voltage | Vcp | 1.9 | 2.0 | 2.1 | V | |
| Timer Latch current | Icp | 0.5 | 1.0 | 1.5 | μA | |
| ((OSC BLOCK)) | | | | | | |
| OSC constant current | IcT | 1.35/RT | 1.5/RT | 1.65/RT | A | |
| OSC Max voltage | VoscH | 1.8 | 2.0 | 2.2 | V | f _{CT} =60kHz |
| OSC Min voltage | VoscL | 0.3 | 0.5 | 0.7 | V | f _{CT} =60kHz |
| MAX DUTY | MAXDUTY | 44 | 46.5 | 49 | % | f _{CT} =60kHz |
| Soft start current | I _{SS} | 1.0 | 2.0 | 3.0 | μA | |
| IS COMP detect Voltage | V _{ISC} | 0.45 | 0.50 | 0.55 | V | |
| SS COMP detect voltage | V _{SS} | 2.0 | 2.2 | 2.4 | V | |
| SRT ON resistance | RSRT | — | 200 | 400 | Ω | |
| ((UVLO BLOCK)) | | | | | | |
| Operating voltage | V _{UVLOH} | 4.000 | 4.200 | 4.400 | V | |
| Shut down voltage | V _{UVLOL} | 3.800 | 4.000 | 4.200 | V | |
| ((FEED BACK BLOCK)) | | | | | | |
| IS threshold voltage | V _{IS} | 1.225 | 1.250 | 1.275 | V | |
| VS threshold voltage | V _{VS} | 1.220 | 1.250 | 1.280 | V | |
| IS source current 1 | I _{IS1} | — | — | 1.5 | μA | DUTY=2.0V |
| IS source current 2 | I _{IS2} | 13.0 | 20.0 | 27.0 | μA | DUTY=0V、IS=0.5V |
| VS source current | I _{VS} | — | — | 1.0 | μA | |
| ((Output BLOCK)) | | | | | | |
| Output voltage H | V _{OUTNH} | VCC-0.3 | VCC-0.1 | — | V | |
| Output voltage L | V _{OUTNL} | — | 0.1 | 0.3 | V | |
| Output sink resistance | R _{SINKN} | — | 8 | 16 | Ω | I _{sink} = 10mA |
| Output source resistance | R _{SOURCEN} | — | 10 | 20 | Ω | I _{source} = 10mA |
| Drive output frequency | FN | 58.5 | 60.0 | 61.5 | kHz | RT=18kΩ CT=400pF |
| ((BURST MODE)) | | | | | | |
| BOSC Max voltage | V _{BURH} | 1.94 | 2.0 | 2.06 | V | f _{BCT} =0.2kHz |
| BOSC Min Voltage | V _{BURL} | 0.4 | 0.5 | 0.6 | V | f _{BCT} =0.2kHz |
| BOSC constant current | I _{BUROSC} | 1.35/BRT | 1.5/BRT | 1.65/BRT | A | |
| BOSC frequency | FBOSC | 261 | 275 | 289 | Hz | BRT=33kΩ BCT=0.051μF |
| ((REG BLOCK)) | | | | | | |
| REG output voltage | V _{REG} | 3.038 | 3.100 | 3.162 | V | |
| REG source current | I _{REG} | 5.0 | — | — | mA | |
| ((COMP BLOCK)) | | | | | | |
| Over voltage detect | V _{COMPH} | 2.20 | 2.5 | 2.80 | V | |
| Under voltage detect | V _{COMPL} | 0.590 | 0.640 | 0.690 | V | |
| ((FAIL PIN)) | | | | | | |
| Normal output voltage | V _{PH} | 0.45 | 0.5 | 0.55 | V | |
| Protect output voltage | V _{PL} | 2.9 | 3.1 | 3.3 | V | |
| Protect cancel voltage detect | V _{FAIL} | 0.36 | 0.40 | 0.44 | V | |

(This product is not designed for normal operation with in a radio active environment.)

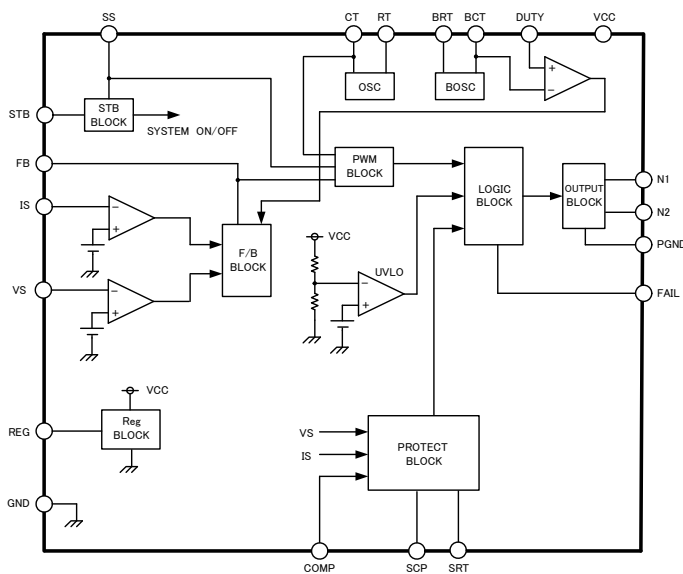
Package Dimensions



SOP20 (Unit:mm)

SSOP-B20 (Unit:mm)

Block Diagram



Pin Description

| Pin No. | Pin Name | Function |
|---------|----------|--|
| 1 | DUTY | Control PWM mode and BURST mode |
| 2 | BRT | External resistor from BRT to GND for adjusting the BURST triangle oscillator |
| 3 | BCT | External capacitor from BCT to GND for adjusting the BURST triangle oscillator |
| 4 | RT | External resistor from SRT to RT for adjusting the triangle oscillator |
| 5 | SRT | External resistor from SRT to RT for adjusting the triangle oscillator |
| 6 | CT | External capacitor from CT to GND for adjusting the triangle oscillator |
| 7 | GND | GROUND |
| 8 | FB | Error amplifier output |
| 9 | IS | Error amplifier input① |
| 10 | VS | Error amplifier input② |
| 11 | STB | Stand-by switch |
| 12 | COMP | Under, over voltage detect |
| 13 | REG | Internal regulator output |
| 14 | SS | External capacitor from SS to GND for Soft Start Control |
| 15 | SCP | External capacitor from SCP1 to GND for Timer Latch |
| 16 | N2 | FET driver |
| 17 | PGND | Ground for FET drivers |
| 18 | N1 | FET driver |
| 19 | FAIL | Protect clock output |
| 20 | Vcc | Supply voltage input |

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and the IC. Use adequate margins for steady state and transient characteristics.
2. Recommended Operating Range
The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however, the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within $\pm 0.3V$ compared with the PGND pin
6. The BD9882F and BD9882FV incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of the thermal shutdown circuit is assumed.
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
10. By STB voltage, BD9882F and BD9882FV are changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8~1.8V).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
12. This IC is a monolithic IC which (as shown is Fig-1) has P⁺ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows.
 ○ (When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
 ○ (When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

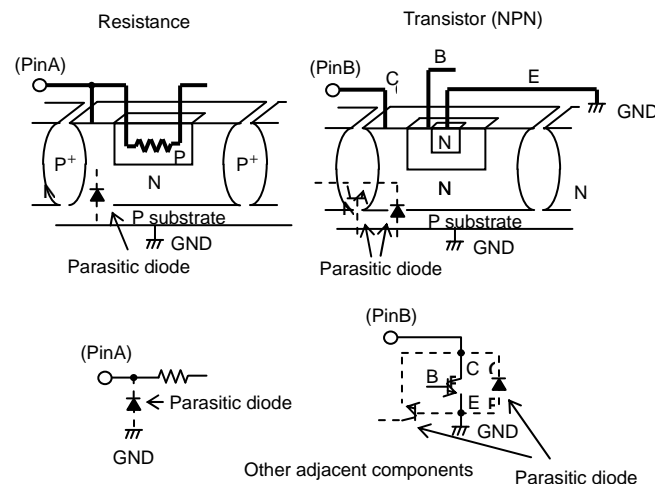


Fig-1 Simplified structure of a Bipolar IC

Notes

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