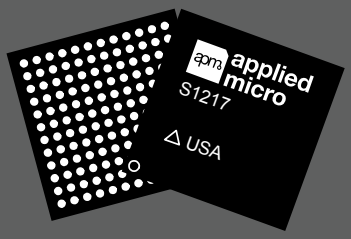
S1217

Serial OC-3/12 - to - 8 Bit Transceiver

PRODUCT BRIEF



The S1217 transceiver provides a fully integrated serialization/de-serialization device that performs all necessary parallel-to-serial and serial-to-parallel functions in conformance with SONET/SDH transmission standards. The S1217 receive section operates with a channel selectable operating rate of 155.52 or 622.08 Mbps. Included is an integrated CDR as well as SONET/SDH framer with alarms. The S1217 can be configured to operate with and without the use of a micro controller MII (Media Independent Interface) and Non-MII modes respectively.

The figure below, System Block Diagram, shows a typical network application.

Features

- Supports both OC-3 and OC-12 data rates.
- 8-bit LVCMOS parallel data path
- SONET/SDH framing capability with frame pulse output and OOF/LOF alarms
- Transmit FIFO, maximizing transmit timing
- Lock detect outputs and signal detect inputs with selectable CDR reference frequencies of 19.44, 77.76 or 155.52 MHz
- Embedded diagnostics including BIST and multiple loopback modes: Diagnostic / Line / Parallel / Serial Clock loop timing
- CMOS 0.13 micron technology
- 1.2V & 3.3V / 2.5V power supply requirements with no sequencing required. I/Os directly compatible with: 2.5V/3.3V LVDS, or 3.3V LVPECL using either an AC or DC coupled
- interface.
- Minimal external components required;
- featuring internal loop filter components, internally biased outputs, internal common mode bias for AC inputs and internal bias for LVPECL drivers.
- Complies with Bellcore and ITU-T
- specifications for jitter tolerance, jitter
- transfer, and jitter generation
- Typical 320 mW power in LVDS mode
- 81 PBGA package with green/RoHS compliant lead free option

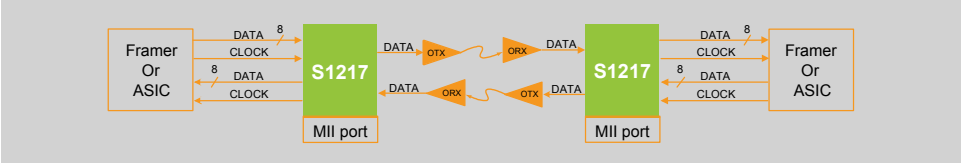
Applications

- SONET/SDH modules & test equipment
- ATM over SONET/SDH
- Section repeaters & add drop multiplexers
- Broad-band cross-connects
- Fiber optic terminators & test equipment

Overview

The S1217 transceiver implements SONET/SDH serialization/ deserialization, and transmission functions. This device can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, framing/byte alignment, and system timing. The system timing circuitry consists of management of the data stream and clock distribution throughout the front end.

S1217 System Block Diagram



For technical support inquiries, submit your product related questions to support@appliedmicro.com.

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