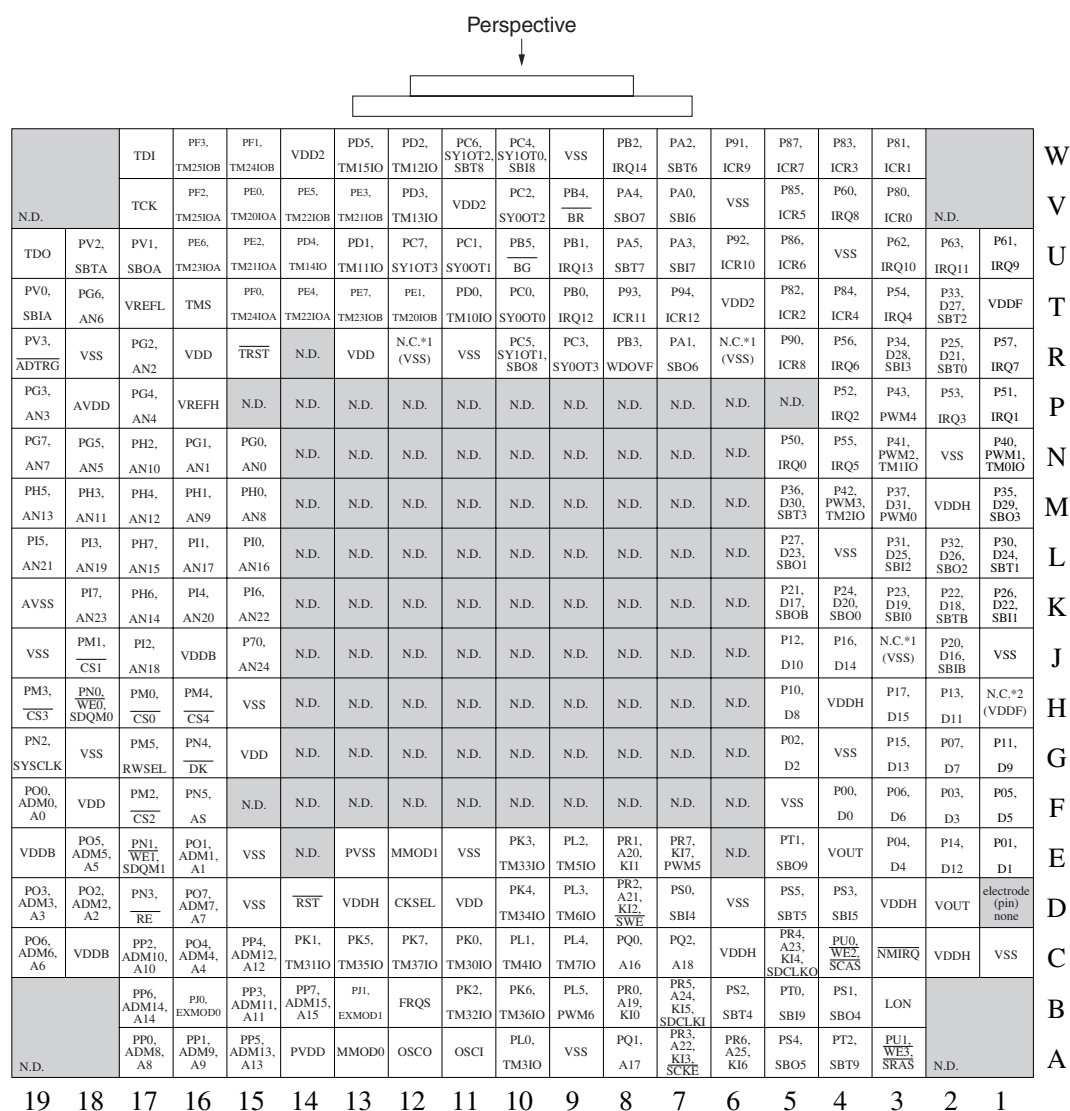


# **MN103S33N**

|   |              |  |              |
|---|--------------|--|--------------|
| <b>Type</b>                               |              | MN103S33N (under development)  |              |
| <b>Command ROM (x64-bit)</b>              |              | 512 K-byte   |              |
| <b>Data RAM (x32-bit)</b>                 |              | 24 K-byte  |              |
| <b>Package</b>                            |              | MLGA344-C-1313   |              |
| <b>Minimum Instruction Execution Time</b> |              | 25 ns (at 2.3 V to 2.7 V, 40 MHz)  |              |
| <b>Interrupts</b>                         |              | • RESET • IRQ × 15 • NMI • Key input • Timer × 44 • Input capture × 16 • PWM × 8 • SIF × 25<br>• DMA × 12 • WDT • A/D • System error   |              |
| <b>Timer Counter</b>                      |              | 8-bit timer × 12<br>Reload-down count<br>Cascade connection possible (usable as a 16-, 32-bit timer)<br><br>8-bit timer with PWM × 8<br>Reload-down count<br>Cascade connection possible (usable as a 16-, 32-bit timer)<br>PWM generating function<br><br>16-bit timer × 6<br>Up-down count<br>Input capture function<br>PWM generating function<br>Compare/capture register 2-ch.<br><br>16-bit timer × 6<br>Reload-down count<br><br>Watchdog timer × 1 |              |
| <b>DMA Controller</b>                     |              | Number of channels: 4<br>Unit of transfer: 8/16/32 bits<br>Max. Transfer cycles: 65535<br>Staring factor: external interrupt, timer factor, PNM factor, serial transmission/reception factor, A/D conversion finish, software factor<br>Transfer method: 2-bus cycle transfer<br>Adressing modes: fixed, increment, decrement<br>Transfer modes: word transfer, burst transfer, intermittent transfer  |              |
| <b>Serial Interface</b>                   |              | Serial 0, 1, 3 to 8, A, B: start-stop synchronization/synchronization/I <sup>2</sup> C commonly used, 10 lines<br>Serial 2, 9: 2 lines for start-stop synchronization only, serial 2: 10 bytes containing receive FIFO   |              |
| <b>I/O Pins</b>                           | <b>I/O</b>   | 170  | • Common use |
|   | <b>Input</b> | 25   | • Common use |
| <b>A/D Inputs</b>                         |              | 10-bit × 25-ch.  |              |
| <b>PWM</b>                                |              | 12-, 14-bit resolution × 5-ch.<br>output waveform value load control function provided 16-bit resolution × 2-ch.   |              |
| <b>ICR</b>                                |              | 28-bit × 13-ch. + 16-bit × 6-ch. (common with timer)   |              |
| <b>OCR</b>                                |              | 16-bit × 4-ch. (common with timer)   |              |
| <b>Timer Synchronous Output</b>           |              | 4-bit (synchronous output) × 2-ch.   |              |

## T.B.D.

## Pin Assignment



MLGA344-C-1313

\* N.D. has an electrode (pin) but N.C. is not guaranteed.

\* Each of VDDH, VDD, VDDDB, VDDF, VDD2, and VSS has multiple electrodes (pins). Connect the same electrode names to the same power supply.

\*1: Connect the J3, R6, and R12 pins to the VSS for the MN103SF33N.

\*2: Connect the H1 and T1 pins to the VDDF power for the MN103SF33N.

## Support Tool

|                                     |                                    |                                   |
|-------------------------------------|------------------------------------|-----------------------------------|
| ■ <b>In-circuit Emulator</b>        | PX-ICE103S33 (under development)   | Not applicable to MLGA344-C-1313. |
|                                     |                                    |                                   |
| ■ <b>Flash Memory Built-in Type</b> | Type                               | MN103SF33N (under development)    |
|                                     | Command ROM (× 64-bit)             | 512 K-byte                        |
|                                     | Data RAM (× 32-bit)                | 24 K-byte                         |
|                                     | Minimum instruction execution time | 25 ns (at 2.3 V to 2.7 V, 40 MHz) |
|                                     | Package                            | MLGA344-C-1313                    |

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