



STS5N15F4

N-channel 150 V, 0.057Ω, 5 A, SO-8
STripFET™ DeepGATE™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STS5N15F4	150 V	< 0.063 Ω	5 A

- N-channel enhancement mode
- 100% avalanched rated
- Low gate charge
- Very low on-resistance

Application

- Switching applications

Description

This STripFET™ DeepGATE™ Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance, with a new gate structure, providing superior switching performances.

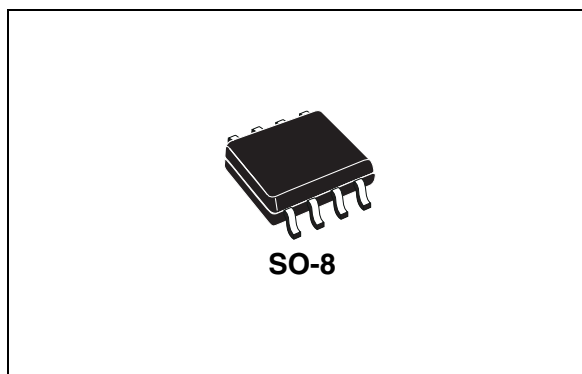


Figure 1. Internal schematic diagram

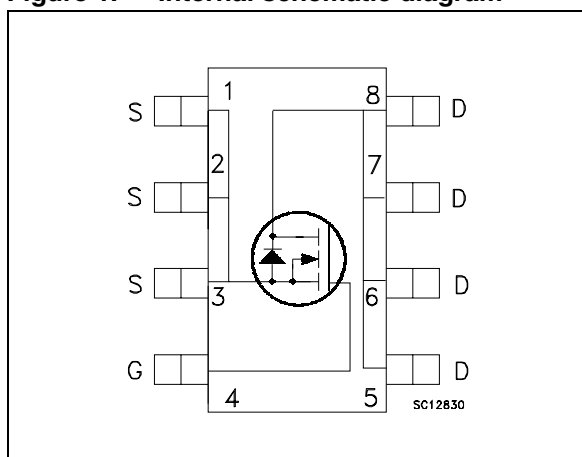


Table 1. Device summary

Order code	Marking	Package	Packaging
STS5N15F4	5U15-	SO-8	Tape and reel

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	150	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	2.5	W
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature		

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, $t < 10\text{ sec}$

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 140\text{ V}$)	125	mJ

2 Electrical characteristics

($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	150			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 150\text{ V}$, $V_{DS} = 150\text{ V}$, @ $125\text{ }^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$		0.057	0.063	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	2710	-	pF
C_{oss}	Output capacitance			180		pF
C_{rss}	Reverse transfer capacitance			69.5		pF
Q_g	Total gate charge	$V_{DD} = 75\text{ V}$, $I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}$ Figure 14 on page 7	-	48	-	nC
Q_{gs}	Gate-source charge			10.8		nC
Q_{gd}	Gate-drain charge			13.7		nC
R_g	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	-	1.9	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=75\text{ V}$, $I_D=3\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ <i>Figure 13 on page 7</i>	-	13.5	-	ns
t_r	Rise time			5.1		ns
$t_{d(off)}$	Turn-off delay time			39.7		ns
t_f	Fall time			11.4		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=6\text{ A}$, $V_{GS}=0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD}=6\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$, $V_R=120\text{ V}$, $T_J=150\text{ }^\circ\text{C}$ <i>Figure 15 on page 7</i>	-	85.2		ns
Q_{rr}	Reverse recovery charge			277.6		nC
I_{RRM}	Reverse recovery current			8.2		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

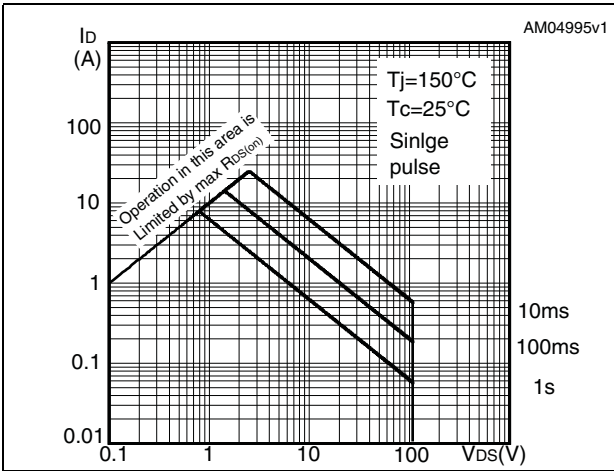


Figure 3. Thermal impedance

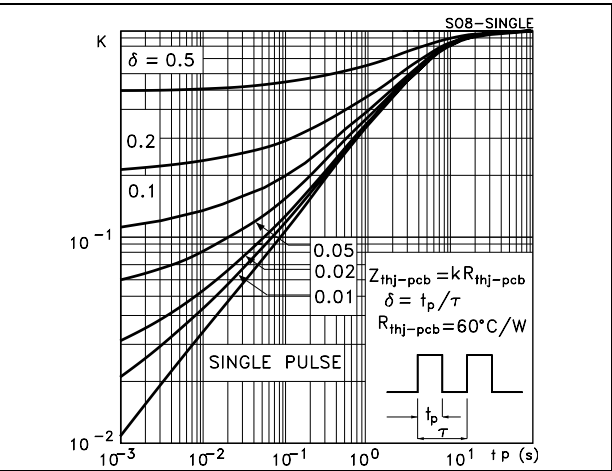


Figure 4. Output characteristics

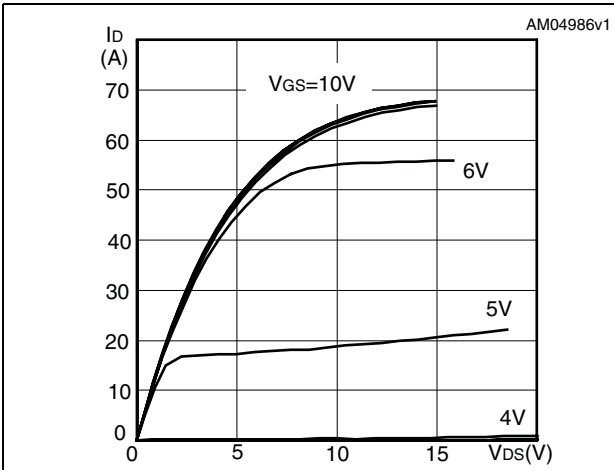


Figure 5. Transfer characteristics

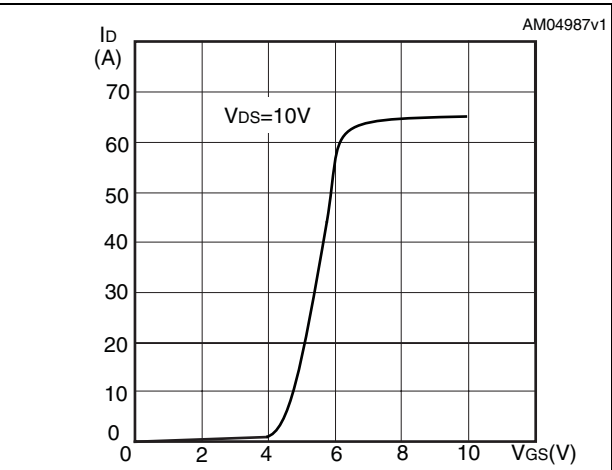


Figure 6. Normalized B_{VDS} vs temperature

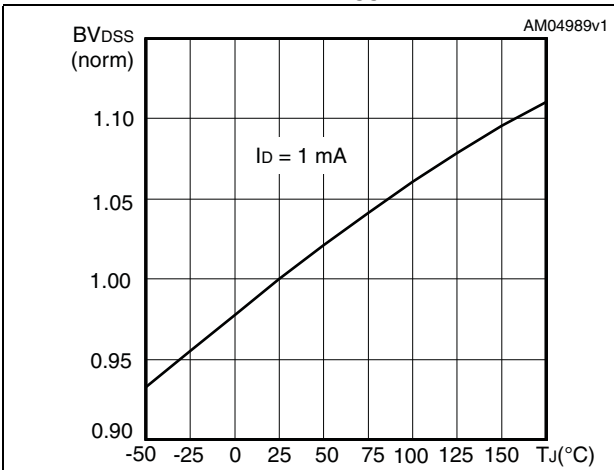


Figure 7. Static drain-source on resistance

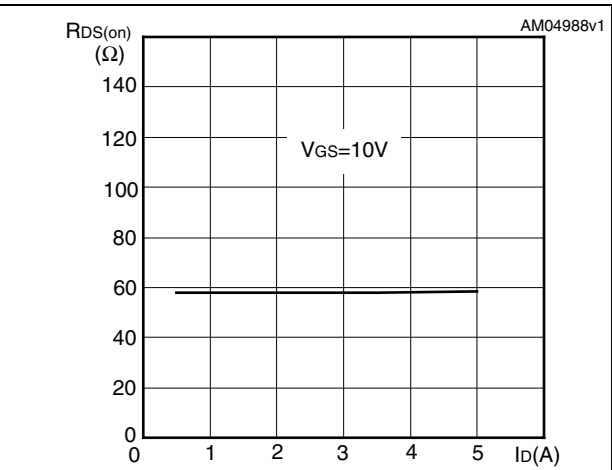


Figure 8. Gate charge vs gate-source voltage

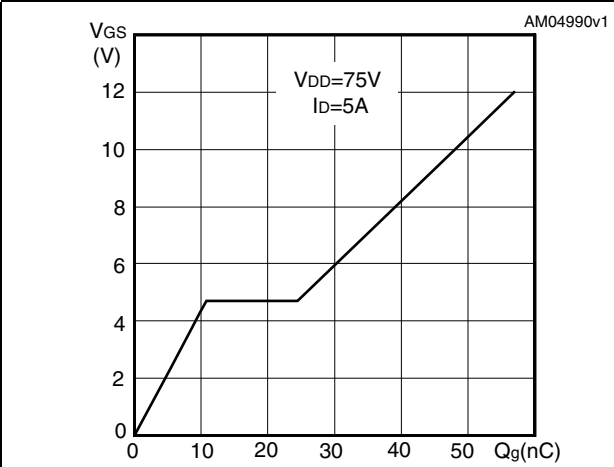


Figure 9. Capacitance variations

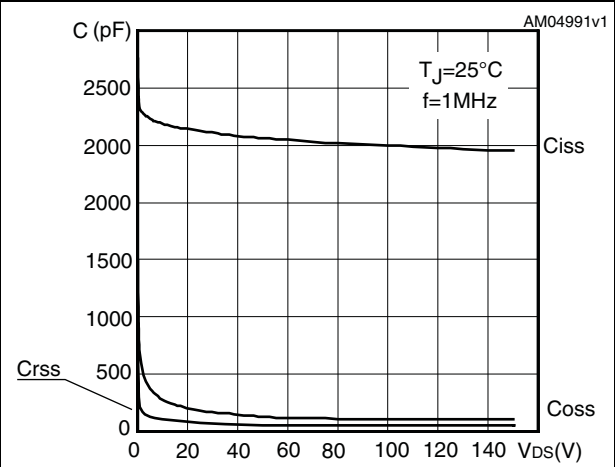


Figure 10. Normalized gate threshold voltage vs temperature

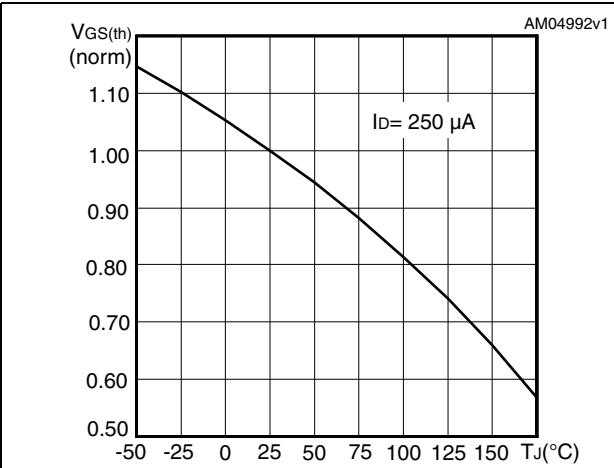


Figure 11. Normalized on resistance vs temperature

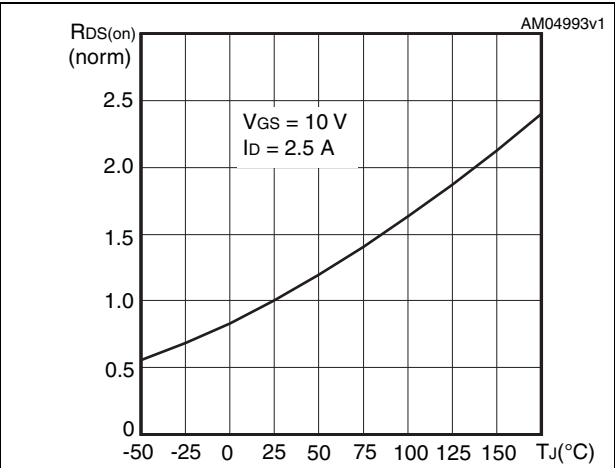
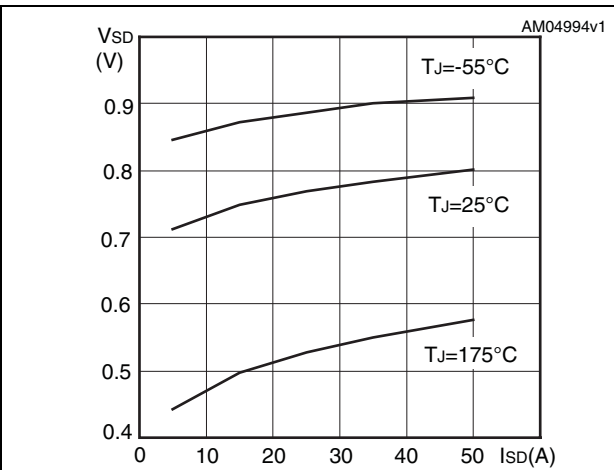


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

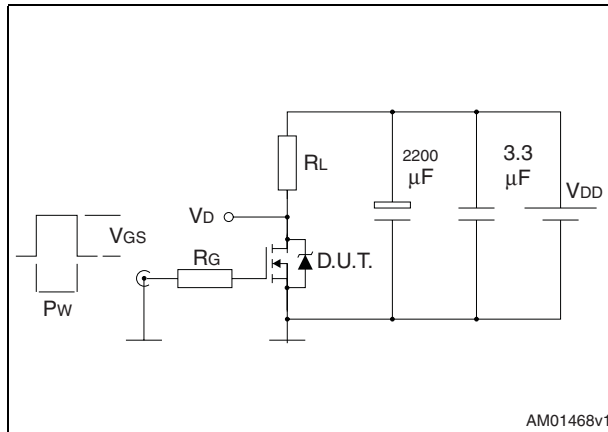


Figure 14. Gate charge test circuit

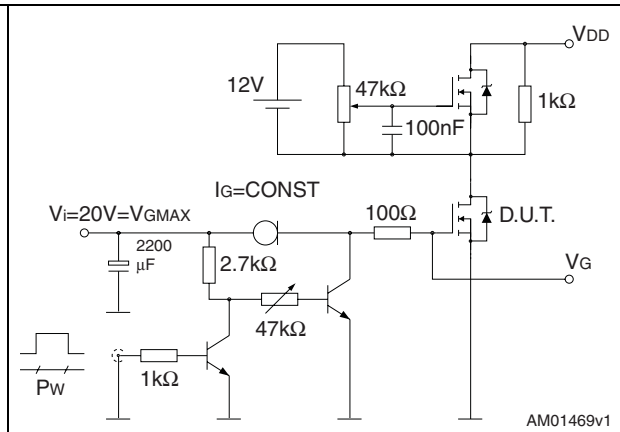


Figure 15. Test circuit for inductive load switching and diode recovery times

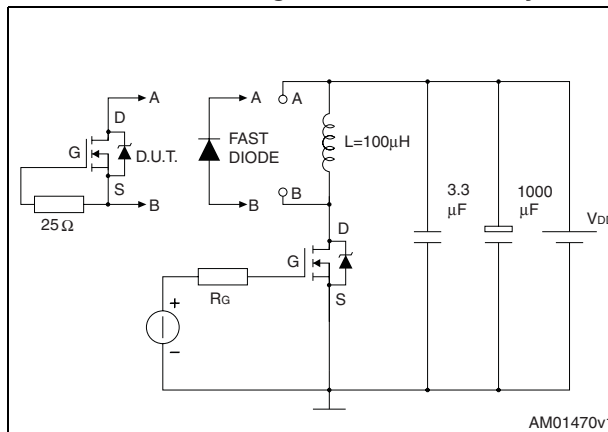


Figure 16. Unclamped inductive load test circuit

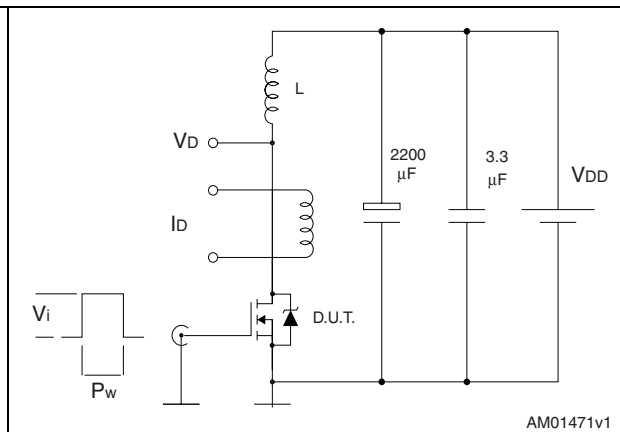


Figure 17. Unclamped inductive waveform

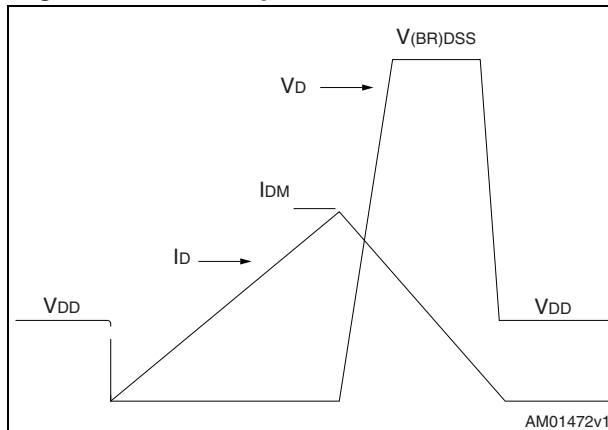
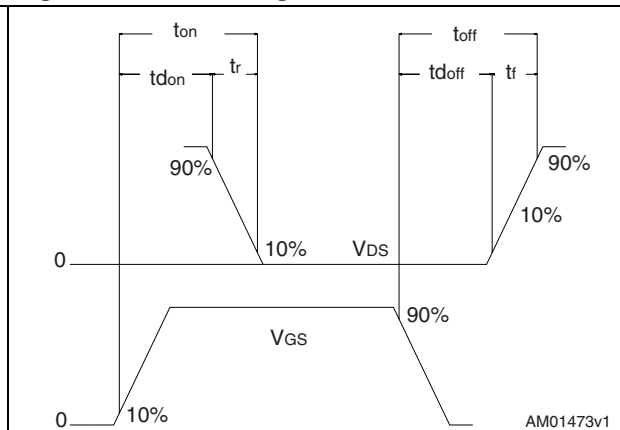


Figure 18. Switching time waveform

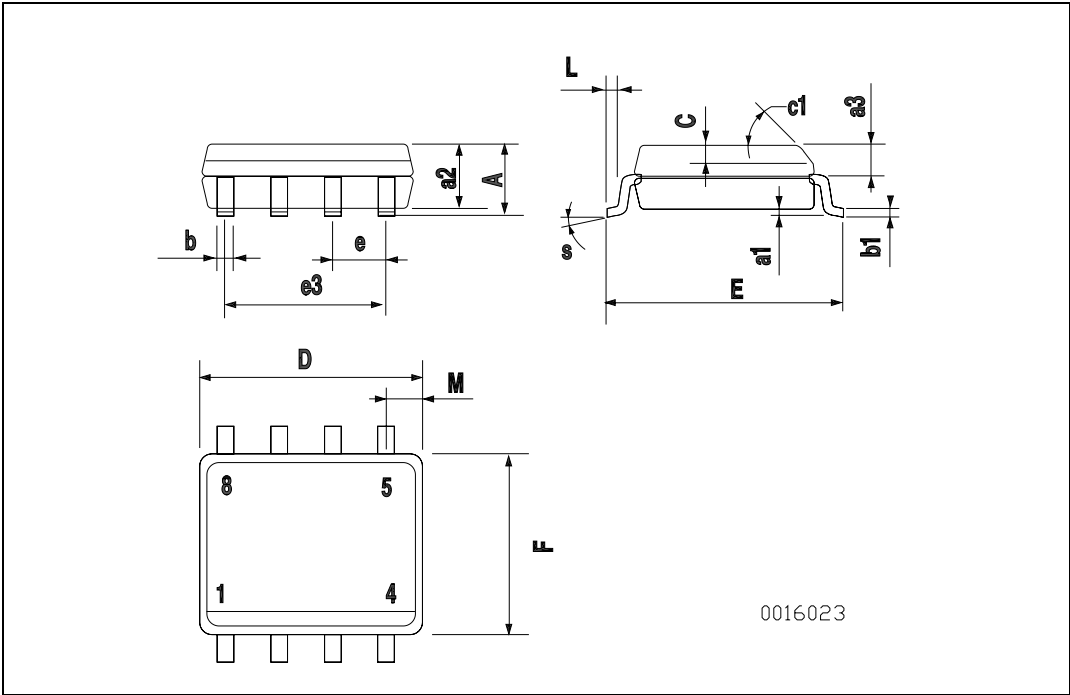


4 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
23-Jul-2009	1	First release
03-Aug-2009	2	Updated figures 6 , 7 , 10 and 11

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