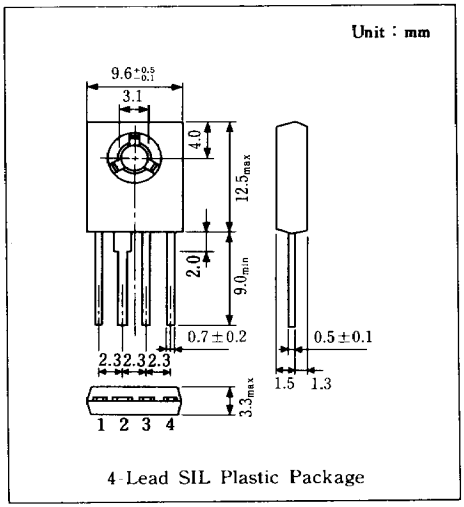
AN7800R/AN78M00R Series

Positive Output Voltage Regulators with Reset Pin (1A/500mA Type)

■ Outline

The AN7800R and the AN78M00R series are fixed positive output voltage regulators with reset pin. Stabilized fixed output voltage is obtained from unstable DC input voltage without using any external components. Three types of output voltage, 5V, 9V and 12V, are available for the AN7800R series, and four types, 5V, 8V, 9V and 12V, are available for the AN78M00R series. They can be used in power circuits with current capacity 1A/500mA. ON/OFF of output voltage can be controlled by the reset pin.

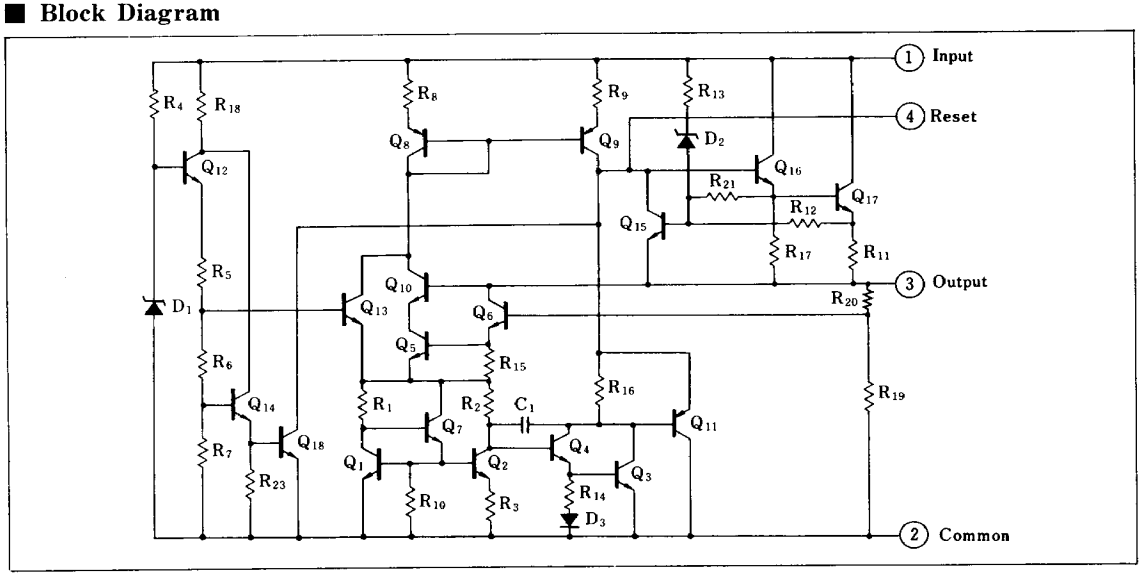


4-Lead SIL Plastic Package

■ Features

- No external components
- Maximum output current : 1A (AN78××R), 500mA (AN78M××R)
- Output voltage : 5V, 9V, 12V(AN7800R) : 5V, 8V, 9V, 12V (AN78M08R)
- Short-circuit current limiting built in
- Thermal overload protection built in
- Output transistor safe area compensation
- ON/OFF of output voltage can be controlled by reset pin.

■ Block Diagram



Panasonic

■ Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Rating	Unit
Input Voltage	V_I	35	V
Power Dissipation	P_D	10*1	W
Operating Ambient Temperature	T_{opr}	−20～+80	℃
Storage Temperature	T_{stg}	−55～+150	℃

*1 Follow the derating curve. When T_j exceeds 150℃, the internal circuit cuts off the output.

■ Electrical Characteristics (Ta=25℃)

AN7800R Series

● AN7805R (1A, 5V Type)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Output Voltage	V_O	1	T_j=25℃	4.8	5	5.2	V
Output Voltage Tolerance	V_O	1	V_I=8~20V, I_O=5mA~1A, T_j=0~125℃, P_D≦15W	4.75		5.25	V
Line Regulation	REG_{IN}	1	V_I=7.5～25V, T_j=25℃		3	100	mV
			V_I=8～12V, T_j=25℃		1	50	mV
Load Regulation	REG_L	1	I_O=5mA～1.5A, T_j=25℃		15	100	mV
			I_O=250～750mA, T_j=25℃		5	50	mV
Bias Current	I_{Bias}	2	T_j=25℃		3.9	8	mA
Input Bias Current Fluctuation	$\Delta I_{Bias(I)}$	2	V_I=7.5～25V, T_j=25℃			1.3	mA
Load Bias Current Fluctuation	$\Delta I_{Bias(L)}$	2	V_O=5mA～1A, T_j=25℃			0.5	mA
Output Noise Voltage	V_{no}	1	f=10Hz～100kHz		40		μV
Ripple Rejection Ratio	RR	3	V_I=8～18V, I_O=100mA, f=120Hz	62			dB
Minimum Input/Output Voltage Difference	$V_{DIF(min.)}$	4	I_O=1A, T_j=25℃		2		V
Output Impedance	Z_O	5	f=1kHz		17		mΩ
Output Short Circuit Current	$I_{O(Short)}$	1	V_I=35V, T_j=25℃		300		mA
Peak Output Current	$I_{O(Peak)}$	1	T_j=25℃		2		A
Output Voltage Temperature Coefficient	$\Delta V_O/T_a$	1	I_O=5mA, T_j=0～125℃		−0.3		mV/℃
Output Voltage at Reset	$V_{O(Reset)}$	6	T_j=25℃, $I_{L(Reset)}$=1mA			1	V
Reset Input Current	$I_{L(Reset)}$	6	T_j=25℃			1	mA

Note 1 The specified condition T_j=25℃ means that the test should be carried out with the test time so short (within 10ms) that the drift in characteristic value due to the rise in chip junction temperature can be ignored.

Note 2 When not specified, V_I=10V, I_O=500mA, C_I=0.33μF, C_O=0.1μF and T_j=0～125℃

■ Electrical Characteristics (Ta=25℃)

● AN7809R (1A, 9V Type)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Output Voltage	V_O	1	T_j=25℃	8.65	9	9.35	V
Output Voltage Tolerance	V_O	1	V_I=12~24V, I_O=5mA~1A, T_j=0~125℃, P_D≦15W	8.55		9.45	V
Line Regulation	REG_{IN}	1	V_I=11.5~26V, T_j=25℃		7	180	mV
			V_I=12~18V, T_j=25℃		2	90	mV
Load Regulation	REG_L	1	I_O=5mA~1.5A, T_j=25℃		12	180	mV
			I_O=250~750mA, T_j=25℃		4	90	mV
Bias Current	I_{Bias}	2	T_j=25℃		3.9	8	mA
Input Bias Current Fluctuation	$\Delta I_{Bias(IN)}$	2	V_I=11.5~26V, T_j=25℃			1	mA
Load Bias Current Fluctuation	$\Delta I_{Bias(L)}$	2	I_O=5mA~1A, T_j=25℃			0.5	mA
Output Noise Voltage	V_{no}	1	f=10Hz~100kHz		57		μV
Ripple Rejection Ratio	RR	3	V_I=12~22V, I_O=100mA, f=120Hz	56			dB
Minimum Input/Output Voltage Difference	$V_{DIF(min.)}$	4	I_O=1A, T_j=25℃		2		V
Output Impedance	Z_O	5	f=1kHz		16		mΩ
Output Short Circuit Current	$I_{O(Short)}$	1	V_I=26V, T_j=25℃		700		mA
Peak Output Current	$I_{O(Peak)}$	1	T_j=25℃		2		A
Output Voltage Temperature Coefficient	$\Delta V_O/T_a$	1	I_O=5mA, T_j=0~125℃		−0.5		mV/℃
Output Voltage at Reset	$V_{O(Reset)}$	6	T_j=25℃, $I_{I(Reset)}$=1mA			1	V
Reset Input Current	$I_{I(Reset)}$	6	T_j=25℃			1	mA

Note 1) The specified condition T_j=25℃ means that the test should be carried out with the test time so short (within 10ms) that the drift in characteristic value due to the rise in chip junction temperature can be ignored.
Note 2) When not specified, V_I=15V, I_O=500mA, C_I=0.33μF, C_O=0.1μF and T_j=0~125℃

● AN7812R (1A, 12V Type)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Output Voltage	V_O	1	T_j=25℃	11.5	12	12.5	V
Output Voltage Tolerance	V_O	1	V_I=15~27V, I_O=5mA~1A, T_j=0~125℃, P_D≦15W	11.4		12.6	V
Line Regulation	REG_{IN}	1	V_I=14.5~30V, T_j=25℃		10	240	mV
			V_I=16~22V, T_j=25℃		3	120	mV
Load Regulation	REG_L	1	I_O=5mA~1.5A, T_j=25℃		12	240	mV
			I_O=250~750mA, T_j=25℃		4	120	mV
Bias Current	I_{Bias}	2	T_j=25℃		4	8	mA
Input Bias Current Fluctuation	$\Delta I_{Bias(IN)}$	2	V_I=14.5~30V, T_j=25℃			1	mA
Load Bias Current Fluctuation	$\Delta I_{Bias(L)}$	2	V_O=5mA~1A, T_j=25℃			0.5	mA
Output Noise Voltage	V_{no}	1	f=10Hz~100kHz		75		μV
Ripple Rejection Ratio	RR	3	V_I=15~25V, I_O=100mA, f=120Hz	55			dB
Minimum Input/Output Voltage Difference	$V_{DIF(min.)}$	4	I_O=1A, T_j=25℃		2		V
Output Impedance	Z_O	5	f=1kHz		18		mΩ
Output Short Circuit Current	$I_{O(Short)}$	1	V_I=35V, T_j=25℃		700		mA
Peak Output Current	$I_{O(Peak)}$	1	T_j=25℃		2		A
Output Voltage Temperature Coefficient	$\Delta V_O/T_a$	1	I_O=5mA, T_j=0~125℃		−0.8		mV/℃
Output Voltage at Reset	$V_{O(Reset)}$	6	T_j=25℃, $I_{I(Reset)}$=1mA			1	V
Reset Input Current	$I_{I(Reset)}$	6	T_j=25℃			1	mA

Note 1) The specified condition T_j=25℃ means that the test should be carried out with the test time so short (within 10ms) that the drift in characteristic value due to the rise in chip junction temperature can be ignored.
Note 2) When not specified, V_I=19V, I_O=500mA, C_I=0.33μF, C_O=0.1μF and T_j=0~125℃

■ Electrical Characteristics (Ta = 25℃)

AN78M00R Series

● AN78M05R (500mA, 5V Type)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Output Voltage	V_O	1	T_j = 25℃	4.8	5	5.2	V
Output Voltage Tolerance	V_O	1	V_I = 7.5~20V, I_O = 5~350mA, T_j = 0~125℃, P_D ≦ 15W	4.75		5.25	V
Line Regulation	REG_{IN}	1	V_I = 7.5~25V, T_j = 25℃		3	100	mV
			V_I = 8~25V, T_j = 25℃		1	50	mV
Load Regulation	REG_L	1	I_O = 5~500mA, T_j = 25℃		20	100	mV
			I_O = 5~200mA, T_j = 25℃		10	50	mV
Bias Current	I_{Bias}	2	T_j = 25℃		4.0	6	mA
Input Bias Current Fluctuation	$\Delta I_{Bias(IN)}$	2	V_I = 8~25V, T_j = 25℃			0.8	mA
Load Bias Current Fluctuation	$\Delta I_{Bias(L)}$	2	V_O = 5~350mA, T_j = 25℃			0.5	mA
Output Noise Voltage	V_{no}	1	f = 10Hz~100kHz		40		μV
Ripple Rejection Ratio	RR	3	V_I = 8~18V, I_O = 100mA, f = 120Hz	62			dB
Minimum Input Output Voltage Difference	$V_{DIF(min.)}$	4	I_O = 500mA, T_j = 25℃		2		V
Output Short Circuit Current	$I_{O(Short)}$	1	V_I = 35V, T_j = 25℃		300		mA
Peak Output Current	$I_{O(Peak)}$	1	T_j = 25℃		700		mA
Output Voltage Temperature Coefficient	$\Delta V_O/T_a$	1	I_O = 5mA, T_j = 0~125℃		−0.5		mV/℃
Output Voltage at Reset	$V_{O(Reset)}$	6	T_j = 25℃, $I_{O(Reset)}$ = 1mA			1	V
Reset Input Current	$I_{I(Reset)}$	6	T_j = 25℃			1	mA

Note 1 The specified condition T_j = 25℃ means that the test should be carried out with the test time so short (within 10ms) that the drift in characteristic value due to the rise in chip junction temperature can be ignored.
Note 2 When not specified, V_I = 10V, I_O = 350mA, C_I = 0.33μF, C_O = 0.1μF and T_j = 0~125℃

● AN78M08R (500mA, 8V Type)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Output Voltage	V_O	1	T_j = 25℃	7.7	8	8.3	V
Output Voltage Tolerance	V_O	1	V_I = 10.5~23V, I_O = 5~350mA, T_j = 0~125℃, P_D ≦ 15W	7.6		8.4	V
Line Regulation	REG_{IN}	1	V_I = 10.5~25V, T_j = 25℃		6	100	mV
			V_I = 11~25V, T_j = 25℃		2	50	mV
Load Regulation	REG_L	1	I_O = 5~500mA, T_j = 25℃		25	160	mV
			I_O = 5~200mA, T_j = 25℃		10	80	mV
Bias Current	I_{Bias}	2	T_j = 25℃		4.1	6	mA
Input Bias Current Fluctuation	$\Delta I_{Bias(IN)}$	2	V_I = 10.5~25V, T_j = 25℃			0.8	mA
Load Bias Current Fluctuation	$\Delta I_{Bias(L)}$	2	V_O = 5~350mA, T_j = 25℃			0.5	mA
Output Noise Voltage	V_{no}	1	f = 10Hz~100kHz		52		μV
Ripple Rejection Ratio	RR	3	V_I = 11.5~21.5V, I_O = 100mA, f = 120Hz	56			dB
Minimum Input Output Voltage Difference	$V_{DIF(min.)}$	4	I_O = 500mA, T_j = 25℃		2		V
Output Short Circuit Current	$I_{O(Short)}$	1	V_I = 35V, T_j = 25℃		300		mA
Peak Output Current	$I_{O(Peak)}$	1	T_j = 25℃		0.7		A
Output Voltage Temperature Coefficient	$\Delta V_O/T_a$	1	I_O = 5mA, T_j = 0~125℃		−0.5		mV/℃
Output Voltage at Reset	$V_{O(Reset)}$	6	T_j = 25℃, $I_{O(Reset)}$ = 1mA			1	V
Reset Input Current	$I_{I(Reset)}$	6	T_j = 25℃			1	mA

Note 1 The specified condition T_j = 25℃ means that the test should be carried out with the test time so short (within 10ms) that the drift in characteristic value due to the rise in chip junction temperature can be ignored.
Note 2 When not specified, V_I = 14V, I_O = 350mA, C_I = 0.33μF, C_O = 0.1μF and T_j = 0~125℃

■ Electrical Characteristics (Ta=25℃)

● AN78M09R (500mA, 9V Type)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Output Voltage	V_O	1	T_j=25℃	8.65	9	9.35	V
Output Voltage Tolerance	V_O	1	V_I=11.5~24V, I_O=5~350mA, T_j=0~125℃, P_D≦15W	8.55		9.45	V
Line Regulation	REG_{IN}	1	V_I=11.5~25V, T_j=25℃		7	100	mV
			V_I=12~25V, T_j=25℃		2	50	mV
Load Regulation	REG_L	1	I_O=5~500mA, T_j=25℃		25	180	mV
			I_O=5~200mA, T_j=25℃		10	90	mV
Bias Current	I_{Bias}	2	T_j=25℃		4.1	6.0	mA
Input Bias Current Fluctuation	$\Delta I_{Bias(IN)}$	2	V_I=12~25V, T_j=25℃			0.8	mA
Load Bias Current Fluctuation	$\Delta I_{Bias(L)}$	2	V_O=5~350mA, T_j=25℃			0.5	mA
Output Noise Voltage	V_{no}	1	f=10Hz~100kHz		60		μV
Ripple Rejection Ratio	RR	3	V_I=12~22V, I_O=100mA, f=120Hz	56			dB
Minimum Input/Output Voltage Difference	$V_{DIF(min.)}$	4	I_O=500mA, T_j=25℃		2		V
Output Short Circuit Current	$I_{O(Short)}$	1	V_I=35V, T_j=25℃		300		mA
Peak Output Current	$I_{O(Peak)}$	1	T_j=25℃		0.7		A
Output Voltage Temperature Coefficient	$\Delta V_O/T_a$	1	I_O=5mA, T_j=0~125℃		−0.5		mV/℃
Output Voltage at Reset	$V_{O(Reset)}$	6	T_j=25℃, $I_{I(Reset)}$=1mA			1	V
Reset Input Current	$I_{I(Reset)}$	6	T_j=25℃			1	mA

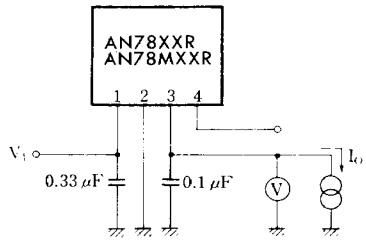
Note 1) The specified condition T_j=25℃ means that the test should be carried out with the test time so short (within 10ms) that the drift in characteristic value due to the rise in chip junction temperature can be ignored.
Note 2) When not specified, V_I=15V, I_O=350mA, C_I=0.33μF, C_O=0.1μF and T_j=0~125℃

● AN78M12R (500mA, 12V Type)

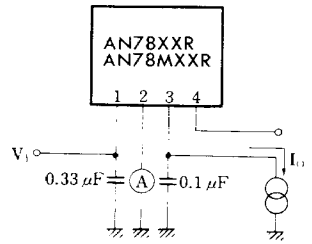
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Output Voltage	V_O	1	T_j=25℃	11.5	12	12.5	V
Output Voltage Tolerance	V_O	1	V_I=14.5~27V, I_O=5~350mA, T_j=0~125℃, P_D≦15W	11.4		12.6	V
Line Regulation	REG_{IN}	1	V_I=14.5~30V, T_j=25℃		8	100	mV
			V_I=16~30V, T_j=25℃		2	50	mV
Load Regulation	REG_L	1	I_O=5~500mA, T_j=25℃		25	240	mV
			I_O=5~200mA, T_j=25℃		10	120	mV
Bias Current	I_{Bias}	2	T_j=25℃		4.3	6	mA
Input Bias Current Fluctuation	$\Delta I_{Bias(IN)}$	2	V_I=14.5~30V, T_j=25℃			0.8	mA
Load Bias Current Fluctuation	$\Delta I_{Bias(L)}$	2	V_O=5~350mA, T_j=25℃			0.5	mA
Output Noise Voltage	V_{no}	1	f=10Hz~100kHz		75		μV
Ripple Rejection Ratio	RR	3	V_I=15~25V, I_O=100mA, f=120Hz	55			dB
Minimum Input/Output Voltage Difference	$V_{DIF(min.)}$	4	I_O=500mA, T_j=25℃		2		V
Output Short Circuit Current	$I_{O(Short)}$	1	V_I=35V, T_j=25℃		300		mA
Peak Output Current	$I_{O(Peak)}$	1	V_I=35V, T_j=25℃		700		mA
Output Voltage Temperature Coefficient	$\Delta V_O/T_a$	1	I_O=5mA, T_j=0~125℃		−0.5		mV/℃
Output Voltage at Reset	$V_{O(Reset)}$	6	T_j=25℃, $I_{I(Reset)}$=1mA			1	V
Reset Input Current	$I_{I(Reset)}$	6	T_j=25℃			1	mA

Note 1) The specified condition T_j=25℃ means that the test should be carried out with the test time so short (within 10ms) that the drift in characteristic value due to the rise in chip junction temperature can be ignored.
Note 2) When not specified, V_I=19V, I_O=350mA, C_I=0.33μF, C_O=0.1μF and T_j=0~125℃

Test Circuit 1 (V_O, REG_{IN}, REG_L, V_{no} / $I_{O(Short)}$, $I_{O(Peak)}$)

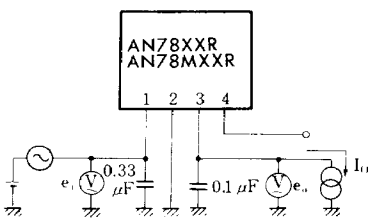


Test Circuit 2 (I_{Bias}, $\Delta I_{Bias(IN)}$, $\Delta I_{Bias(L)}$)



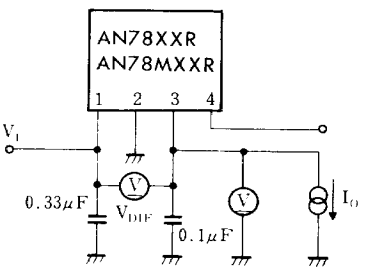
Note) The test time should be so short (within 10ms) the drift in characteristic value due to the rise in chip junction temperature can be ignored.

Test Circuit 3 (RR)



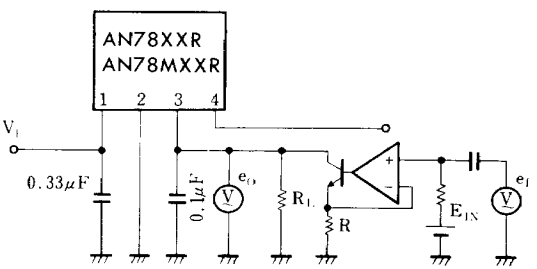
Note) $RR = 20 \log \left(|e_i| / |e_o| \right)$

Test Circuit 4 ($V_{DIF(min.)}$)



Note) V_{DIF} Value with V_O lowered by 5% from the prescribed value by lowering V_I

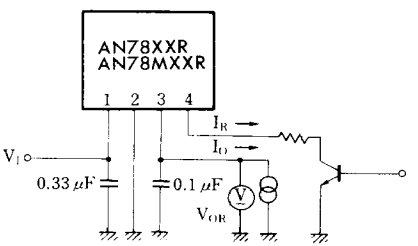
Test Circuit 5 (Z_O)



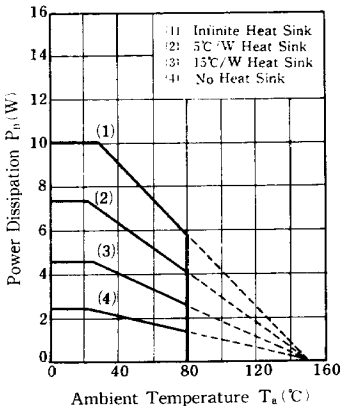
$$Z_{(OUT)} = \frac{|e_O|}{|e_I|}$$

DC load level is set by E_{IN} and R_L.

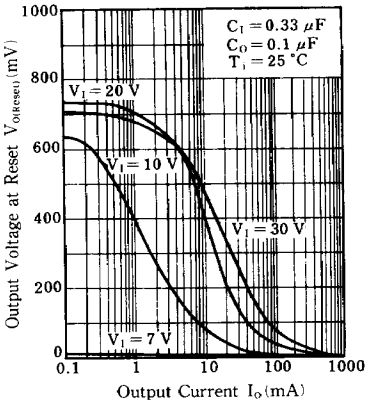
Test Circuit 6 ($V_{O(Reset)}$, $I_{I(Reset)}$)



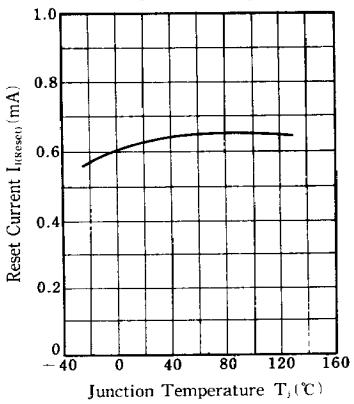
$P_D - Ta$



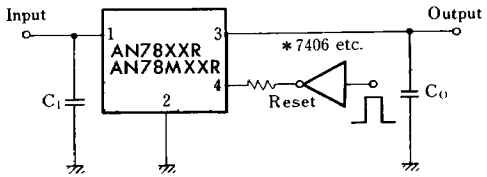
$V_{O(Reset)} - I_O$



$I_{I(Reset)} - Tj$



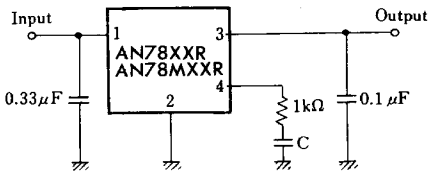
■ Basic Regulator Circuit



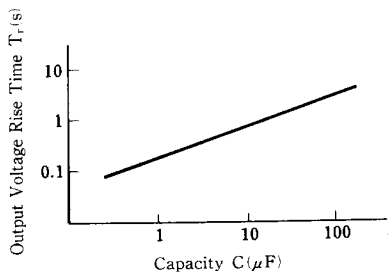
* For TTL, an open collector type inverter, buffer, gate etc. can be used.
Beware of the break down of TTL, as the reset pin bears voltage higher than the output voltage V_O by 1~2V.
C_I is set when the input line is long.
C_O improves the temperature response.

■ Application Circuit

(1) Soft Start Circuit



※ Control of Output Voltage Rise Time



■ Several Output Reset Circuits