Thermally Enhanced, Fully Integrated, Hall-Effect-Based High-Precision Linear Current Sensor IC with 100 µΩ Current Conductor

FEATURES AND BENEFITS

- Industry-leading total output accuracy achieved with new piecewise linear digital temperature compensation of offset and sensitivity
- Industry-leading noise performance through proprietary amplifier and filter design techniques
- 120 kHz typical bandwidth
- 4.1 µs output rise time in response to step input current
- Integrated shield greatly reduces capacitive coupling from current conductor to die due to high dV/dt signals, and prevents offset drift in high-side, high-voltage applications
- Greatly improved total output error through digitally programmed and compensated gain and offset over the full operating temperature range
- Small package size, with easy mounting capability
- Monolithic Hall IC for high reliability
- Ultralow power loss: 100 µΩ internal conductor resistance
- Galvanic isolation allows use in economical, high-side current sensing in high-voltage systems
- 4.5 to 5.5 V, single supply operation
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage

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PACKAGE: 5-pin package (suffix CB)

Additional leadforms available for qualifying volumes

DESCRIPTION

The Allegro™ ACS770 family of current sensor ICs provides economical and precise solutions for AC or DC current sensing. Typical applications include motor control, load detection and management, power supply and DC-to-DC converter control, inverter control, and overcurrent fault detection.

The device consists of a precision, low-offset linear Hall circuit with a copper conduction path located near the die. Applied current flowing through this copper conduction path generates a magnetic field that is concentrated by a low magnetic hysteresis core, then converted by the Hall IC into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional output voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy at the factory. Proprietary digital temperature compensation technology greatly improves the IC accuracy and temperature stability without influencing the high-bandwidth operation of the analog output.

High-level immunity to current conductor dV/dt and stray electric fields is offered by Allegro proprietary integrated shield technology for low output voltage ripple and low offset drift in high-side, high-voltage applications.

The output of the device has a positive slope (>$V_{CC}/2$ for bidirectional devices) when an increasing current flows through the primary copper conduction path (from terminal 4 to terminal 5), which is the path used for current sampling. The internal resistance of this conductive path is 100 µΩ typical, providing low power loss.

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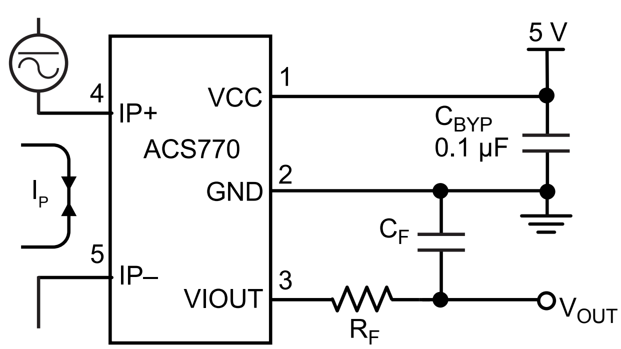
TÜV America
Certificate Number:
U8V 14 05 54214 028

Application 1: the ACS770 outputs an analog signal, V_{OUT}, that varies linearly with the bidirectional AC or DC primary sampled current, I_P, within the range specified. R_F and C_F are for optimal noise management, with values that depend on the application.



Typical Application

FEATURES AND BENEFITS (continued)

- Undervoltage lockout for V_{CC} below specification
- AEC Q-100 automotive qualified
- UL certified, File No. E316429

DESCRIPTION (continued)

The thickness of the copper conductor allows survival of the device at high overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 1 through 3). This allows the ACS770 family of sensor ICs to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The device is fully calibrated prior to shipment from the factory. The ACS770 family is lead (Pb) free. All leads are plated with 100% matte tin, and there is no Pb inside the package. The heavy gauge leadframe is made of oxygen-free copper.

SELECTION GUIDE

Part Number [1]	Package		Primary Sampled Current, I_P (A)	Sensitivity Sens (Typ.) (mV/A)	Current Directionality	T_{OP} (°C)	Packing [2]
	Terminals	Signal Pins					
ACS770LCB-050B-PFF-T	Formed	Formed	±50	40	Bidirectional	–40 to 150	34 pieces per tube
ACS770LCB-050U-PFF-T	Formed	Formed	50	80	Unidirectional		
ACS770LCB-100B-PFF-T	Formed	Formed	±100	20	Bidirectional		
ACS770LCB-100B-PSS-T	Straight	Straight	±100	20	Bidirectional		
ACS770LCB-100U-PFF-T	Formed	Formed	100	40	Unidirectional		
ACS770LCB-100U-PSF-T [3]	Straight	Formed	100	40	Unidirectional		
ACS770KCB-150B-PFF-T	Formed	Formed	±150	13.3	Bidirectional	–40 to 125	
ACS770KCB-150B-PSF-T	Straight	Formed	±150	13.3	Bidirectional		
ACS770KCB-150B-PSS-T	Straight	Straight	±150	13.3	Bidirectional		
ACS770KCB-150U-PFF-T	Formed	Formed	150	26.7	Unidirectional		
ACS770KCB-150U-PSF-T	Straight	Formed	150	26.7	Unidirectional		
ACS770ECB-200B-PFF-T	Formed	Formed	±200	10	Bidirectional	–40 to 85	
ACS770ECB-200B-PSF-T	Straight	Formed	±200	10	Bidirectional		
ACS770ECB-200U-PFF-T	Formed	Formed	200	20	Unidirectional		
ACS770ECB-200U-PSF-T	Straight	Formed	200	20	Unidirectional		

[1] Additional leadform options available for qualified volumes.
[2] Contact Allegro for additional packing options.
[3] ACS770LCB-100U-PSF-T part variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Date of status change: June 5, 2017. Deadline for receipt of LAST TIME BUY orders: December 31, 2017. For existing customer transition, and for new customers or new applications, contact Allegro.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		6	V
Reverse Supply Voltage	V_{RCC}		–0.5	V
Forward Output Voltage	V_{IOUT}		25	V
Reverse Output Voltage	V_{RIOUT}		–0.5	V
Output Source Current	$I_{OUT(Source)}$	VIOUT to GND	3	mA
Output Sink Current	$I_{OUT(Sink)}$	Minimum pull-up resistor of 500 Ω, from VCC to VIOUT	10	mA
Nominal Operating Ambient Temperature	T_{OP}	Range E	–40 to 85	°C
		Range K	–40 to 125	°C
		Range L	–40 to 150	°C
Maximum Junction	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Surge Strength Test Voltage	V_{SURGE}	Tested ±5 pulses at 2/minute in compliance to IEC 61000-4-5 1.2 µs (rise) / 50 µs (width)	8000	V
Dielectric Strength Test Voltage [1]	V_{ISO}	Agency type-tested for 60 seconds per UL standard 60950-1, 2nd Edition	4800	VAC
Working Voltage for Basic Isolation	V_{WFSI}	For basic (single) isolation per UL standard 60950-1, 2nd Edition	990	VDC or V_{pk}
			700	V_{rms}
Working Voltage for Reinforced Isolation	V_{WFRI}	For reinforced (double) isolation per UL standard 60950-1, 2nd Edition	636	VDC or V_{pk}
			450	V_{rms}

[1] 60-second testing is only done during the UL certification process. In production, Allegro conducts 1-second isolation testing according to UL 60950-1, 2nd Edition.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

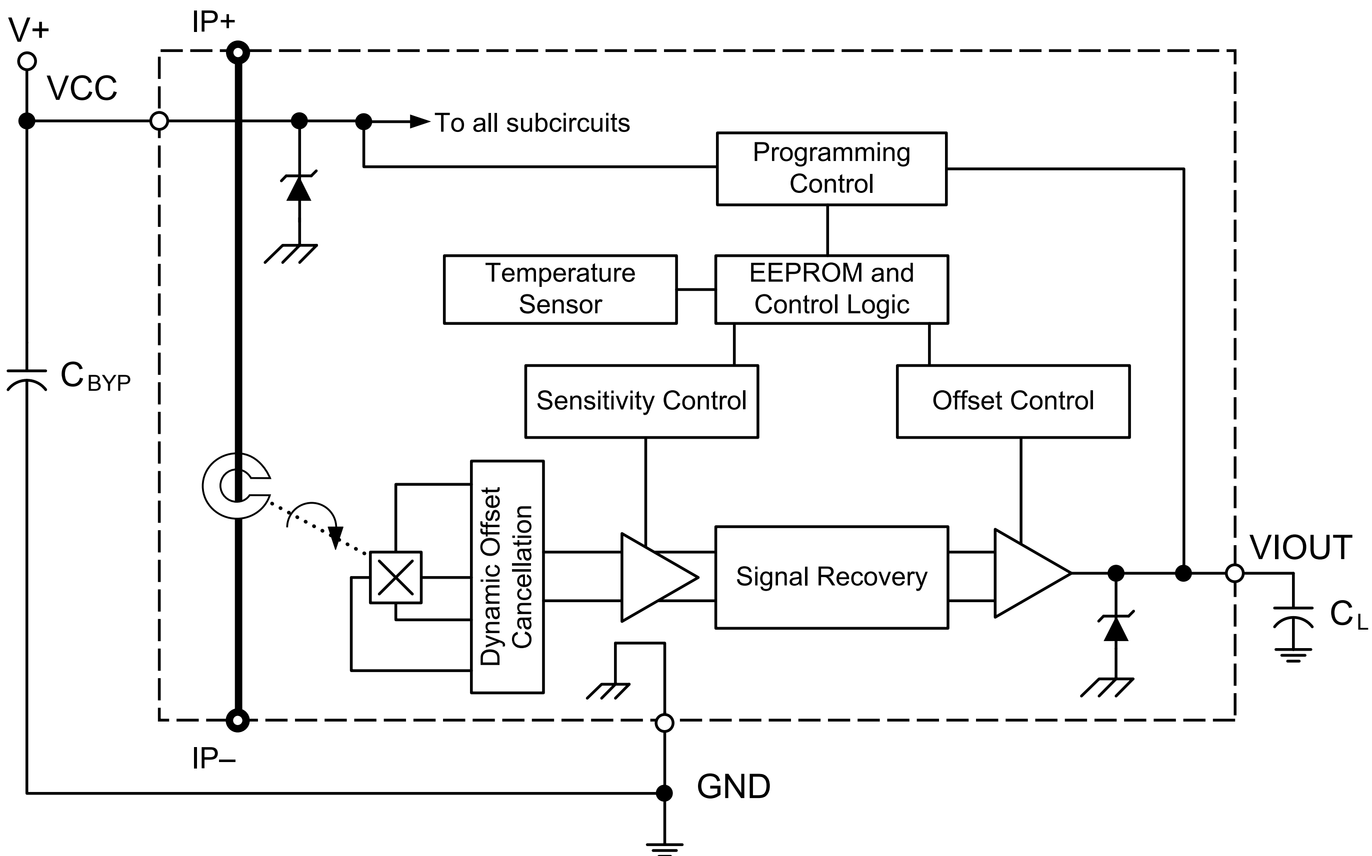
Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Mounted on the Allegro evaluation board with 2800 mm^2 (1400 mm^2 on component side and 1400 mm^2 on opposite side) of 4 oz. copper connected to the primary leadframe and with thermal vias connecting the copper layers. Performance is based on current flowing through the primary leadframe and includes the power consumed by the PCB.	7	°C/W

[2] Additional thermal information available on the Allegro website.

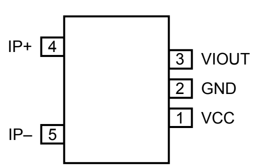
TYPICAL OVERCURRENT CAPABILITIES [3][4]

Characteristic	Symbol	Notes	Rating	Unit
Overcurrent	I_{POC}	T_A = 25°C, 1 second duration, 1% duty cycle	1200	A
		T_A = 85°C, 1 second duration, 1% duty cycle	900	A
		T_A = 150°C, 1 second duration, 1% duty cycle	600	A

[3] Test was done with Allegro evaluation board. The maximum allowed current is limited by T_J(max) only.
[4] For more overcurrent profiles, please see FAQ on the Allegro website, www.allegromicro.com.



Functional Block Diagram



Pinout Diagram

Terminal List Table

Number	Name	Description
1	VCC	Device power supply terminal
2	GND	Signal ground terminal
3	VIOUT	Analog output signal
4	IP+	Terminal for current being sampled
5	IP–	Terminal for current being sampled

COMMON OPERATING CHARACTERISTICS: Valid at T_{OP} = –40°C to 150°C, C_{BYP} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	Output open	–	10	15	mA
Supply Zener Voltage	V_Z	T_A = 25°C, I_{CC} = 30 mA	6.5	7.5	–	V
Power-On Delay [1][2]	t_{POD}	T_A = 25°C, C_{BYP} = open	–	90	–	µs
Temperature Compensation Power-On Time [1]	t_{TC}	T_A = 25°C, C_{BYP} = open	–	90	–	µs
Undervoltage Lockout (UVLO) Threshold [1]	V_{UVLOH}	T_A = 25°C, V_{CC} rising	–	3.8	–	V
	V_{UVLOL}	T_A = 25°C, V_{CC} falling	–	3	–	V
UVLO Enable/Disable Delay Time [1][2]	t_{UVLOE}	T_A = 25°C, C_{BYP} = open, V_{CC} Fall Time (5 V to 3 V) = 1 µs	–	75	–	µs
	t_{UVLOD}	T_A = 25°C, C_{BYP} = Open, V_{CC} Recover Time (3 V to 5 V) = 1 µs	–	14	–	µs
Power-On Reset Voltage [1]	V_{PORH}	T_A = 25°C, V_{CC} rising	–	2.9	–	V
	V_{PORL}	T_A = 25°C, V_{CC} falling	–	2.7	–	V
Rise Time [1][2]	t_r	I_P step = 60% of I_P+, 10% to 90% rise time, T_A = 25°C, C_L = 0.47 nF	–	4.1	–	µs
Propagation Delay Time [1][2]	t_{PROP}	I_P step = 60% of I_P+, 20% input to 20% output, T_A = 25°C, C_L = 0.47 nF	–	2.4	–	µs
Response Time [1][2]	$t_{RESPONSE}$	I_P step = 60% of I_P+, 80% input to 80% output, T_A = 25°C, C_{OUT} = 0.47 nF	–	4.6	–	µs
Internal Bandwidth	BW_i	–3 dB; T_A = 25°C, C_L = 0.47 nF	–	120	–	kHz
Output Load Resistance	R_L	VIOUT to GND	4.7	–	–	kΩ
Output Load Capacitance	C_L	VIOUT to GND	–	–	10	nF
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	100	–	µΩ
Quiescent Output Voltage [1]	$V_{IOUT(QBI)}$	Bidirectional variant, I_P = 0 A, T_A = 25°C	–	$V_{CC}/2$	–	V
	$V_{IOUT(QUNI)}$	Unidirectional variant, I_P = 0 A, T_A = 25°C	–	0.5	–	V
Ratiometry [1]	V_{RAT}	V_{CC} = 4.5 to 5.5 V	–	100	–	%

[1] See Characteristic Definitions section of this datasheet.
[2] See Timing Data Section of this datasheet.

X050B PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 150°C, C_{BYP} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–50	–	50	A
Sensitivity [2]	$Sens_{TA}$	Measured using full-scale I_P, T_A = 25°C	39.04	40	40.96	mV/A
	$Sens_{(TOP)HT}$	Measured using full-scale I_P, T_{OP} = 25°C to 150°C	39.04	40	40.96	mV/A
	$Sens_{(TOP)LT}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	38.6	40	41.4	mV/A
Sensitivity Drift Over Lifetime [3]	$\Delta Sens_{LIFE}$	T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–0.72	±0.24	0.72	mV/A
Noise [4]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	10	–	mV
Nonlinearity	E_{LIN}	Measured using full-scale and half-scale I_P,	–1	–	1	%
Electrical Offset Voltage [5][6]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±4	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–10	±6	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Electrical Offset Voltage Drift Over Lifetime [3]	$\Delta V_{OE(LIFE)}$	I_P = 0 A, T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–5	±2	5	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 50 A	–	120	300	mA
Total Output Error [7]	$E_{TOT(TA)}$	Measured using full-scale I_P, T_A = 25°C	–2.4	±0.5	2.4	%
	$E_{TOT(HT)}$	Measured using full-scale I_P, T_{OP} = 25°C to 150°C	–2.4	±1.5	2.4	%
	$E_{TOT(LT)}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	–3.5	±2	3.5	%
Total Output Error Drift Over Lifetime [3]	$\Delta E_{TOT(LIFE)}$	T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–1.9	±0.6	1.9	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[3] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[4] ±3 sigma noise voltage.
[5] Drift is referred to ideal $V_{IOUT(QBI)}$ = 2.5 V.
[6] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[7] This parameter may drift a maximum of $\Delta E_{TOT(LIFE)}$ over lifetime.

X050U PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 150°C, C_{BYP} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		0	–	50	A
Sensitivity [2]	$Sens_{TA}$	Measured using full-scale I_P, T_A = 25°C	78.08	80	81.92	mV/A
	$Sens_{(TOP)HT}$	Measured using full-scale I_P, T_{OP} = 25°C to 150°C	78.08	80	81.92	mV/A
	$Sens_{(TOP)LT}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	77.2	80	82.8	mV/A
Sensitivity Drift Over Lifetime [3]	$\Delta Sens_{LIFE}$	T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–1.44	±0.48	1.44	mV/A
Noise [4]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	20	–	mV
Nonlinearity	E_{LIN}	Measured using full-scale and half-scale I_P	–1	–	1	%
Electrical Offset Voltage [5][6]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±4	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–10	±6	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Electrical Offset Voltage Drift Over Lifetime [3]	$\Delta V_{OE(LIFE)}$	I_P = 0 A, T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–5	±2	5	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 50 A	–	120	300	mA
Total Output Error [7]	$E_{TOT(TA)}$	Measured using full-scale I_P, T_A = 25°C	–2.4	±0.5	2.4	%
	$E_{TOT(HT)}$	Measured using full-scale I_P, T_{OP} = 25°C to 150°C	–2.4	±1.5	2.4	%
	$E_{TOT(LT)}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	–3.5	±2	3.5	%
Total Output Error Drift Over Lifetime [3]	$\Delta E_{TOT(LIFE)}$	T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–1.9	±0.6	1.9	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[3] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[4] ±3 sigma noise voltage.
[5] Drift is referred to ideal $V_{IOUT(QBI)}$ = 0.5 V.
[6] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[7] This parameter may drift a maximum of $\Delta E_{TOT(LIFE)}$ over lifetime.

X100B PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 150°C, C_{BYP} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–100	–	100	A
Sensitivity [2]	$Sens_{TA}$	Measured using full-scale I_P, T_A = 25°C	19.52	20	20.48	mV/A
	$Sens_{(TOP)HT}$	Measured using full-scale I_P, T_{OP} = 25°C to 150°C	19.52	20	20.48	mV/A
	$Sens_{(TOP)LT}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	19.3	20	20.7	mV/A
Sensitivity Drift Over Lifetime [3]	$\Delta Sens_{LIFE}$	T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–0.36	±0.12	0.36	mV/A
Noise [4]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	6	–	mV
Nonlinearity	E_{LIN}	Measured using full-scale and half-scale I_P	–1	–	1	%
Electrical Offset Voltage [5][6]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±4	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–10	±6	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Electrical Offset Voltage Drift Over Lifetime [3]	$\Delta V_{OE(LIFE)}$	I_P = 0 A, T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–5	±2	5	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 100 A	–	170	400	mA
Total Output Error [7]	$E_{TOT(TA)}$	Measured using full-scale I_P, T_A = 25°C	–2.4	±0.5	2.4	%
	$E_{TOT(HT)}$	Measured using full-scale I_P, T_{OP} = 25°C to 150°C	–2.4	±1.5	2.4	%
	$E_{TOT(LT)}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	–3.5	±2	3.5	%
Total Output Error Drift Over Lifetime [3]	$\Delta E_{TOT(LIFE)}$	T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–1.9	±0.6	1.9	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[3] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[4] ±3 sigma noise voltage.
[5] Drift is referred to ideal $V_{IOUT(QBI)}$ = 2.5 V.
[6] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[7] This parameter may drift a maximum of $\Delta E_{TOT(LIFE)}$ over lifetime.

X100U PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 150°C, C_{BYP} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		0	–	100	A
Sensitivity [2]	$Sens_{TA}$	Measured using full-scale I_P, T_A = 25°C	39.04	40	40.96	mV/A
	$Sens_{(TOP)HT}$	Measured using full-scale I_P, T_{OP} = 25°C to 150°C	39.04	40	40.96	mV/A
	$Sens_{(TOP)LT}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	38.6	40	41.4	mV/A
Sensitivity Drift Over Lifetime [3]	$\Delta Sens_{LIFE}$	T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–0.72	±0.24	0.72	mV/A
Noise [4]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	12	–	mV
Nonlinearity	E_{LIN}	Measured using full-scale and half-scale I_P	–1	–	1	%
Electrical Offset Voltage [5][6]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±4	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 150°C	–10	±6	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Electrical Offset Voltage Drift Over Lifetime [3]	$\Delta V_{OE(LIFE)}$	I_P = 0 A, T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–5	±2	5	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 100 A	–	170	400	mA
Total Output Error [7]	$E_{TOT(TA)}$	Measured using full-scale I_P, T_A = 25°C	–2.4	±0.5	2.4	%
	$E_{TOT(HT)}$	Measured using full-scale I_P, T_{OP} = 25°C to 150°C	–2.4	±1.5	2.4	%
	$E_{TOT(LT)}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	–3.5	±2	3.5	%
Total Output Error Drift Over Lifetime [3]	$\Delta E_{TOT(LIFE)}$	T_{OP} = –40°C to 150°C, shift after AEC-Q100 grade 0 qualification testing	–1.9	±0.6	1.9	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[3] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[4] ±3 sigma noise voltage.
[5] Drift is referred to ideal $V_{IOUT(QBI)}$ = 0.5 V.
[6] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[7] This parameter may drift a maximum of $\Delta E_{TOT(LIFE)}$ over lifetime.

X150B PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 125°C, C_{BYP} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–150	–	150	A
Sensitivity [2]	$Sens_{TA}$	Measured using full-scale I_P, T_A = 25°C	13.01	13.33	13.65	mV/A
	$Sens_{(TOP)HT}$	Measured using full-scale I_P, T_{OP} = 25°C to 125°C	13.01	13.33	13.65	mV/A
	$Sens_{(TOP)LT}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	12.86	13.33	13.8	mV/A
Sensitivity Drift Over Lifetime [3]	$\Delta Sens_{LIFE}$	T_{OP} = –40°C to 125°C, shift after AEC-Q100 grade 0 qualification testing	–0.24	±0.08	0.24	mV/A
Noise [4]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	4	–	mV
Nonlinearity	E_{LIN}	Measured using full-scale and half-scale I_P	–1	–	1	%
Electrical Offset Voltage [5][6]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±4	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 125°C	–10	±6	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Electrical Offset Voltage Drift Over Lifetime [3]	$\Delta V_{OE(LIFE)}$	I_P = 0 A, T_{OP} = –40°C to 125°C, shift after AEC-Q100 grade 0 qualification testing	–5	±2	5	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 150 A	–	225	400	mA
Total Output Error [7]	$E_{TOT(TA)}$	Measured using full-scale I_P, T_A = 25°C	–2.4	±0.5	2.4	%
	$E_{TOT(HT)}$	Measured using full-scale I_P, T_{OP} = 25°C to 125°C	–2.4	±1.5	2.4	%
	$E_{TOT(LT)}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	–3.5	±2	3.5	%
Total Output Error Drift Over Lifetime [3]	$\Delta E_{TOT(LIFE)}$	T_{OP} = –40°C to 125°C, shift after AEC-Q100 grade 0 qualification testing	–1.9	±0.6	1.9	%
Symmetry	E_{SYM}	Over half-scale of I_P	99	100	101	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[3] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[4] ±3 sigma noise voltage.
[5] Drift is referred to ideal $V_{IOUT(QBI)}$ = 2.5 V.
[6] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[7] This parameter may drift a maximum of $\Delta E_{TOT(LIFE)}$ over lifetime.

X150U PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 125°C, C_{BYP} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		0	–	150	A
Sensitivity [2]	$Sens_{TA}$	Measured using full-scale I_P, T_A = 25°C	26.02	26.66	27.30	mV/A
	$Sens_{(TOP)HT}$	Measured using full-scale I_P, T_{OP} = 25°C to 125°C	26.02	26.66	27.30	mV/A
	$Sens_{(TOP)LT}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	25.73	26.66	27.59	mV/A
Sensitivity Drift Over Lifetime [3]	$\Delta Sens_{LIFE}$	T_{OP} = –40°C to 125°C, shift after AEC-Q100 grade 0 qualification testing	–0.48	±0.16	0.48	mV/A
Noise [4]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	6	–	mV
Nonlinearity	E_{LIN}	Measured using full-scale and half-scale I_P	–1	–	1	%
Electrical Offset Voltage [5][6]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±4	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 125°C	–10	±6	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Electrical Offset Voltage Drift Over Lifetime [3]	$\Delta V_{OE(LIFE)}$	I_P = 0 A, T_{OP} = –40°C to 125°C, shift after AEC-Q100 grade 0 qualification testing	–5	±2	5	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 150 A	–	225	400	mA
Total Output Error [7]	$E_{TOT(TA)}$	Measured using full-scale I_P, T_A = 25°C	–2.4	±0.5	2.4	%
	$E_{TOT(HT)}$	Measured using full-scale I_P, T_{OP} = 25°C to 125°C	–2.4	±1.5	2.4	%
	$E_{TOT(LT)}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	–3.5	±2	3.5	%
Total Output Error Drift Over Lifetime [3]	$\Delta E_{TOT(LIFE)}$	T_{OP} = –40°C to 125°C, shift after AEC-Q100 grade 0 qualification testing	–1.9	±0.6	1.9	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[3] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[4] ±3 sigma noise voltage.
[5] Drift is referred to ideal $V_{IOUT(QBI)}$ = 0.5 V.
[6] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[7] This parameter may drift a maximum of $\Delta E_{TOT(LIFE)}$ over lifetime.

X200B PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 85°C, C_{BYP} = 0.1 μF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		–200	–	200	A
Sensitivity [2]	$Sens_{TA}$	Measured using full-scale I_P, T_A = 25°C	9.76	10	10.24	mV/A
	$Sens_{(TOP)HT}$	Measured using full-scale I_P, T_{OP} = 25°C to 85°C	9.76	10	10.24	mV/A
	$Sens_{(TOP)LT}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	9.65	10	10.35	mV/A
Sensitivity Drift Over Lifetime [3]	$\Delta Sens_{LIFE}$	T_{OP} = –40°C to 85°C, shift after AEC-Q100 grade 0 qualification testing	–0.18	±0.06	0.18	mV/A
Noise [4]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	3	–	mV
Nonlinearity	E_{LIN}	Measured using full-scale and half-scale I_P	–1	–	1	%
Electrical Offset Voltage [5][6]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±4	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 85°C	–10	±6	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Electrical Offset Voltage Drift Over Lifetime [3]	$\Delta V_{OE(LIFE)}$	I_P = 0 A, T_{OP} = –40°C to 85°C, shift after AEC-Q100 grade 0 qualification testing	–5	±2	5	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 200 A	–	250	575	mA
Total Output Error [7]	$E_{TOT(TA)}$	Measured using full-scale I_P, T_A = 25°C	–2.4	±0.5	2.4	%
	$E_{TOT(HT)}$	Measured using full-scale I_P, T_{OP} = 25°C to 85°C	–2.4	±1.5	2.4	%
	$E_{TOT(LT)}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	–3.5	±2	3.5	%
Total Output Error Drift Over Lifetime [3]	$\Delta E_{TOT(LIFE)}$	T_{OP} = –40°C to 85°C, shift after AEC-Q100 grade 0 qualification testing	–1.9	±0.6	1.9	%

[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[3] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[4] ±3 sigma noise voltage.
[5] Drift is referred to ideal $V_{IOUT(QBI)}$ = 2.5 V.
[6] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[7] This parameter may drift a maximum of $\Delta E_{TOT(LIFE)}$ over lifetime.

X200U PERFORMANCE CHARACTERISTICS [1]: T_{OP} = –40°C to 85°C, C_{BYP} = 0.1 µF, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Primary Sampled Current	I_P		0	–	200	A
Sensitivity [2]	$Sens_{TA}$	Measured using full-scale I_P, T_A = 25°C	19.52	20	20.48	mV/A
	$Sens_{(TOP)HT}$	Measured using full-scale I_P, T_{OP} = 25°C to 85°C	19.52	20	20.48	mV/A
	$Sens_{(TOP)LT}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	19.3	20	20.7	mV/A
Sensitivity Drift Over Lifetime [3]	$\Delta Sens_{LIFE}$	T_{OP} = –40°C to 85°C, shift after AEC-Q100 grade 0 qualification testing	–0.36	±0.12	0.36	mV/A
Noise [4]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	6	–	mV
Nonlinearity	E_{LIN}	Measured using full-scale and half-scale I_P	–1	–	1	%
Electrical Offset Voltage [5][6]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–10	±4	10	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 85°C	–10	±6	10	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–20	±6	20	mV
Electrical Offset Voltage Drift Over Lifetime [3]	$\Delta V_{OE(LIFE)}$	I_P = 0 A, T_{OP} = –40°C to 85°C, shift after AEC-Q100 grade 0 qualification testing	–5	±2	5	mV
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, T_A = 25°C, after excursion of 200 A	–	250	575	mA
Total Output Error [7]	$E_{TOT(TA)}$	Measured using full-scale I_P, T_A = 25°C	–2.4	±0.5	2.4	%
	$E_{TOT(HT)}$	Measured using full-scale I_P, T_{OP} = 25°C to 85°C	–2.4	±1.5	2.4	%
	$E_{TOT(LT)}$	Measured using full-scale I_P, T_{OP} = –40°C to 25°C	–3.5	±2	3.5	%
Total Output Error Drift Over Lifetime [3]	$\Delta E_{TOT(LIFE)}$	T_{OP} = –40°C to 85°C, shift after AEC-Q100 grade 0 qualification testing	–1.9	±0.6	1.9	%

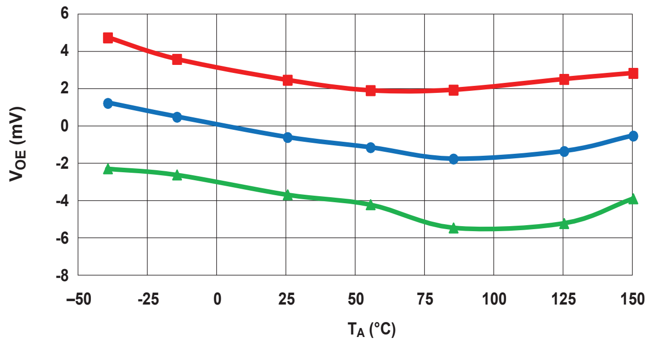
[1] See Characteristic Performance Data page for parameter distributions over temperature range.
[2] This parameter may drift a maximum of $\Delta Sens_{LIFE}$ over lifetime.
[3] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits, including Package Hysteresis. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[4] ±3 sigma noise voltage.
[5] Drift is referred to ideal $V_{IOUT(QBI)}$ = 0.5 V.
[6] This parameter may drift a maximum of $\Delta V_{OE(LIFE)}$ over lifetime.
[7] This parameter may drift a maximum of $\Delta E_{TOT(LIFE)}$ over lifetime.

CHARACTERISTIC PERFORMANCE DATA

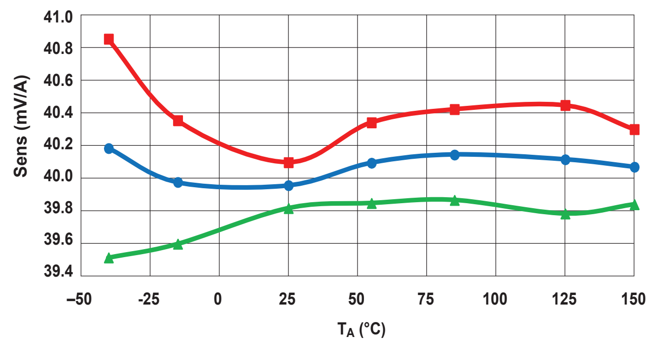
Data Taken using the ACS770LCB-050B

Accuracy Data

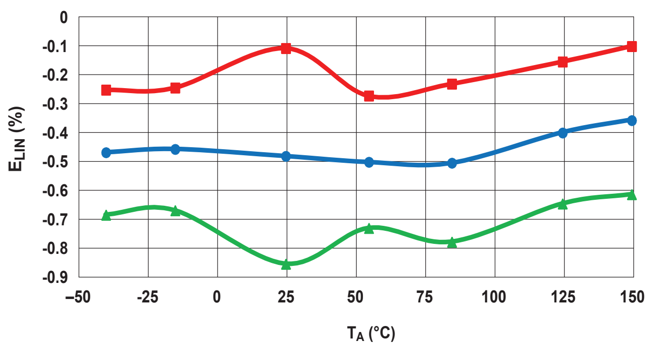
Electrical Offset Voltage versus Ambient Temperature



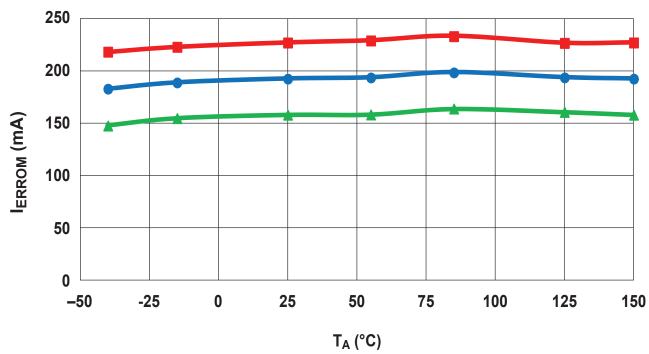
Sensitivity versus Ambient Temperature



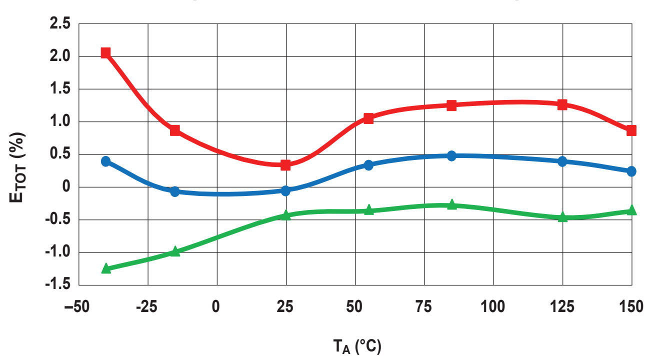
Nonlinearity versus Ambient Temperature



Magnetic Offset Error versus Ambient Temperature



Total Output Error versus Ambient Temperature

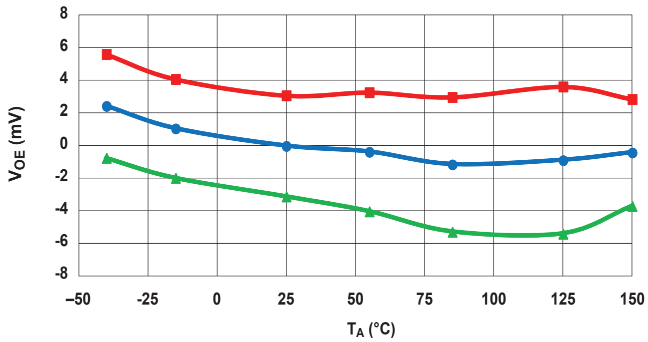


Mean + 3 sigma   Mean   Mean – 3 sigma

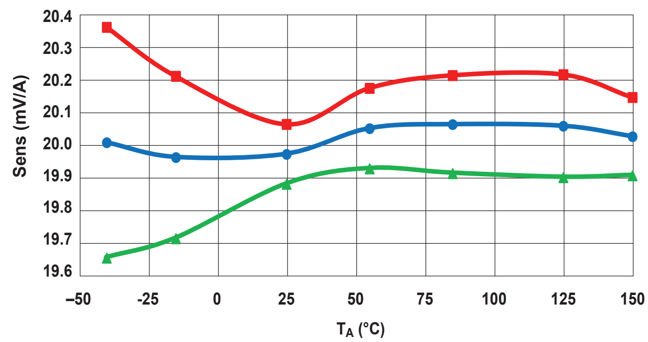
Data Taken using the ACS770LCB-100B

Accuracy Data

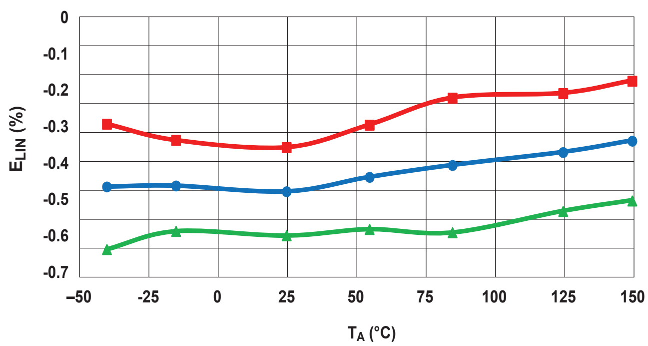
Electrical Offset Voltage versus Ambient Temperature



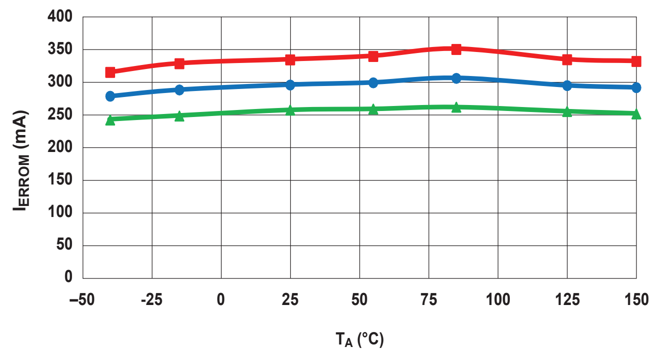
Sensitivity versus Ambient Temperature



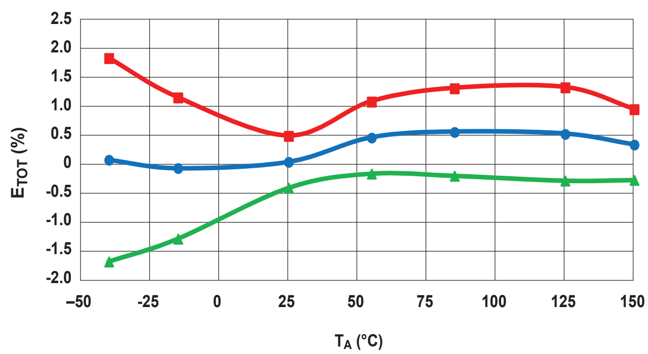
Nonlinearity versus Ambient Temperature



Magnetic Offset Error versus Ambient Temperature



Total Output Error versus Ambient Temperature

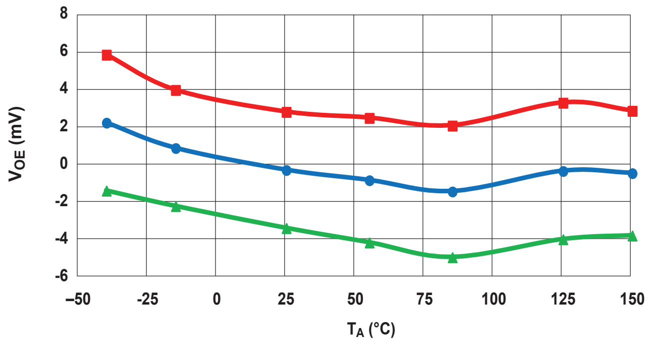


Mean + 3 sigma   Mean   Mean – 3 sigma

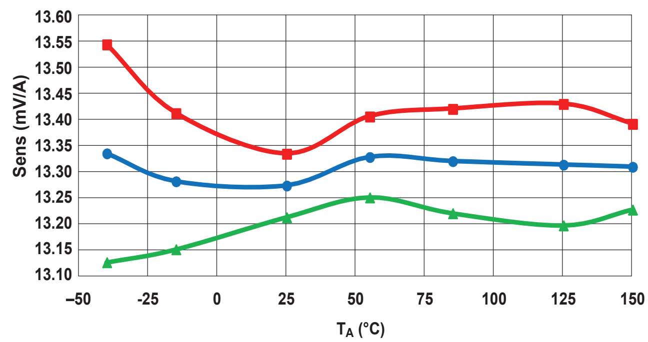
Data Taken using the ACS770KCB-150B

Accuracy Data

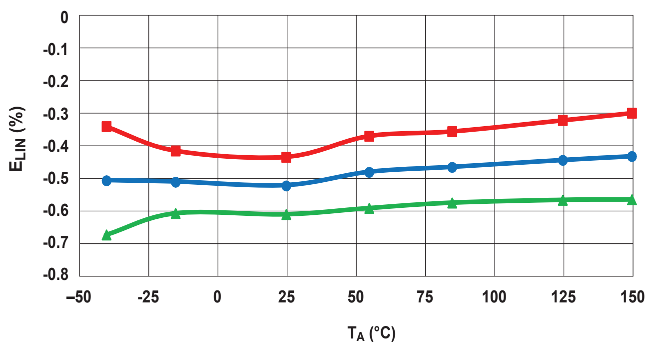
Electrical Offset Voltage versus Ambient Temperature



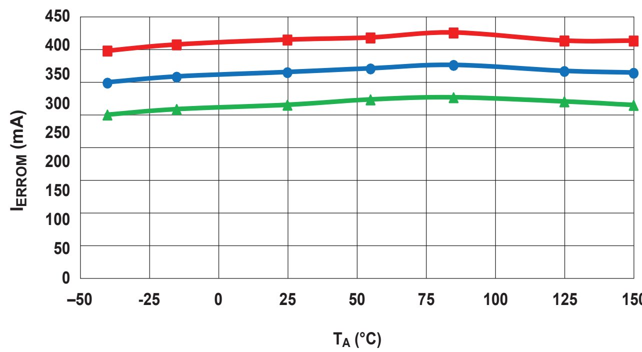
Sensitivity versus Ambient Temperature



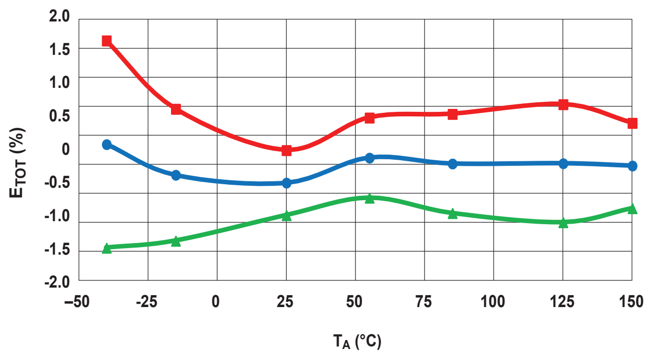
Nonlinearity versus Ambient Temperature



Magnetic Offset Error versus Ambient Temperature



Total Output Error versus Ambient Temperature

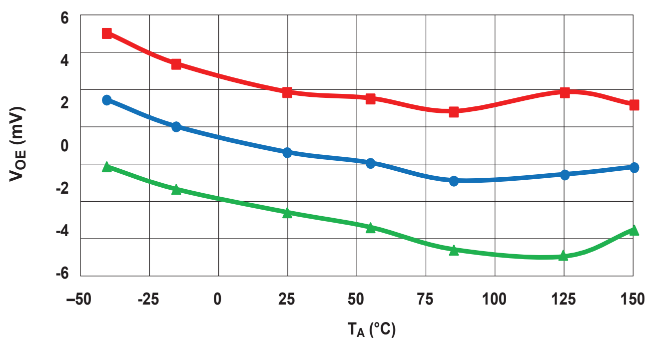


Mean + 3 sigma   Mean   Mean – 3 sigma

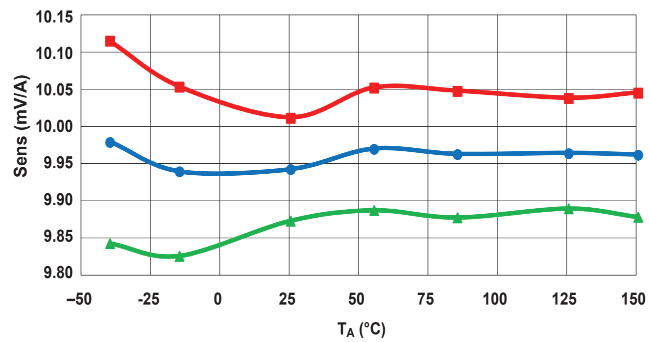
Data Taken using the ACS770ECB-200B

Accuracy Data

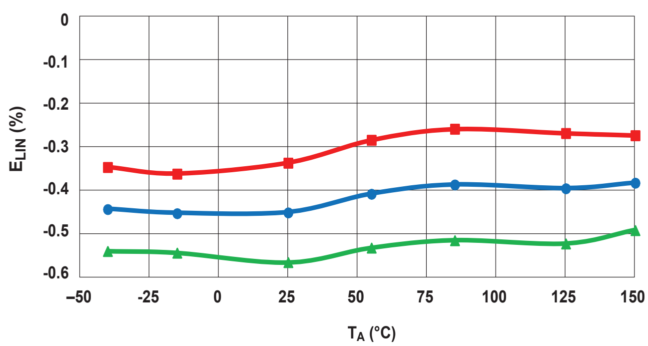
Electrical Offset Voltage versus Ambient Temperature



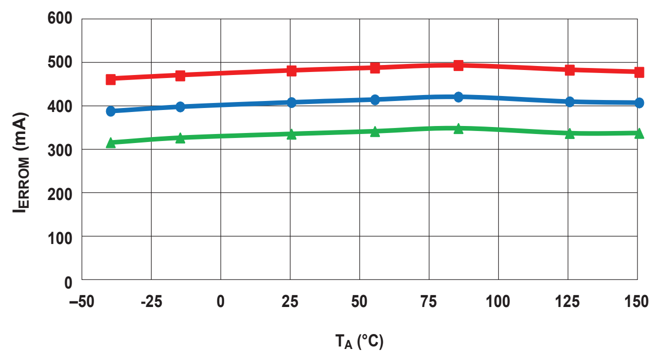
Sensitivity versus Ambient Temperature



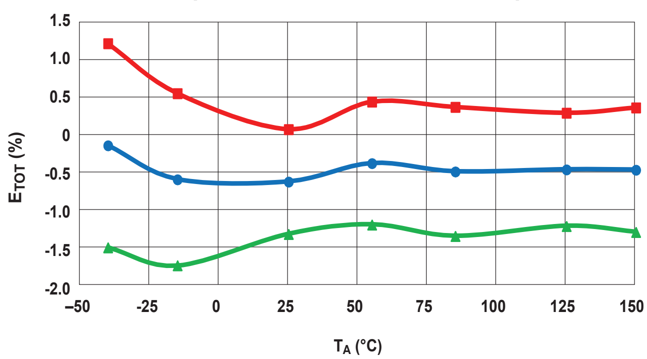
Nonlinearity versus Ambient Temperature



Magnetic Offset Error versus Ambient Temperature



Total Output Error versus Ambient Temperature



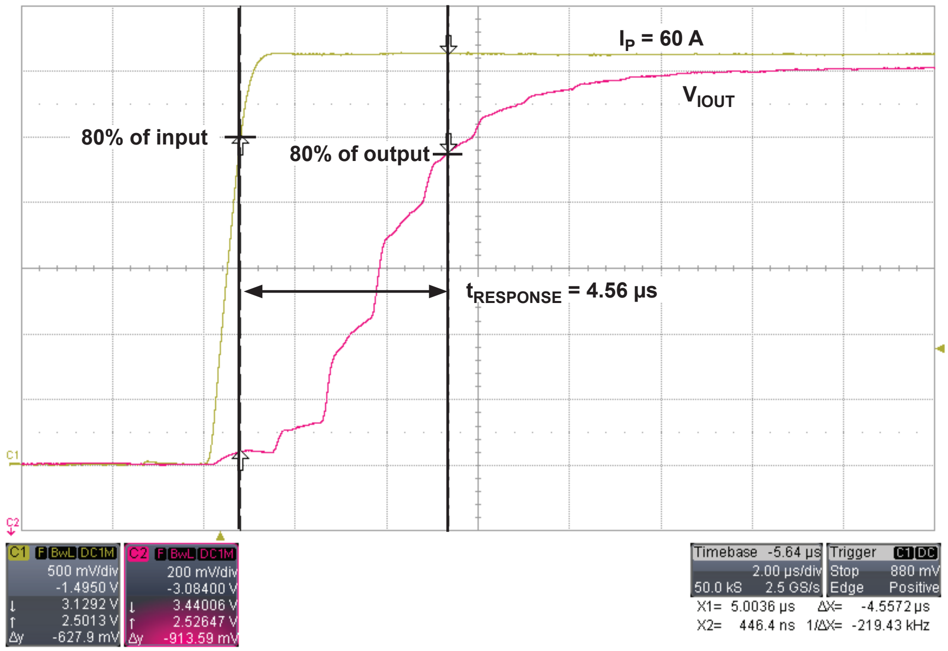
Mean + 3 sigma   Mean   Mean – 3 sigma

Data Taken using the ACS770LCB-100B

Timing Data

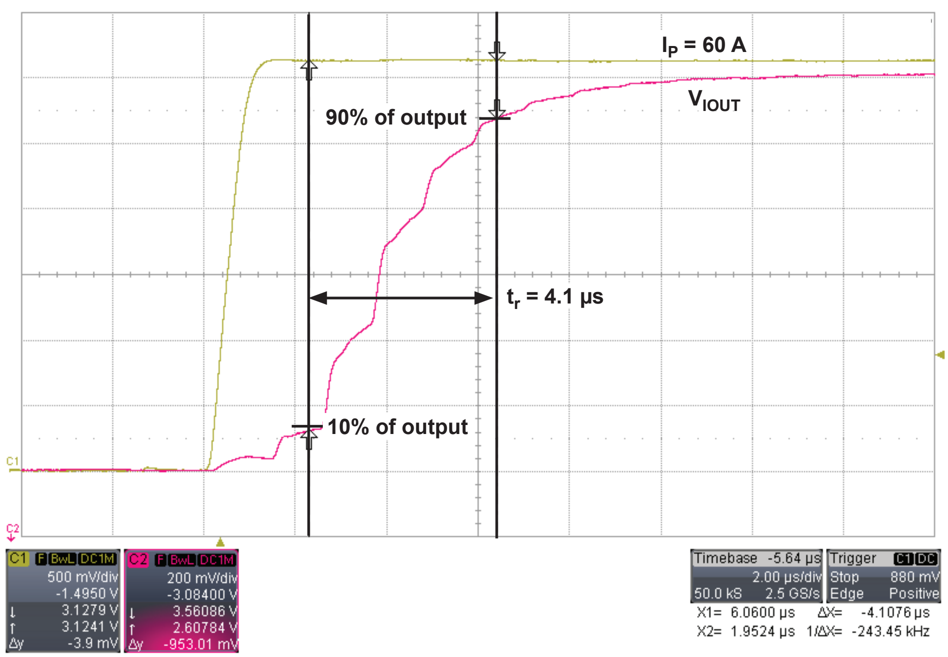
Response Time

I_P = 60 A , 10% to 90% rise time = 1 µs, C_{BYPASS} = 0.1 µF, C_L = 0.47 nF



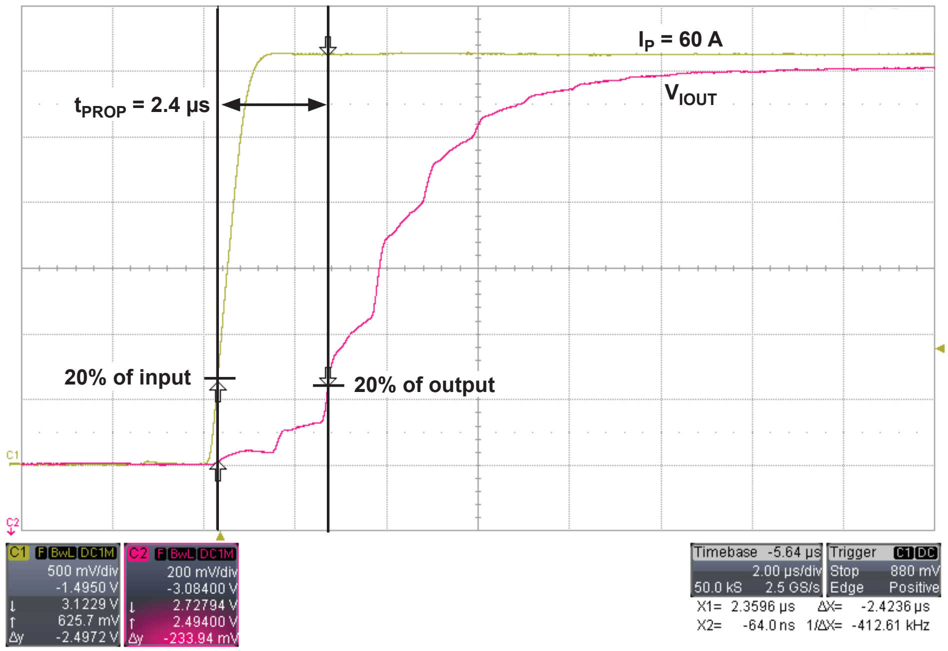
Rise Time

I_P = 60 A , 10% to 90% rise time = 1 µs, C_{BYPASS} = 0.1 µF, C_L = 0.47 nF



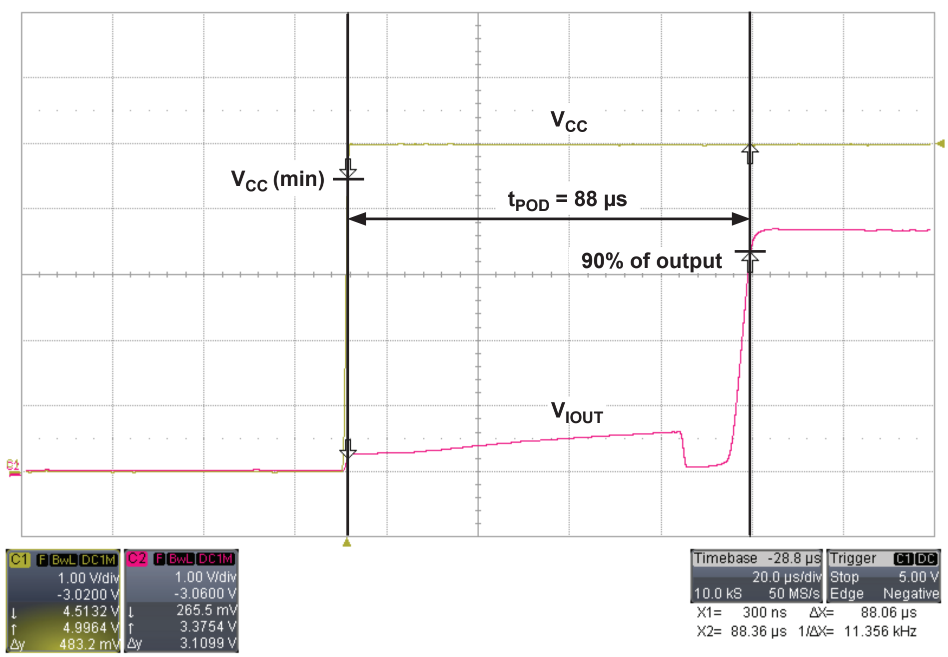
Propagation Time

I_P = 60 A , 10% to 90% rise time = 1 µs, C_{BYPASS} = 0.1 µF, C_L = 0.47 nF



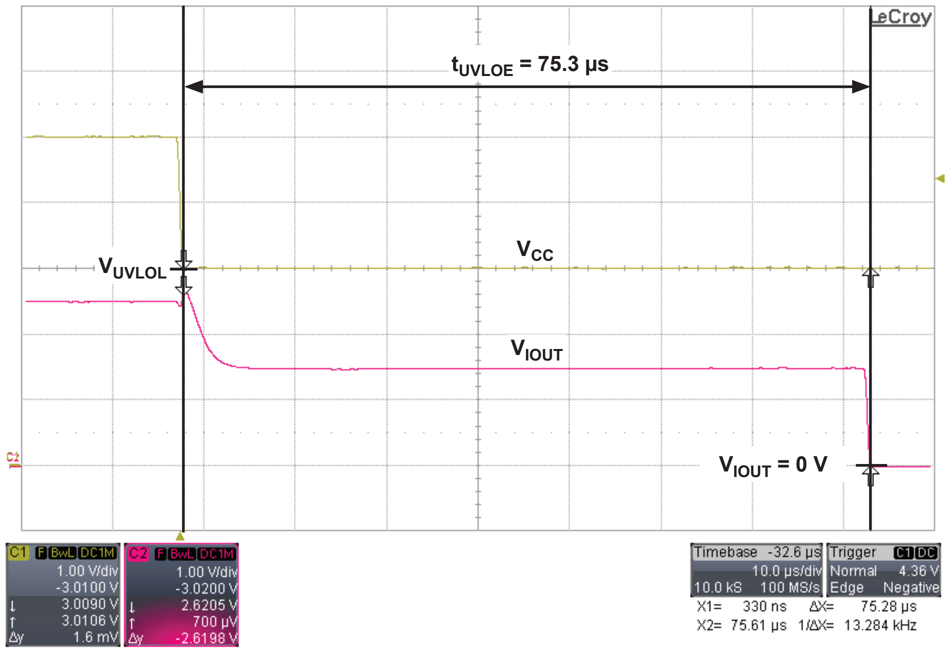
Power-On Delay

I_P = 60 A DC, C_{BYPASS} = Open, C_L = 0.47 nF



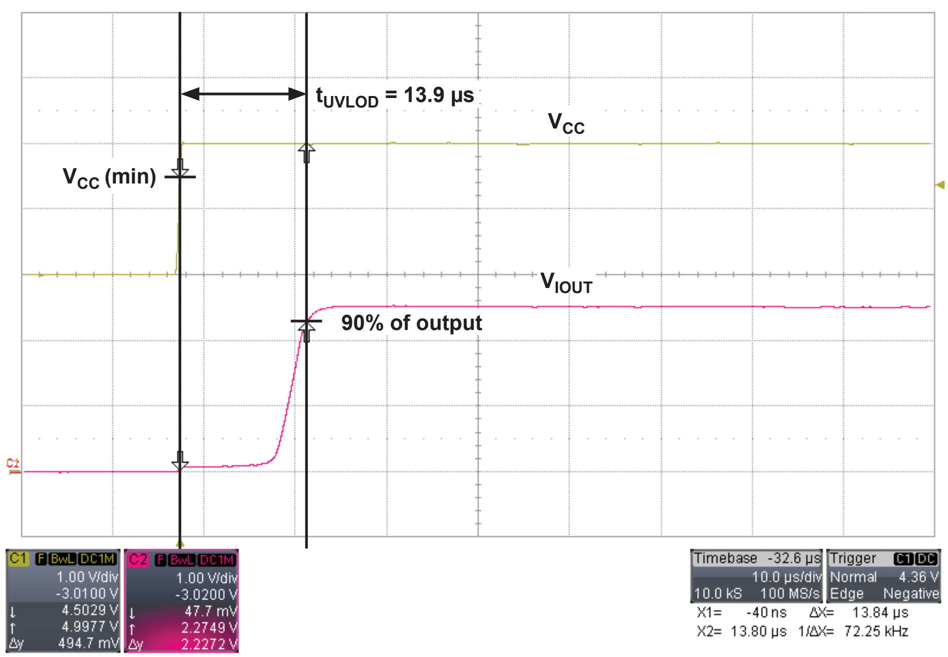
UVLO Enable Time (t_{UVLOE})

I_P = 0 A , C_{BYPASS} = Open, C_L = Open, V_{CC} 5 V to 3 V fall time = 1 µs



UVLO Disable Time (t_{UVLOD})

I_P = 0 A , C_{BYPASS} = Open, C_L = Open, V_{CC} 3 V to 5 V recovery time = 1 µs



CHARACTERISTIC DEFINITIONS

Definitions of Accuracy Characteristics

SENSITIVITY (Sens)

The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the half-scale current of the device.

NOISE (V_{NOISE})

The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

NONLINEARITY (E_{LIN})

The ACS770 is designed to provide a linear output in response to a ramping current. Consider two current levels: I1 and I2. Ideally, the sensitivity of a device is the same for both currents, for a given supply voltage and temperature. Nonlinearity is present when there is a difference between the sensitivities measured at I1 and I2. Nonlinearity is calculated separately for the positive (E_{LINpos}) and negative (E_{LINneg}) applied currents as follows:

$$E_{LINpos} = 100\ (\%) \times \{1 - (Sens_{IPOS2} / Sens_{IPOS1})\}$$

$$E_{LINneg} = 100\ (\%) \times \{1 - (Sens_{INEG2} / Sens_{INEG1})\}$$

where:

$$Sens_{Ix} = (V_{IOUT(Ix)} - V_{IOUT(Q)}) / Ix$$

and I_{POSx} and I_{NEGx} are positive and negative currents.

Then:

$$E_{LIN} = \max(E_{LINpos}, E_{LINneg})$$

RATIOMETRY

The device features a ratiometric output. This means that the quiescent voltage output, V_{IOUTQ}, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC}. The ratiometric change (%) in the quiescent voltage output is defined as:

$$\Delta V_{IOUTQ(\Delta V)} = \frac{V_{IOUTQ(V_{CC})} / V_{IOUTQ(5V)}}{V_{CC} / 5\text{ V}} \times 100\ (\%)$$

and the ratiometric change (%) in sensitivity is defined as:

$$\Delta Sens_{(\Delta V)} = \frac{Sens_{(V_{CC})} / Sens_{(5V)}}{V_{CC} / 5\text{ V}} \times 100\ (\%)$$

QUIESCENT OUTPUT VOLTAGE ($V_{IOUT(Q)}$)

The output of the device when the primary current is zero. For bidirectional current flow, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 5 V translates into $V_{IOUT(QBI)}$ = 2.5 V. For unidirectional devices, when V_{CC} = 5 V, $V_{IOUT(QUNI)}$ = 0.5 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim, magnetic hysteresis, and thermal drift.

ELECTRICAL OFFSET VOLTAGE (V_{OE})

The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ for bidirectional sensor ICs and 0.5 V for unidirectional sensor ICs, due to nonmagnetic causes.

MAGNETIC OFFSET ERROR (I_{ERROM})

The magnetic offset is due to the residual magnetism (remnant field) of the core material. The magnetic offset error is highest when the magnetic circuit has been saturated, usually when the device has been subjected to a full-scale or high-current overload condition. The magnetic offset is largely dependent on the material used as a flux concentrator.

TOTAL OUTPUT ERROR (E_{TOT})

The maximum deviation of the actual output from its ideal value, also referred to as *accuracy*, illustrated graphically in the output voltage versus current chart on the following page.

E_{TOT} is divided into four areas:

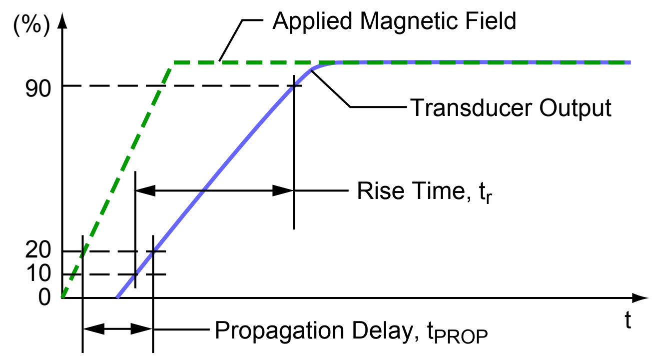
- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy at the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy at the full-scale current flow including temperature effects.

$$E_{TOT(IP)} = \frac{V_{IOUT(IP)} - V_{IOUT\_IDEAL(IP)}}{Sens_{IDEAL} \times I_P} \times 100\ (\%)$$

where

$$V_{IOUT\_IDEAL(IP)} = V_{IOUT(Q)} + (Sens_{IDEAL} \times I_P)$$

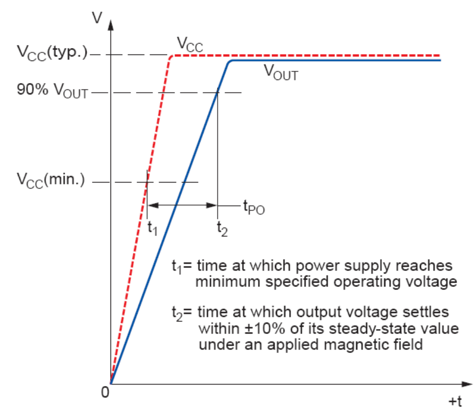
Definitions of Dynamic Response Characteristics



POWER-ON DELAY (t_{POD})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Delay, t_{POD} , is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.



TEMPERATURE COMPENSATION POWER-ON TIME (t_{TC})

After Power-On Delay, t_{POD}, elapses, t_{TC} also is required before a valid temperature compensated output.

RISE TIME (t_r)

The time interval between a) when the device reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

RESPONSE TIME ($t_{RESPONSE}$)

The time interval between a) when the applied current reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied current.

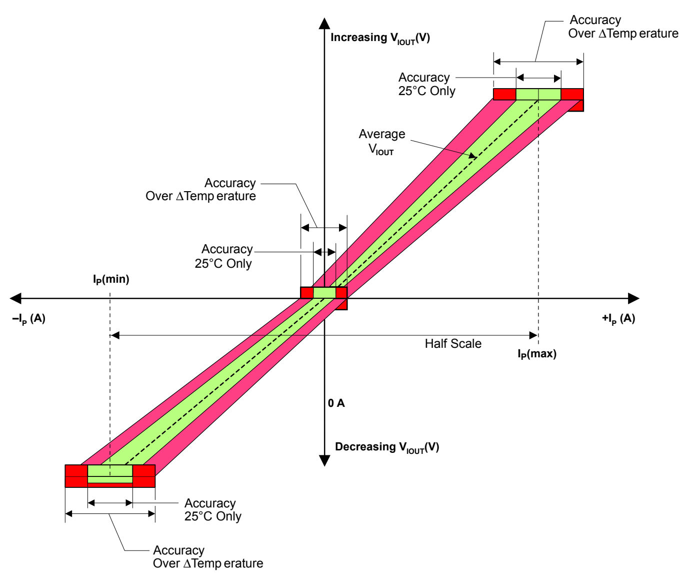
PROPAGATION DELAY (t_{PROP})

The time interval between a) when the input current reaches 20% of its final value, and b) when the output reaches 20% of its final value.

POWER-ON RESET VOLTAGE (V_{POR})

At power-up, to initialize to a known state and avoid current spikes, the ACS770 is held in Reset state. The Reset signal is disabled when V_{CC} reaches V_{UVLOH} and time t_{PORR} has elapsed, allowing output voltage to go from a high-impedance state into normal operation. During power-down, the Reset signal is enabled when V_{CC} reaches V_{PORL}, causing output voltage to go into a high-impedance state. (Note that a detailed description of POR and UVLO operation can be found in the Functional Description section.)

Output Voltage versus Sampled Current
Total Output Error at 0 A and at Full-Scale Current



POWER-ON RESET RELEASE TIME (t_{PORR})

When V_{CC} rises to V_{PORH}, the Power-On Reset Counter starts. The ACS770 output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has exceeded V_{UVLOH}.

UNDERVOLTAGE LOCKOUT THRESHOLD (V_{UVLO})

If V_{CC} drops below V_{UVLOL}, output voltage will be locked to GND. If V_{CC} starts rising, the ACS770 will come out of the locked state when V_{CC} reaches V_{UVLOH}.

SYMMETRY (E_{SYM})

The degree to which the absolute voltage output from the IC varies in proportion to either a positive or negative half-scale primary current. The following equation is used to derive symmetry:

$$100\left(\frac{V_{IOUT\_+half\text{-}scale\ amperes} - V_{IOUT(Q)}}{V_{IOUT(Q)} - V_{IOUT\_-half\text{-}scale\ amperes}}\right)$$

UVLO ENABLE/DISABLE RELEASE TIME (t_{UVLO})

When a falling V_{CC} reaches V_{UVLOL}, time t_{UVLOE} is required to engage Undervoltage Lockout state. When V_{CC} rises above V_{UVLOH}, time t_{UVLOD} is required to disable UVLO and have a valid output voltage.

FUNCTIONAL DESCRIPTION

Power-On Reset (POR) and Undervoltage Lock-Out (UVLO) Operation

The descriptions in this section assume:

Temperature = 25°C,

$V_{CC} = 5$ V,

no output load, and
no significant current flow through the sensor IC.

Voltage levels shown are specific to a bidirectional ACS770; however, the POR and UVLO functionality described also applies to unidirectional sensors.

The reference numbers section refer to figures 1 and 2.

Power-Up

At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (location [1] in figure 1 and [1′] in figure 2), the POR Release counter starts counting for t_{PORR}. At this point, if V_{CC} exceeds V_{UVLOH} [2′], the output will go to V_{CC} / 2 after t_{UVLOD} [3′]. If V_{CC} does not exceed V_{UVLOH} [2], the output will stay in the high-impedance state until V_{CC} reaches V_{UVLOH} [3] and then will go to V_{CC} / 2 after t_{UVLOD} [4].

V_{CC} drops below V_{CC}(min) = 4.5 V

If V_{CC} drops below V_{UVLOL} [4′, 5], the UVLO Enable Counter starts counting. If V_{CC} is still below V_{UVLOL} when the counter reaches t_{UVLOE}, the UVLO function will be enabled and the ouput will be pulled near GND [6]. If V_{CC} exceeds V_{UVLOL} before the UVLO Enable Counter reaches t_{UVLOE} [5′], the output will continue to be V_{CC} / 2.

Coming Out of UVLO

While UVLO is enabled [6], if V_{CC} exceeds V_{UVLOH} [7], UVLO will be disabled after t_{UVLOD}, and the output will be V_{CC} / 2 [8].

Power-Down

As V_{CC} ramps down below V_{UVLOL} [6′, 9], the UVLO Enable Counter will start counting. If V_{CC} is higher than V_{PORL} when the counter reaches t_{UVLOE}, the UVLO function will be enabled and the output will be pulled near GND [10]. The output will enter a high-impedance state as V_{CC} goes below V_{PORL} [11]. If V_{CC} falls below V_{PORL} before the UVLO Enable Counter reaches t_{UVLOE}, the output will transition directly into a high-impedance state [7′].

EEPROM Error Checking And Correction

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up. If an uncorrectable error has occurred, the VOUT pin will go to high impedance and the device will not respond to applied magnetic field.

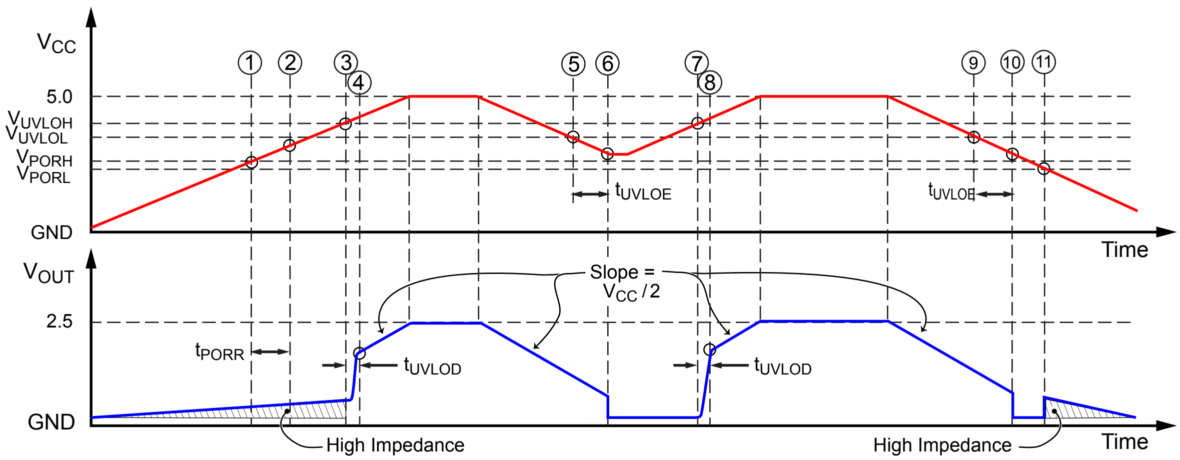


Figure 1: POR and UVLO Operation: Slow Rise Time Case

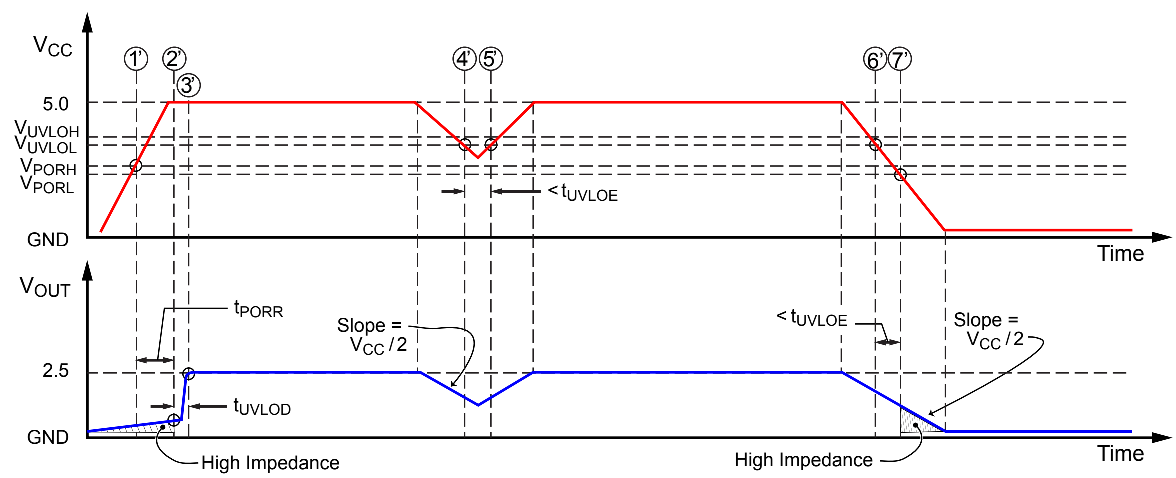


Figure 2: POR and UVLO Operation: Fast Rise Time Case

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. Allegro employs a technique to remove key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed.

In addition to the removal of the thermal and stress related offset, this novel technique also reduces the amount of thermal noise in the Hall sensor IC while completely removing the modulated residue resulting from the chopper operation. The chopper stabilization technique uses a high-frequency sampling clock. For demodulation process, a sample-and-hold technique is used. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

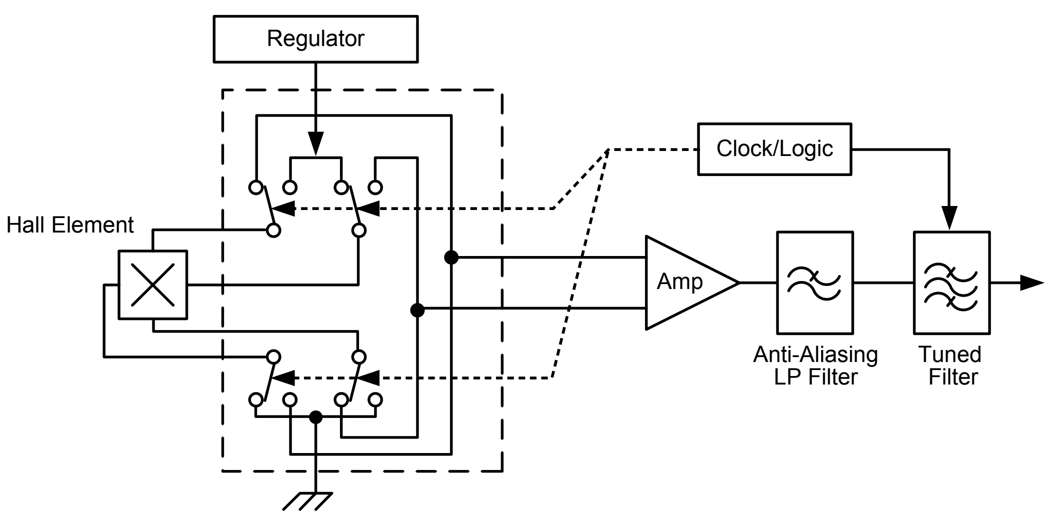
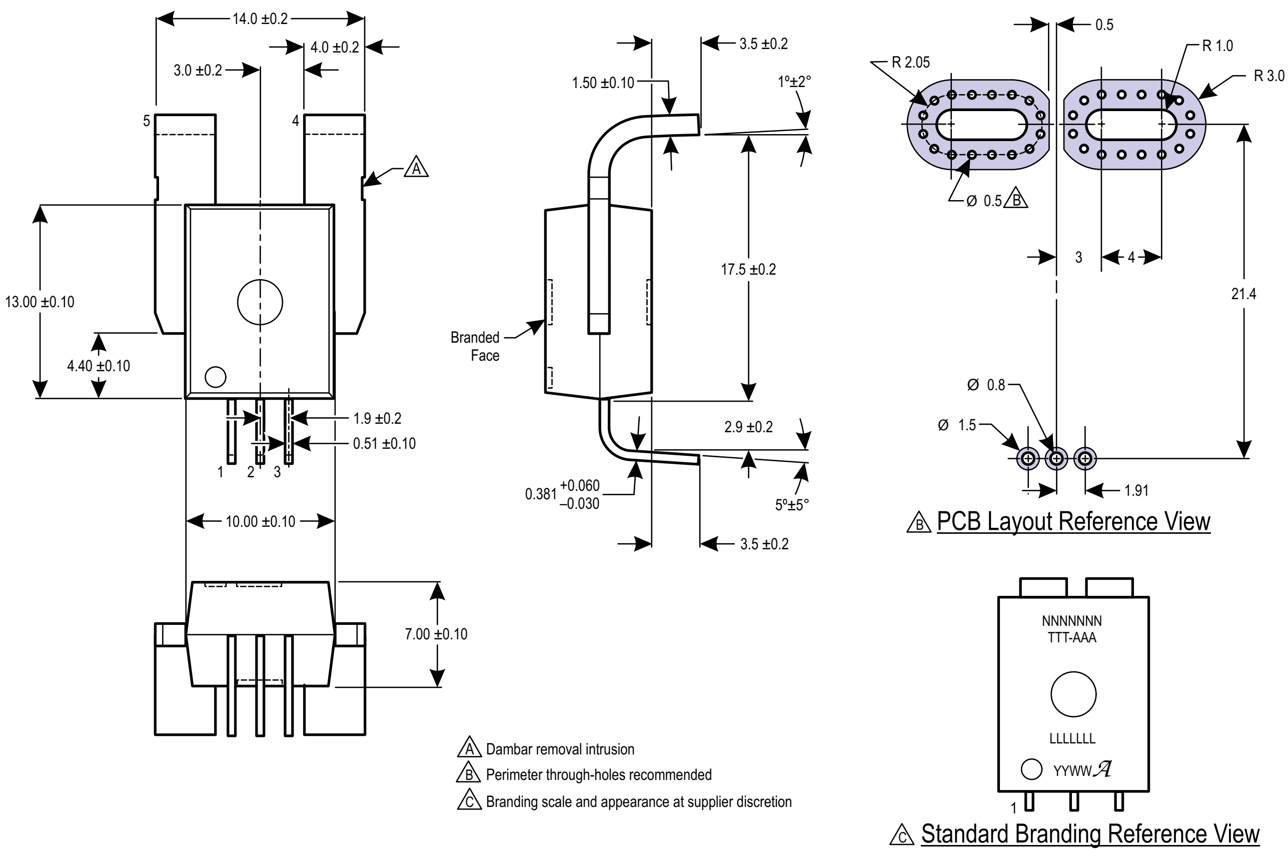


Figure 3: Concept of Chopper Stabilization Technique

PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

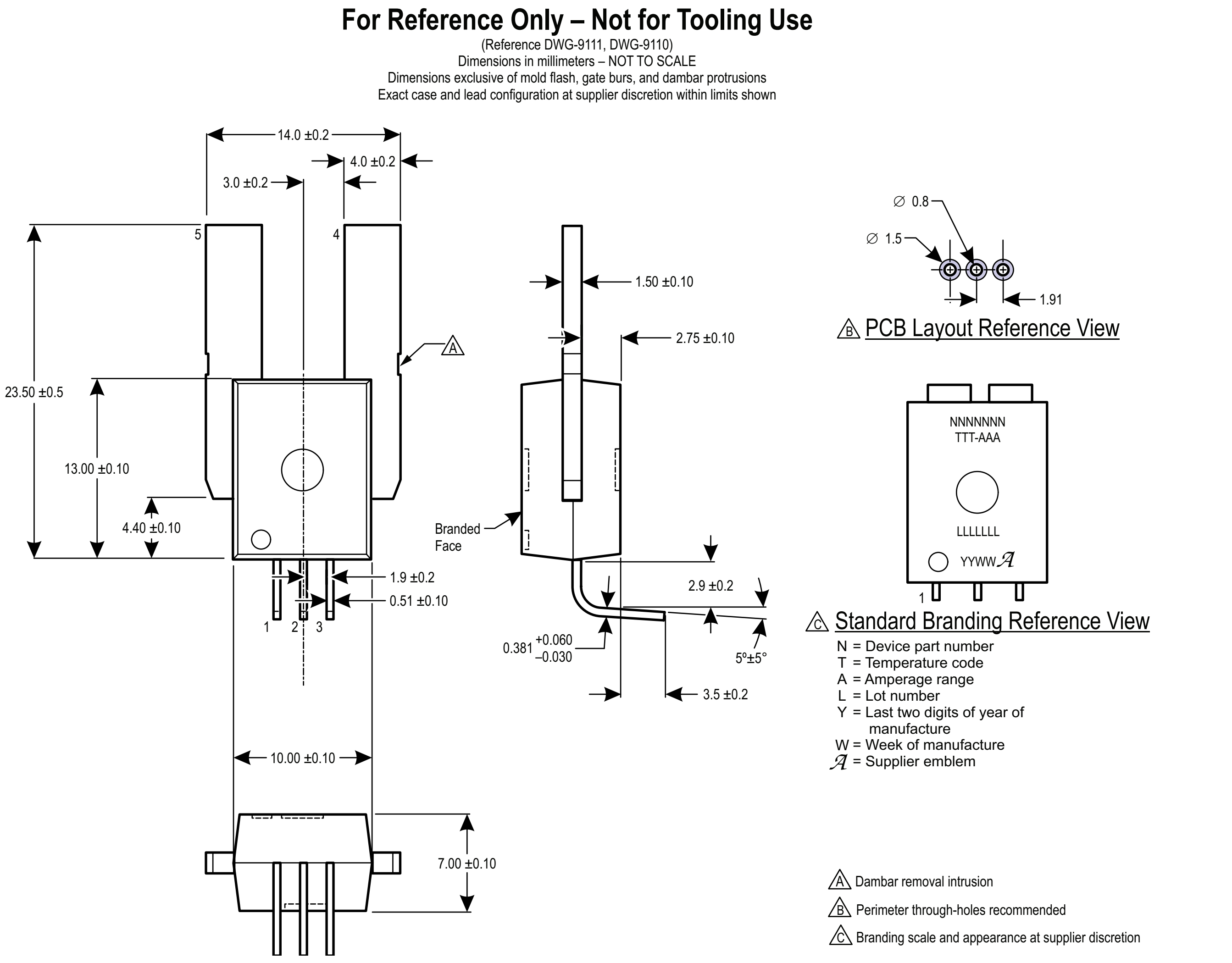
(Reference DWG-9111 & DWG-9110)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



N = Device part number
T = Temperature code
A = Amperage range
L = Lot number
Y = Last two digits of year of manufacture
W = Week of manufacture
𝒜 = Supplier emblem

Creepage distance, current terminals to signal pins: 7.25 mm
Clearance distance, current terminals to signal pins: 7.25 mm
Package mass: 4.63 g typical

Figure 4: Package CB, 5-Pin, Leadform PFF

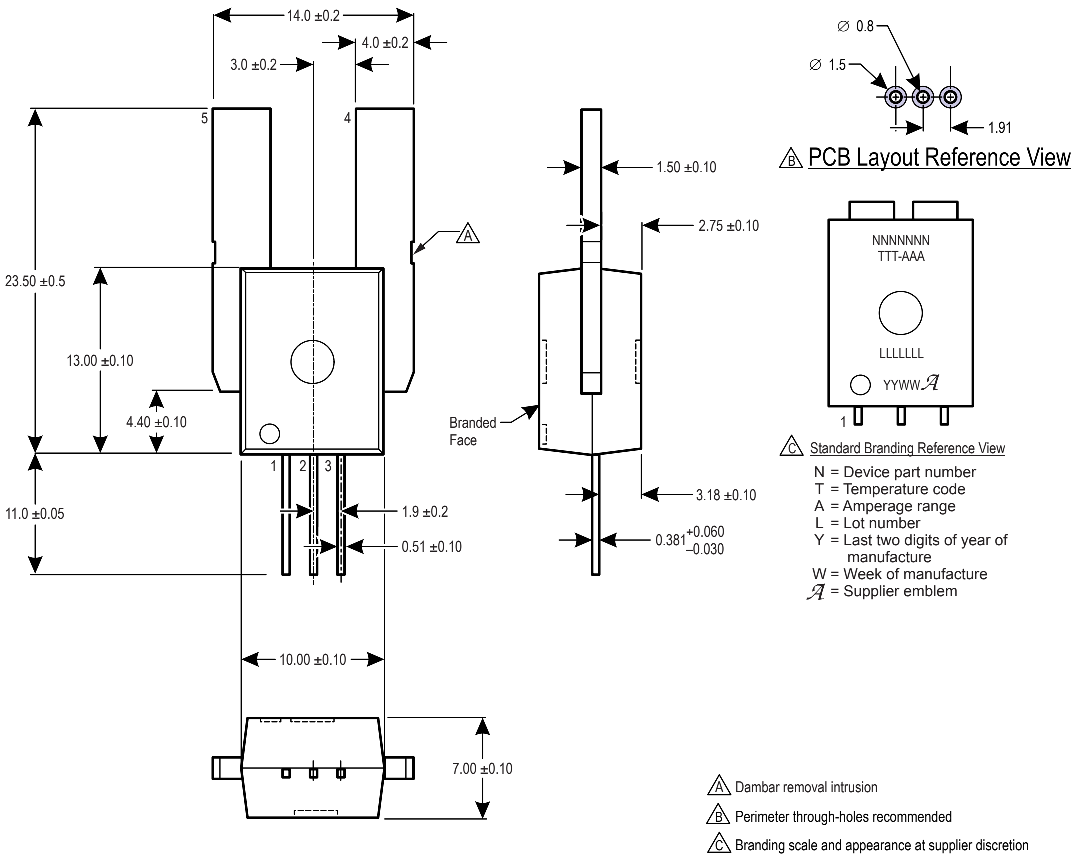


Creepage distance, current terminals to signal pins: 7.25 mm
Clearance distance, current terminals to signal pins: 7.25 mm
Package mass: 4.63 g typical

Figure 5: Package CB, 5-Pin, Leadform PSF

For Reference Only – Not for Tooling Use

(Reference DWG-9111, DWG-9110)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Creepage distance, current terminals to signal pins: 7.25 mm
Clearance distance, current terminals to signal pins: 7.25 mm
Package mass: 4.63 g typical

Figure 6: Package CB, 5-Pin, Leadform PSS

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Revision History

Number	Date	Description
1	December 8, 2014	Revised Selection Guide
2	January 20, 2015	Revised V_{PORH} Typical Value
3	March 11, 2015	Revised V_{RCC}, V_{RIOUT}, $I_{OUT(Source)}$, I_{ERROM} (100 A and 150 A) values, and added Symmetry to X150B PERFORMANCE CHARACTERISTICS table
4	April 8, 2015	Updated TUV certification
5	November 2, 2016	Updated PCB Layout Reference View in Package Outline Drawing on page 27
6	June 5, 2017	Updated status of ACS770LCB-100U-PSF-T part variant to Last-Time Buy
7	November 16, 2017	Added PSS leadform
8	January 30, 2018	Added Dielectric Surge Strength Test Voltage characteristic (page 3) and EEPROM Error Checking and Correction section (page 24)