

IRFP17N50LS

SMPS MOSFET

HEXFET® Power MOSFET

Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- ZVS and High Frequency Circuit
- PWM Inverters

V_{DSS}	$R_{DS(on)}$ typ.	T_{rr}	I_D
500V	0.28Ω	170ns	16A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low T_{rr} and Soft Diode Recovery
- High Performance Optimised Anti-parallel Diode



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	16	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	11	
I_{DM}	Pulsed Drain Current ①	64	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	220	W
	Linear Derating Factor	1.8	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	13	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 screw	10	
			lbft.in(N.m)

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	16	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	64		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}$, $I_S = 16\text{A}$, $V_{GS} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	170	250	ns	$T_J = 25^\circ\text{C}$ $I_F = 16\text{A}$ $T_J = 125^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ④
Q_{rr}	Reverse Recovery Charge	—	470	710		
		—	810	1210	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	7.3	11	A	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Typical SMPS Topologies

- Bridge Converters
- All Zero Voltage Switching

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.6	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.28	0.32	Ω	$V_{GS} = 10V, I_D = 9.9A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	11	—	—	S	$V_{DS} = 50V, I_D = 9.9A$
Q_g	Total Gate Charge	—	—	130	nC	$I_D = 16A$
Q_{gs}	Gate-to-Source Charge	—	—	33		$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	59		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	21	—	ns	$V_{DD} = 250V$
t_r	Rise Time	—	51	—		$I_D = 16A$
$t_{d(off)}$	Turn-Off Delay Time	—	50	—		$R_G = 7.5\Omega$
t_f	Fall Time	—	28	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	2760	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	325	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	37	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	3690	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	84	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	159	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	390	mJ
I_{AR}	Avalanche Current①	—	16	A
E_{AR}	Repetitive Avalanche Energy①	—	22	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.56	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 3.0mH$, $R_G = 25\Omega$, $I_{AS} = 16A$.
- ③ $I_{SD} \leq 16A$, $di/dt \leq 347A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

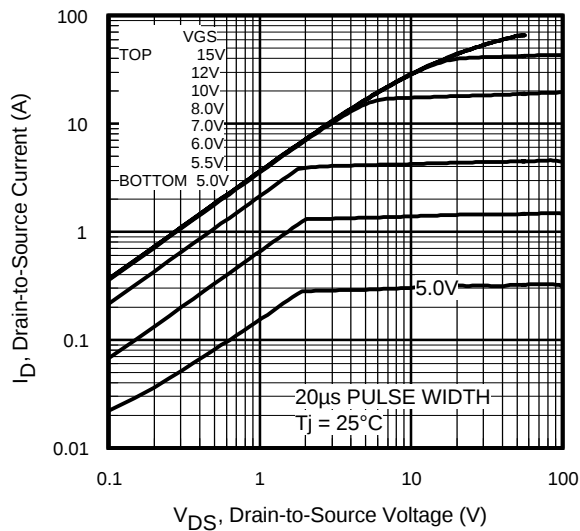


Fig 1. Typical Output Characteristics

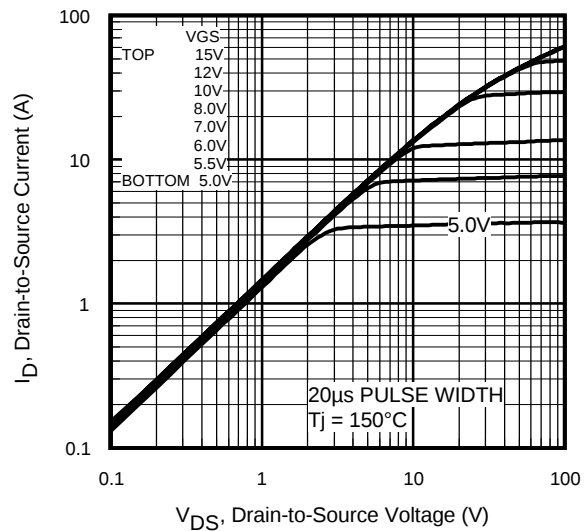


Fig 2. Typical Output Characteristics

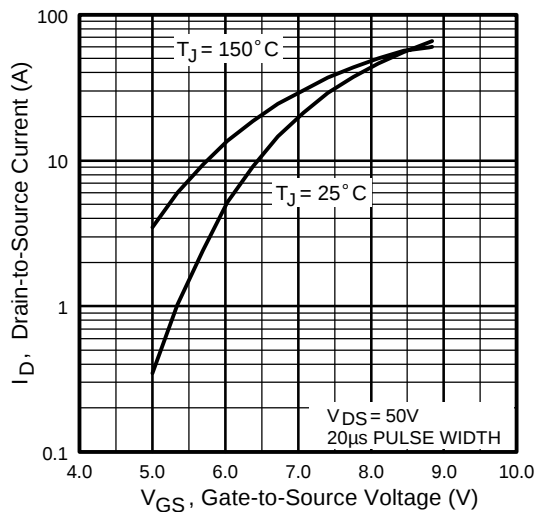


Fig 3. Typical Transfer Characteristics

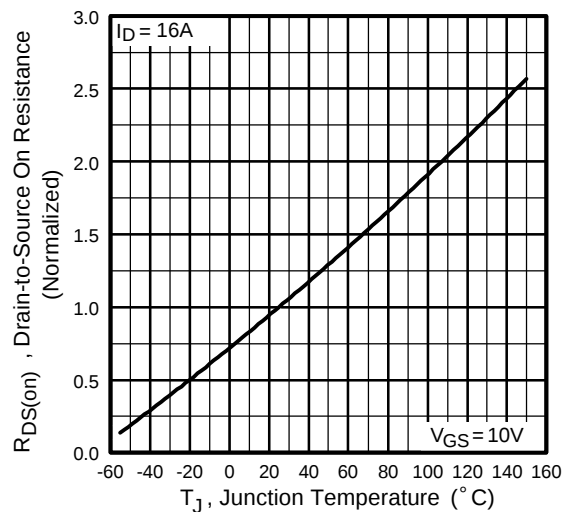


Fig 4. Normalized On-Resistance Vs. Temperature

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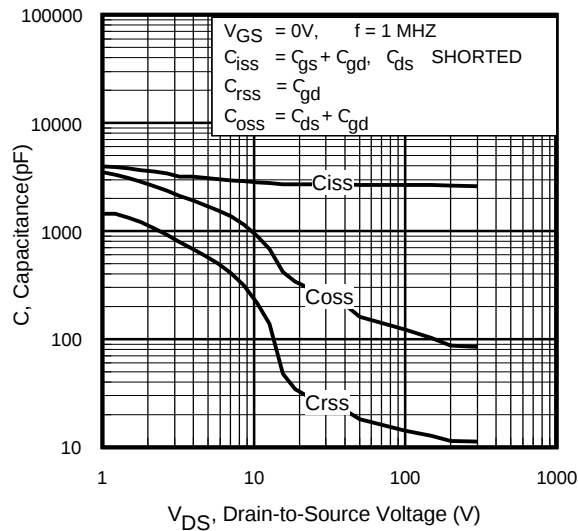


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

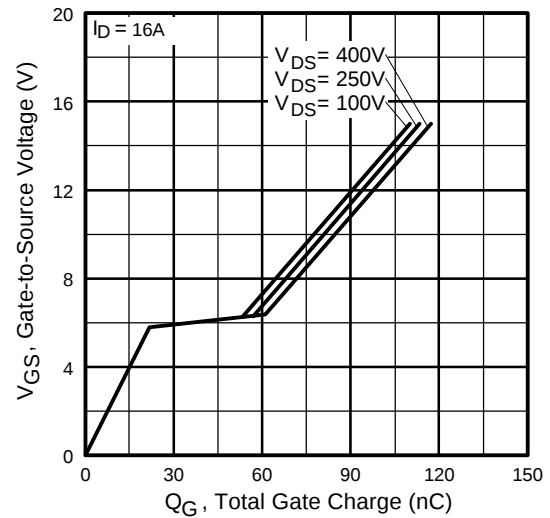


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

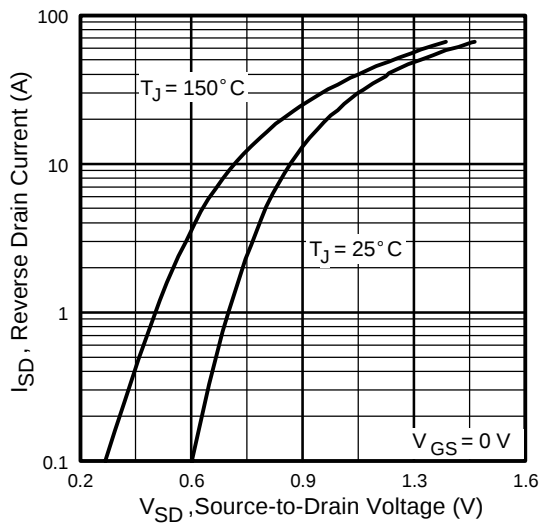


Fig 7. Typical Source-Drain Diode Forward Voltage

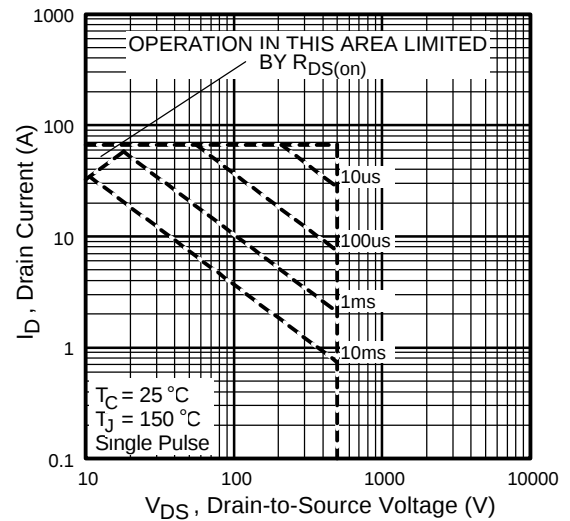


Fig 8. Maximum Safe Operating Area

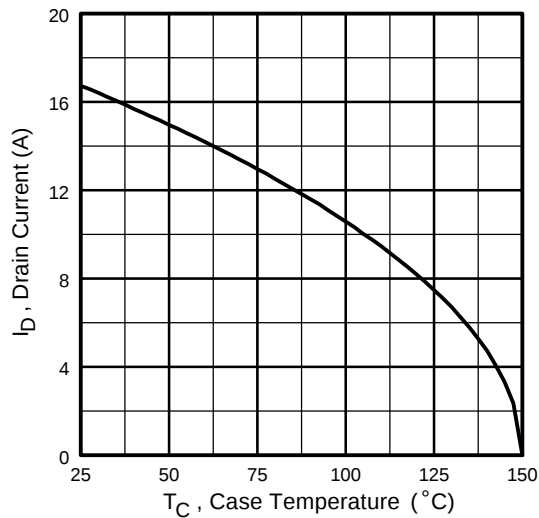


Fig 9. Maximum Drain Current Vs. Case Temperature

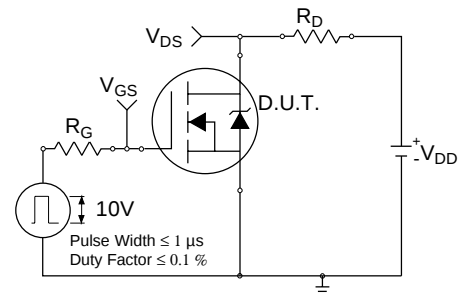


Fig 10a. Switching Time Test Circuit

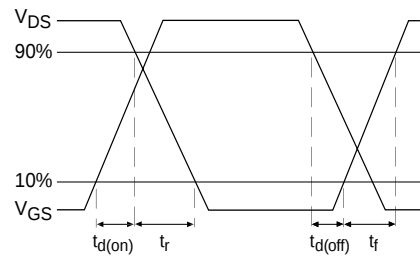


Fig 10b. Switching Time Waveforms

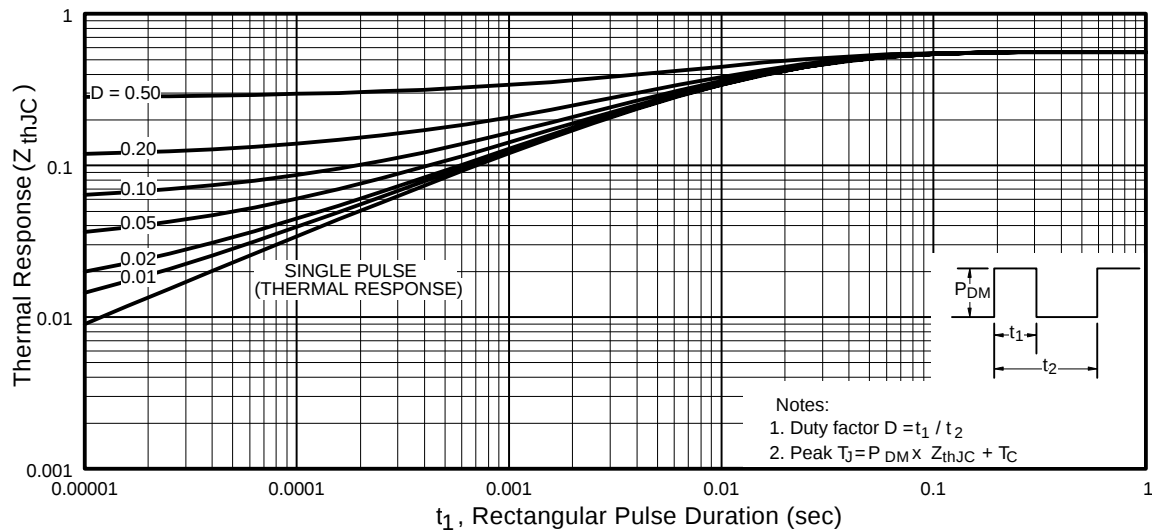


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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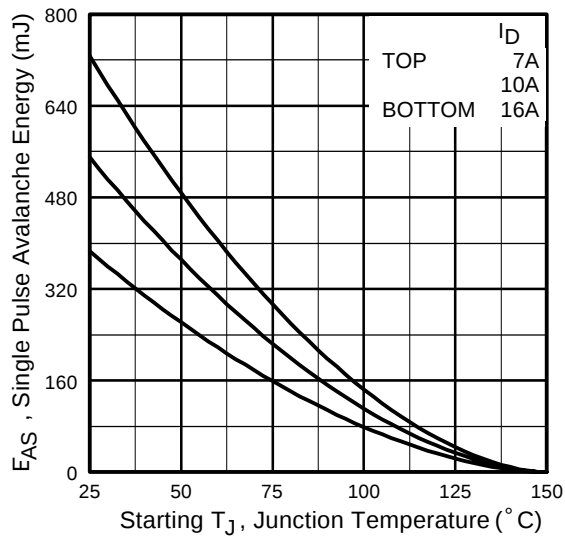


Fig 12a. Maximum Avalanche Energy Vs. Drain Current

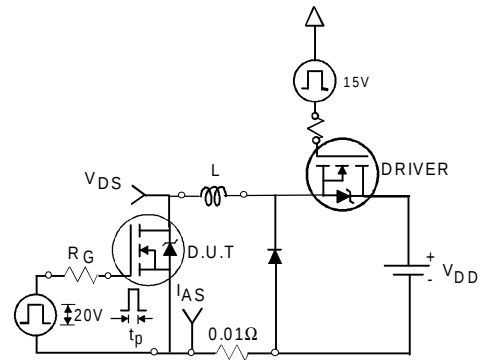


Fig 12c. Unclamped Inductive Test Circuit

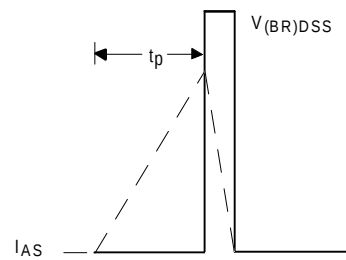


Fig 12d. Unclamped Inductive Waveforms

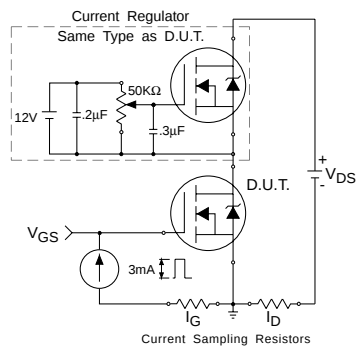


Fig 13a. Gate Charge Test Circuit

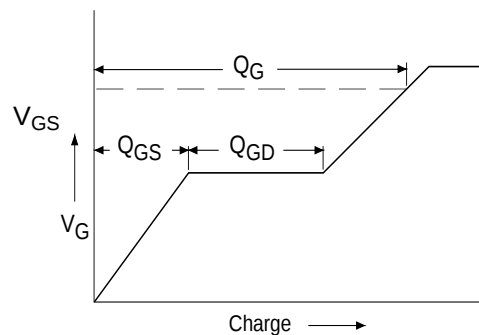
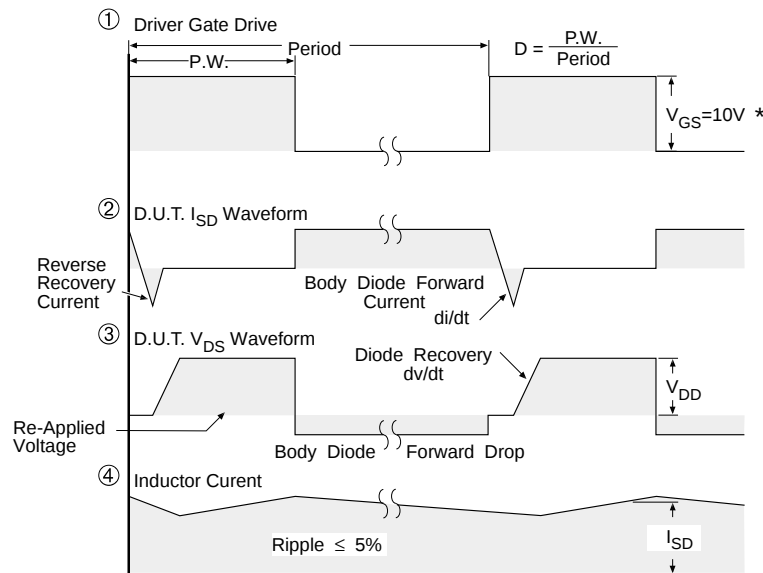
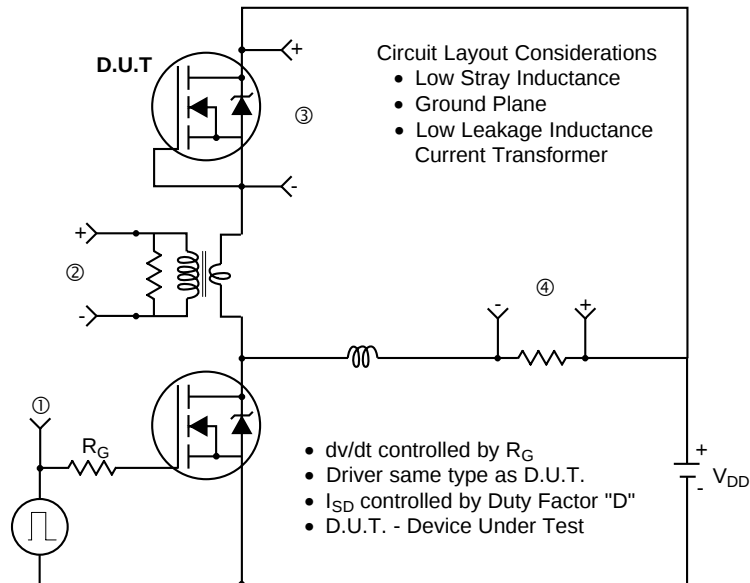


Fig 13b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



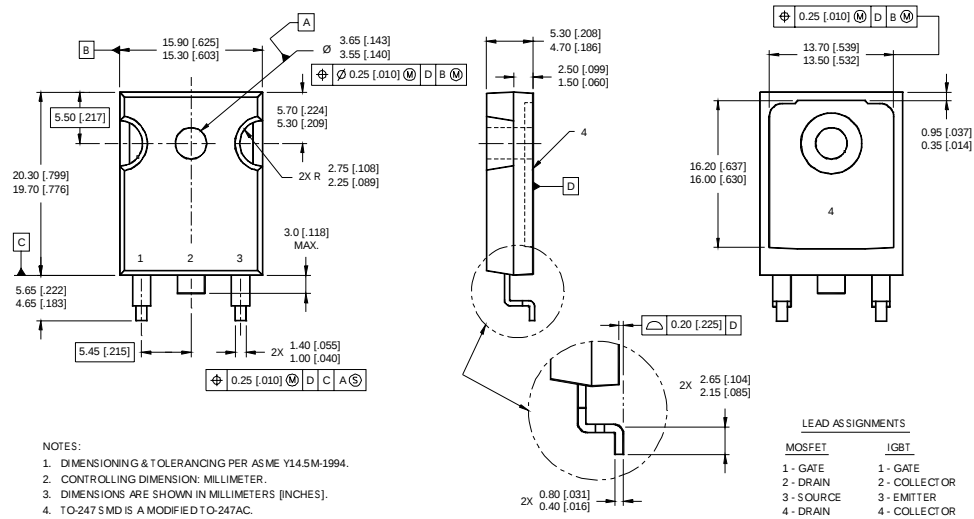
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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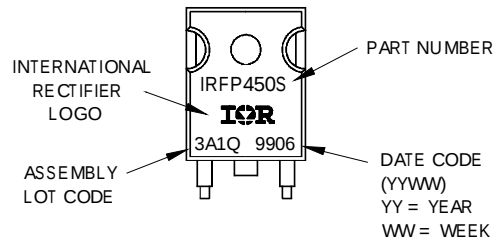
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SMD-247 Package Outline



SMD-247 Part Marking Information

EXAMPLE: THIS IS AN IRFP450S WITH
ASSEMBLY LOT CODE 3A1Q



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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