features

- **Multi-Rate Operation from 155 Mbps Up to 2.5 Gbps**
- **Ultralow Power Consumption**
- **Input Offset Cancellation**
- **High Input Dynamic Range**
- **Output Disable**
- **Output Polarity Select**
- **CML Data Outputs**
- **Single 3.3-V Supply**
- **Surface Mount Small Footprint 3 mm × 3 mm 16-Pin QFN Package**

applications

- **SONET/SDH Transmission Systems at OC3, OC12, OC24, OC48**
- **1.0625-Gbps and 2.125-Gbps Fibre Channel Receivers**
- **Gigabit Ethernet Receivers**

description

The ONET2511PA is a versatile high-speed limiting amplifier for multiple fiber optic applications with data rates up to 2.5 Gbps.

This device provides a gain of about 50 dB, which ensures a fully differential output swing for input signals as low as 3 mV_{p-p}.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1800 mV_{p-p}.

The ONET2511PA is available in a small footprint 3 mm × 3 mm 16-pin QFN package. The circuit requires a single 3.3-V supply.

This power efficient limiting amplifier is characterized for operation from –40°C to 85°C.

available options

T_A	PACKAGED DEVICE	FEATURES
−40°C to 85°C	ONET2511PARGT	16-pin 3 mm x 3 mm QFN, tube
−40°C to 85°C	ONET2511PARGTR	16-pin 3 mm x 3 mm QFN, tape and reel

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block diagram

A simplified block diagram of the ONET2511PA is shown in Figure 1.

This compact, low power 2.5-Gbps limiting amplifier consists of a high-speed data path with offset cancellation block, a loss of signal and RSSI detection block, and a bandgap voltage reference and bias current generation block.

The limiting amplifier requires a single 3.3-V supply voltage. All circuit parts are described in detail below.

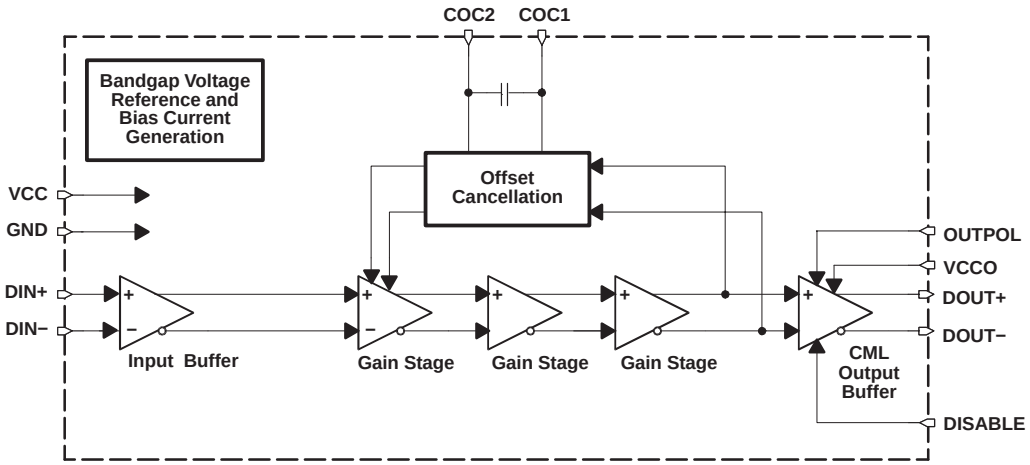

Figure 1. Block Diagram

high-speed data path

The high-speed data signal is applied to the data path by means of the input signal pins DIN+/DIN–. The data path consists of the input stage with $2 \times 50\text{-}\Omega$ on-chip line termination to VCC, three gain stages which provide the required typical gain of about 50 dB, and a CML output stage. The amplified data output signal is available at the output pins DOUT+/DOUT–, which provide $2 \times 50\text{-}\Omega$ back-termination to VCCO. The output stage also includes a data polarity switching function, which is controlled by the OUTPOL input and a disable function, controlled by the signal applied to the DISABLE input pin.

An offset cancellation compensates inevitable internal offset voltages and thus ensures proper operation even for small input data signals.

The low frequency cutoff is as low as 45 kHz with the built-in filter capacitor.

For applications, which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1/COC2 pins.

bandgap voltage and bias generation

The ONET2511PA limiting amplifier is supplied by a single 3.3-V ±10% supply voltage connected to the VCC and VCCO pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuitry generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

package

For the ONET2511PA a small footprint 3 mm × 3 mm 16-pin QFN package is used, with a lead pitch of 0,5 mm. The pinout is shown in Figure 2.

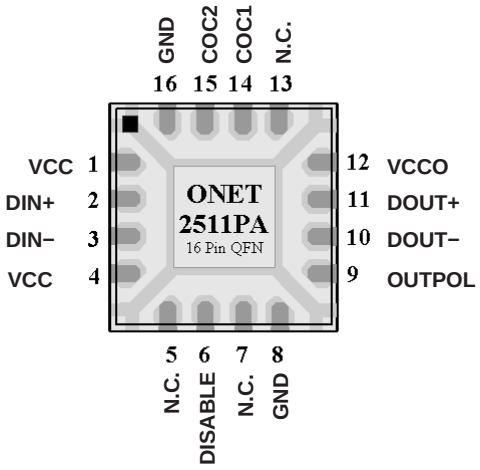

Figure 2. Pinout of ONET2511PA in a 3 mm × 3 mm 16-Pin QFN Package

terminal functions

The following table shows a pin description for the ONET2511PA in a 3 mm x 3 mm 16-pin QFN package.

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
VCC	1, 4	Supply	3.3-V ±10% supply voltage
DIN+	2	Analog in	Noninverted data input. On-chip 50-Ω terminated to VCC
DIN–	3	Analog in	Inverted data input. On-chip 50-Ω terminated to VCC
N.C.	5, 7, 13		Not connected
DISABLE	6	CMOS in	Disables CML output stage when set to high level
GND	8, 16, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
OUTPOL	9	CMOS in	Output data signal polarity select (internally pulled up): Setting to high level or leaving pin open selects normal polarity. Low level selects inverted polarity.
DOUT–	10	CML out	Inverted data output. On-chip 50-Ω back-terminated to VCCO
DOUT+	11	CML out	Noninverted data output. On-chip 50-Ω back-terminated to VCCO
VCCO	12	Supply	3.3-V ±10% supply voltage for output stage
COC1	14	Analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
COC2	15	Analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).

absolute maximum ratings

over operating free-air temperature range unless otherwise noted†

		VALUE	UNIT
V_{CC}, V_{CCO}	Supply voltage, See Note 1	–0.3 to 4	V
V_{DIN+}, V_{DIN-}	Voltage at DIN+, DIN–, See Note 1	0.5 to 4	V
$V_{DISABLE}$, V_{OUTPOL}, V_{DOUT+}, V_{DOUT-}, V_{COC1}, V_{COC2}	Voltage at TH, DISABLE, OUTPOL, DOUT+, DOUT–, COC1, and COC2, See Note 1	–0.3 to 4	V
V_{COC_DIFF}	Differential voltage between COC1 and COC2	±1	V
V_{DIN_DIFF}	Differential voltage between DIN+ and DIN–	±2.5	V
I_{DIN+}, I_{DIN-}, I_{DOUT+}, I_{DOUT-}	Continuous current at inputs and outputs	–25 to 25	mA
ESD	ESD rating at all pins except VCCO	3	kV (HBM)
	ESD rating at VCCO	1.1	
$T_{J(max)}$	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	−65 to 85	°C
T_A	Characterized free-air operating temperature range	−40 to 85	°C
T_L	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}, V_{CCO}	3	3.3	3.6	V
Operating free-air temperature, T_A	−40		85	°C

dc electrical characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}, V_{CCO}	Supply voltage		3	3.3	3.6	V
I_{VCC}	Supply current	DISABLE = low (excludes CML output current)		22	28	mA
V_{OD}	Differential data output voltage swing	DISABLE = high		0.25	10	mV_{p-p}
		DISABLE = low	600	780	1200	mV_{p-p}
R_{IN}, R_{OUT}	Data input/output resistance	Single ended		50		Ω
$V_{IN,MIN}$	Data input sensitivity	BER < 10^{-10}		3	5	mV_{p-p}
$V_{IN,MAX}$	Data input overload		1800			mV_{p-p}
	CMOS input high voltage		2.1			V
	CMOS input low voltage				0.6	V

ac electrical characteristics

over recommended operating conditions (unless otherwise noted), typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low frequency −3-dB bandwidth	C_{OC} = open		45	70	kHz
		C_{OC} = 2.2 nF		0.8		
	Data rate		2.5			Gb/s
v_{NI}	Input referred noise				300	μV_{RMS}
DJ	Deterministic jitter, See Note 2	K28.5 pattern at 2.5 Gbps		8.5	25	ps_{p-p}
		2^{23}−1 PRBS equivalent pattern at 2.5 Gbps		9.3	30	
		2^{23}−1 PRBS equivalent pattern at 155 Mbps		25	50	
RJ	Random jitter	Input = 5 mVpp		6.5		ps_{RMS}
		Input = 10 mVpp		3		
t_r	Output rise time	20% to 80%		60	85	ps
t_f	Output fall time	20% to 80%		60	85	ps
PSNR	Power supply noise rejection	f < 2 MHz	26			dB
t_{DIS}	Disable response time			20		ns

NOTE 2: Deterministic jitter does not include pulse-width distortion due to residual small output offset voltage.

APPLICATION INFORMATION

Figure 3 shows the ONET2511PA connected with an ac-coupled interface to the data signal source as well as to the output load.

The ac-coupling capacitors C_1 through C_4 in the input and output data signal lines are the only required external components. In addition, an optional external filter capacitor (C_{OC}) may be used if a low cutoff frequency is desired.

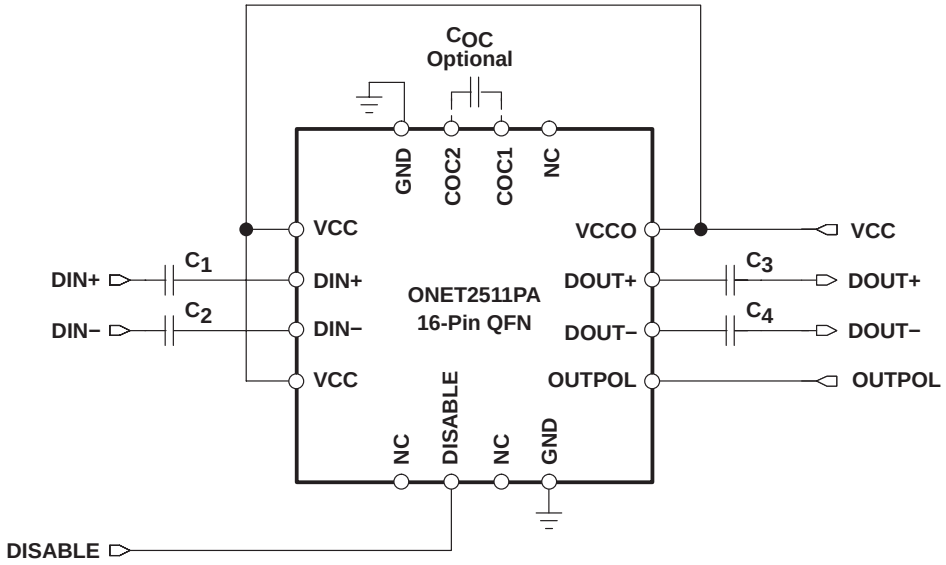

Figure 3. Basic Application Circuit With AC-Coupled I/Os

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = V_{CCO} = +3.3 V and T_A = 25°C (unless otherwise noted)

DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

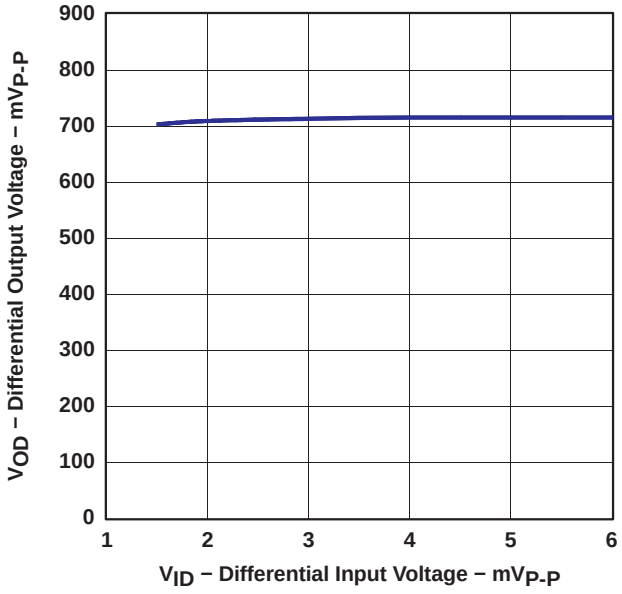

Figure 4

RANDOM JITTER vs DIFFERENTIAL INPUT VOLTAGE

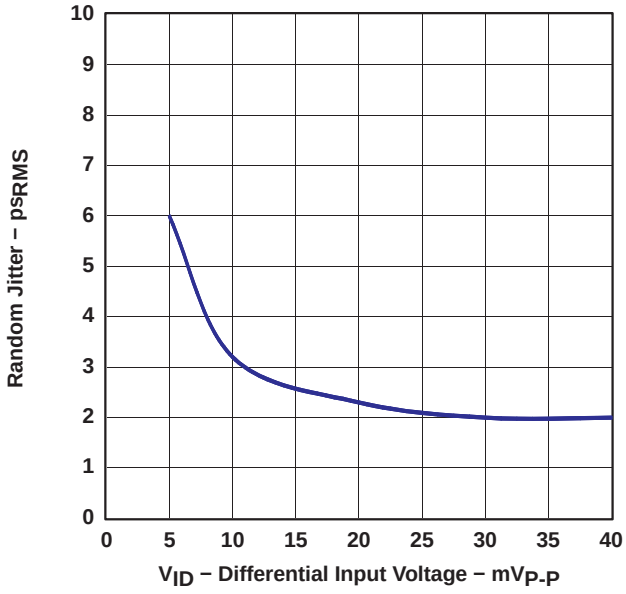

Figure 5

BIT ERROR RATIO vs DIFFERENTIAL INPUT VOLTAGE

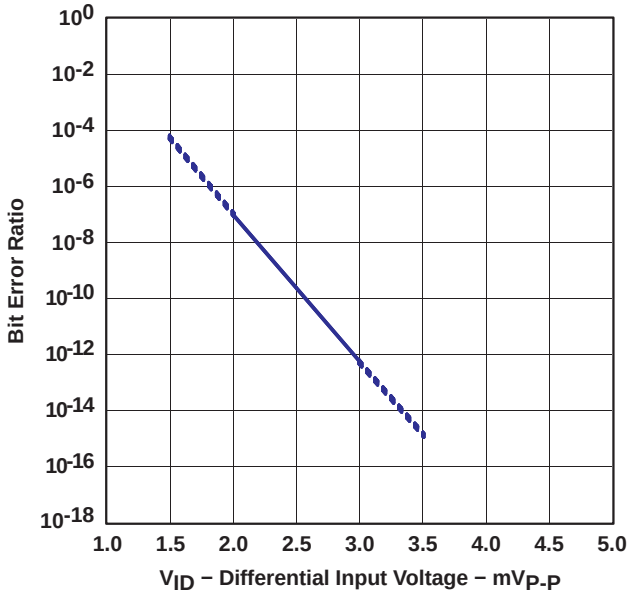

Figure 6

OUTPUT EYE-DIAGRAM AT 2.5 GBPS AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})

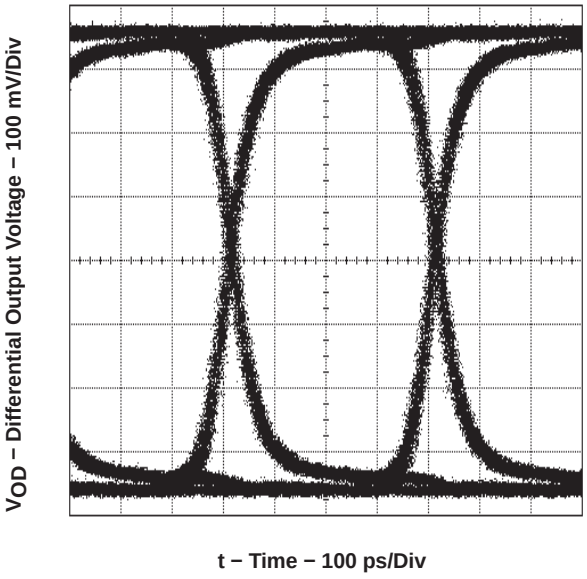

Figure 7

OUTPUT EYE-DIAGRAM AT 2.5 GBPS AND MAXIMUM INPUT VOLTAGE (1800 mV_{p-p})

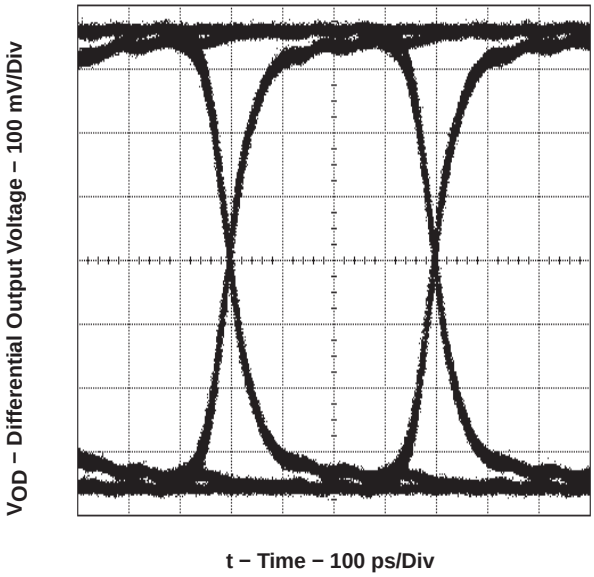

Figure 8

DIFFERENTIAL INPUT RETURN GAIN vs FREQUENCY

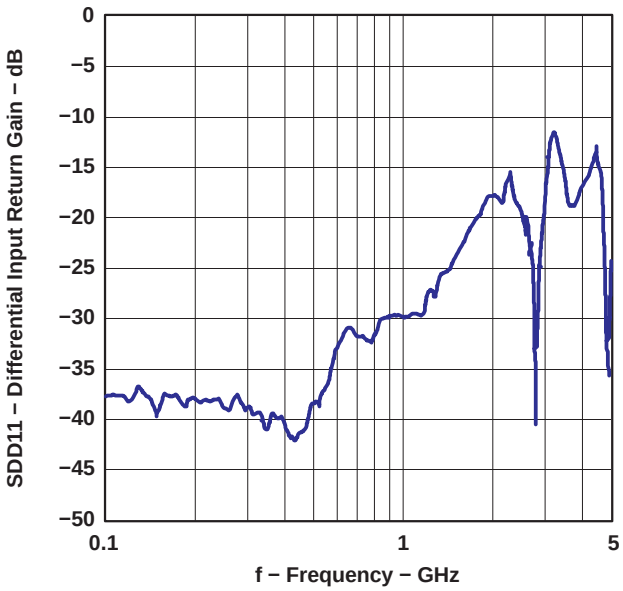

Figure 9

DIFFERENTIAL OUTPUT RETURN GAIN vs FREQUENCY

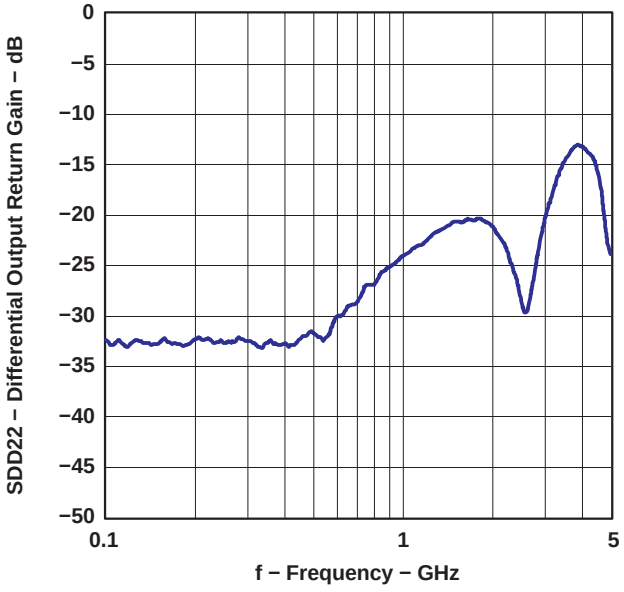

Figure 10

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