BLF871; BLF871S

UHF power LDMOS transistor

Rev. 04 — 19 November 2009 Product data sheet

1. Product profile

1.1 General description

A 100 W LDMOS RF power transistor for broadcast transmitter applications and industrial applications. The transistor can deliver 100 W broadband from HF to 1 GHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital transmitter applications.

Table 1. Typical performance

RF performance at V_{DS} = 40 V in a common-source 860 MHz test circuit.

Mode of operation	f (MHz)	P_L (W)	$P_{L(PEP)}$ (W)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)	PAR (dB)
CW, class AB	860	100	-	-	21	60	-	-
2-tone, class AB	f_1 = 860; f_2 = 860.1	-	100	-	21	47	–35	-
DVB-T (8k OFDM)	858	-	-	24	22	33	–34[1]	8.3[2]

[1] Measured [dBc] with delta marker at 4.3 MHz from center frequency.

[2] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- 2-tone performance at 860 MHz, a drain-source voltage V_{DS} of 40 V and a quiescent drain current I_{Dq} = 0.5 A:
  - Peak envelope power load power = 100 W
  - Power gain = 21 dB
  - Drain efficiency = 47 %
  - Third order intermodulation distortion = –35 dBc
- DVB performance at 858 MHz, a drain-source voltage V_{DS} of 40 V and a quiescent drain current I_{Dq} = 0.5 A:
  - Average output power = 24 W
  - Power gain = 22 dB
  - Drain efficiency = 33 %
  - Third order intermodulation distortion = –34 dBc (4.3 MHz from center frequency)

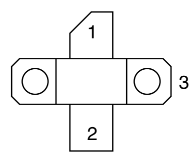
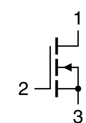
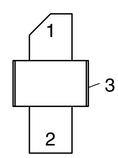
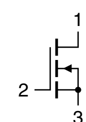
- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Communication transmitter applications in the UHF band
- Industrial applications in the UHF band

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF871 (SOT467C)			
1	drain		 sym112
2	gate		
3	source [1]		
BLF871S (SOT467B)			
1	drain		 sym112
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF871	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT467C
BLF871S	-	earless LDMOST ceramic package; 2 leads	SOT467B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	89	V
V_{GS}	gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; $P_{L(AV)}$ = 50 W	[1]	0.95	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

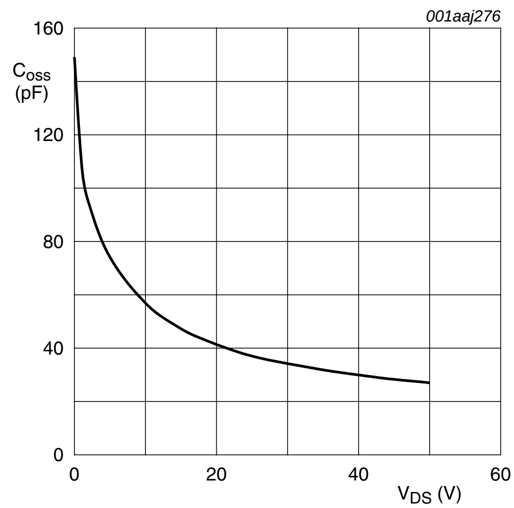
6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.12 mA	[1]	89	-	105.5	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 112 mA	[1]	1.4	-	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 40 V		-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V		16.7	20	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V		-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.7 A	[1]	-	210	-	mΩ
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 40 V; f = 1 MHz		-	95	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 40 V; f = 1 MHz		-	30	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 40 V; f = 1 MHz		-	1	-	pF

[1] I_D is the drain current.



V_{GS} = 0 V; f = 1 MHz.

Fig 1. Output capacitance as a function of drain-source voltage; typical values

7. Application information

Table 7. RF performance in a common-source narrowband 860 MHz test circuit

T_h = 25 °C unless otherwise specified.

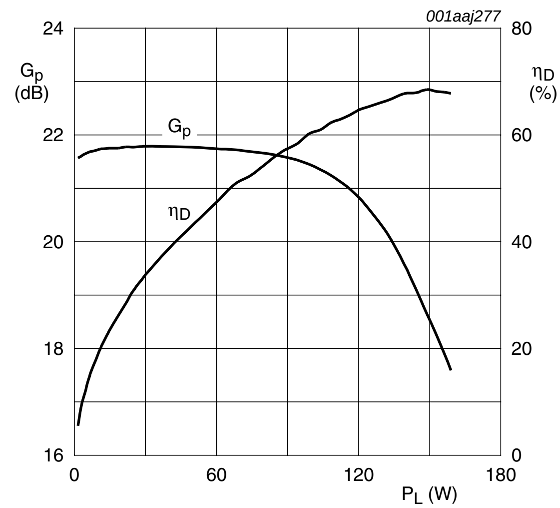
Mode of operation	f (MHz)	V_{DS} (V)	I_{Dq} (A)	$P_{L(PEP)}$ (W)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)	PAR (dB)
2-tone, class AB	f_1 = 860; f_2 = 860.1	40	0.5	100	-	> 19	> 44	< −30	-
DVB-T (8k OFDM)	858	40	0.5	-	24	> 19	> 30	< −31 [1]	> 7.8 [2]

[1] Measured [dBc] with delta marker at 4.3 MHz from center frequency.

[2] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

7.1 Narrowband RF figures

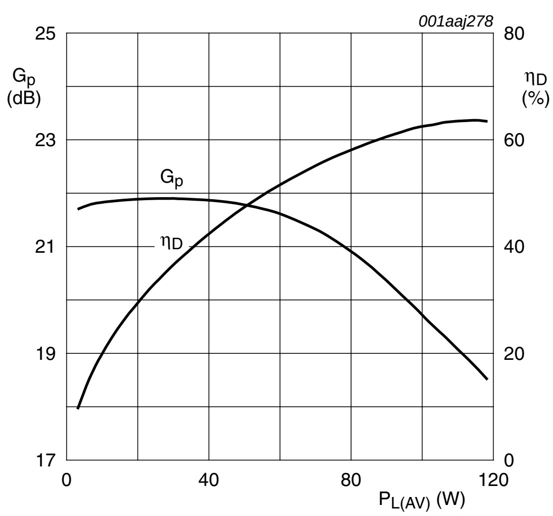
7.1.1 CW



V_{DS} = 40 V; I_{Dq} = 0.5 A; measured in a common source narrowband 860 MHz test circuit.

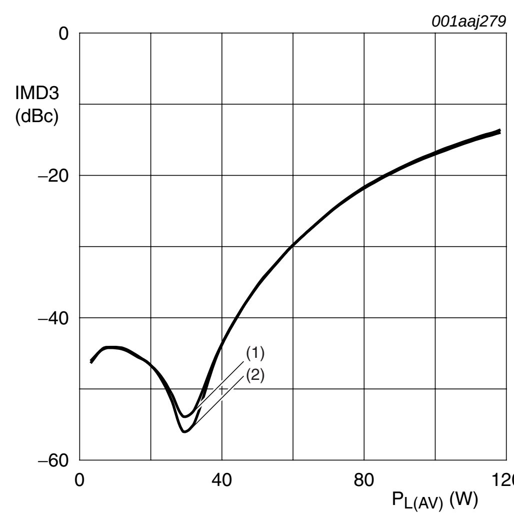
Fig 2. CW power gain and drain efficiency as a function of load power; typical values

7.1.2 2-Tone



V_{DS} = 40 V; I_{Dq} = 0.5 A; measured in a common source narrowband 860 MHz test circuit.

Fig 3. 2-Tone power gain and drain efficiency as functions of average load power; typical values



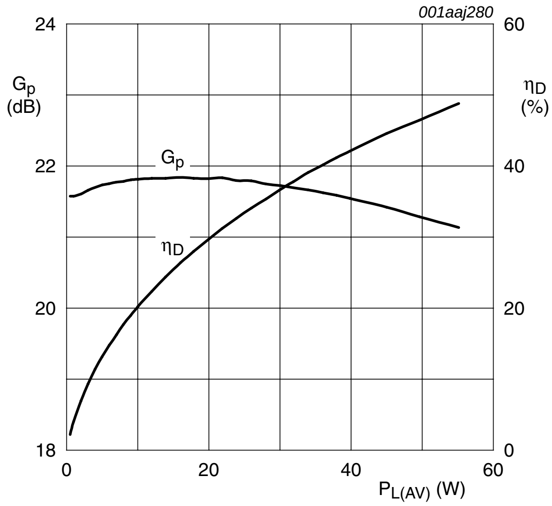
V_{DS} = 40 V; I_{Dq} = 0.5 A; measured in a common source narrowband 860 MHz test circuit.

(1) Low frequency component

(2) High frequency component

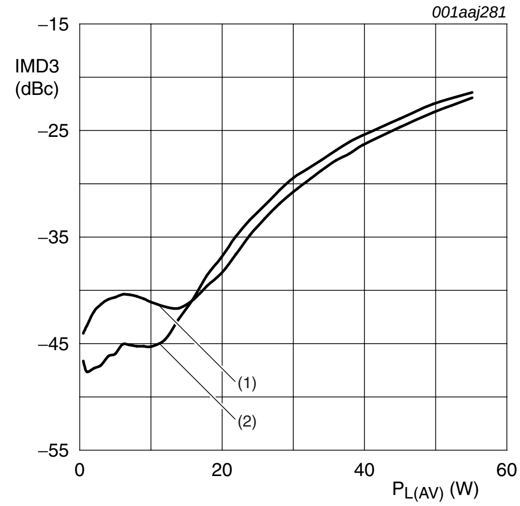
Fig 4. 2-Tone third order intermodulation distortion as a function of average load power; typical values

7.1.3 DVB-T



V_{DS} = 40 V; I_{Dq} = 0.5 A; measured in a common source narrowband 860 MHz test circuit.

Fig 5. DVB-T power gain and drain efficiency as functions of average load power; typical values



V_{DS} = 40 V; I_{Dq} = 0.5 A; measured in a common source narrowband 860 MHz test circuit.

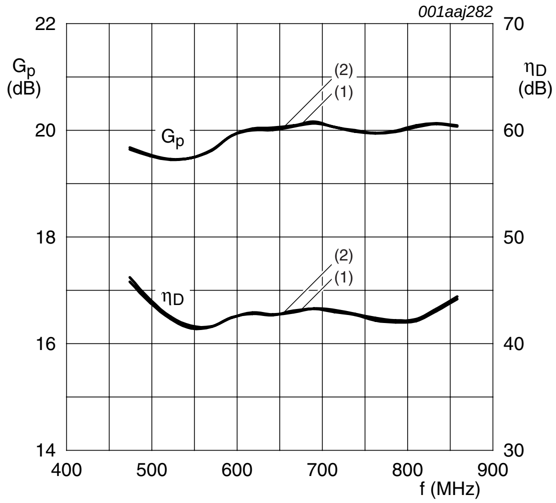
(1) Low frequency component

(2) High frequency component

Fig 6. DVB-T third order intermodulation distortion as a function of average load power; typical values

7.2 Broadband RF figures

7.2.1 2-Tone

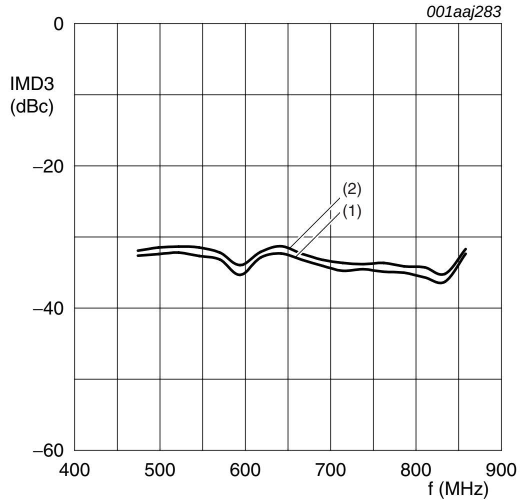


I_{Dq} = 0.5 A; measured in a common source broadband test circuit as described in Section 8.

(1) V_{DS} = 40 V; $P_{L(AV)}$ = 45 W

(2) V_{DS} = 42 V; $P_{L(AV)}$ = 50 W

Fig 7. 2-Tone power gain and drain efficiency as a function of frequency; typical values



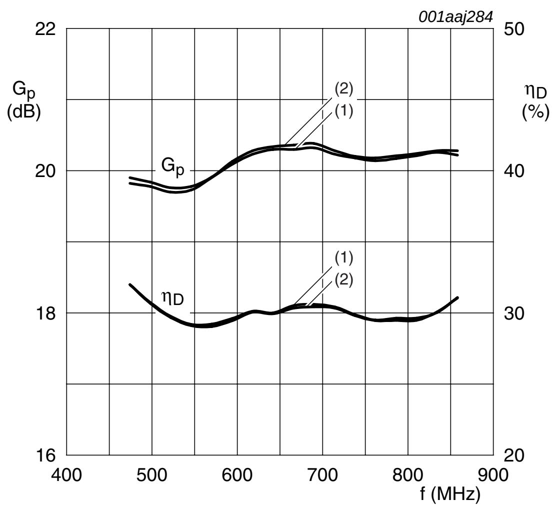
I_{Dq} = 0.5 A; measured in a common source broadband test circuit as described in Section 8.

(1) V_{DS} = 40 V; $P_{L(AV)}$ = 45 W

(2) V_{DS} = 42 V; $P_{L(AV)}$ = 50 W

Fig 8. 2-Tone third order intermodulation distortion as a function of frequency; typical values

7.2.2 DVB-T

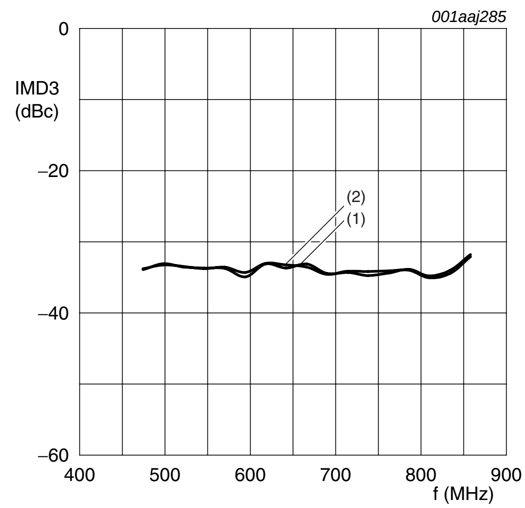


I_{Dq} = 0.5 A; measured in a common source broadband test circuit as described in Section 8.

(1) V_{DS} = 40 V; $P_{L(AV)}$ = 22 W

(2) V_{DS} = 42 V; $P_{L(AV)}$ = 24 W

Fig 9. DVB-T power gain and drain efficiency as functions of frequency; typical values

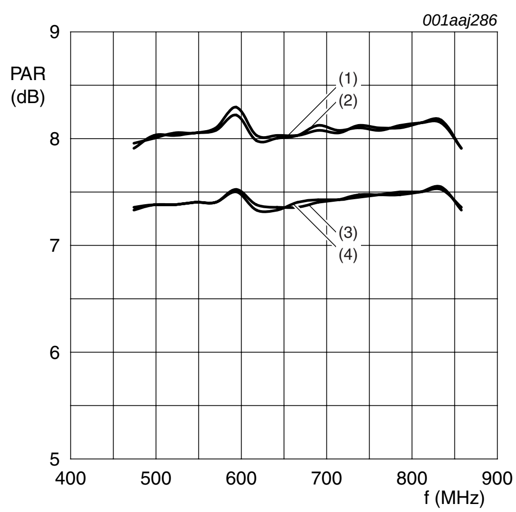


I_{Dq} = 0.5 A; measured in a common source broadband test circuit as described in Section 8.

(1) V_{DS} = 40 V; $P_{L(AV)}$ = 22 W

(2) V_{DS} = 42 V; $P_{L(AV)}$ = 24 W

Fig 10. DVB-T third order intermodulation distortion as a function of frequency; typical values



I_{Dq} = 0.5 A; measured in a common source broadband test circuit as described in Section 8.

PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

(1) PAR at 0.01 % probability on the CCDF; V_{DS} = 40 V; $P_{L(AV)}$ = 22 W

(2) PAR at 0.01 % probability on the CCDF; V_{DS} = 42 V; $P_{L(AV)}$ = 24 W

(3) PAR at 0.1 % probability on the CCDF; V_{DS} = 40 V; $P_{L(AV)}$ = 22 W

(4) PAR at 0.1 % probability on the CCDF; V_{DS} = 42 V; $P_{L(AV)}$ = 24 W

Fig 11. DVB-T PAR at 0.1 % and at 0.01 % probability on the CCDF as function of frequency; typical values

7.3 Ruggedness in class-AB operation

The BLF871 and BLF871S are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 42 V; f = 860 MHz at rated power.

7.4 Impedance information

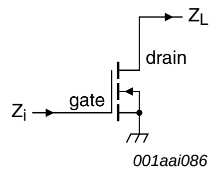


Fig 12. Definition of transistor impedance

Table 8. Typical impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 42 V.

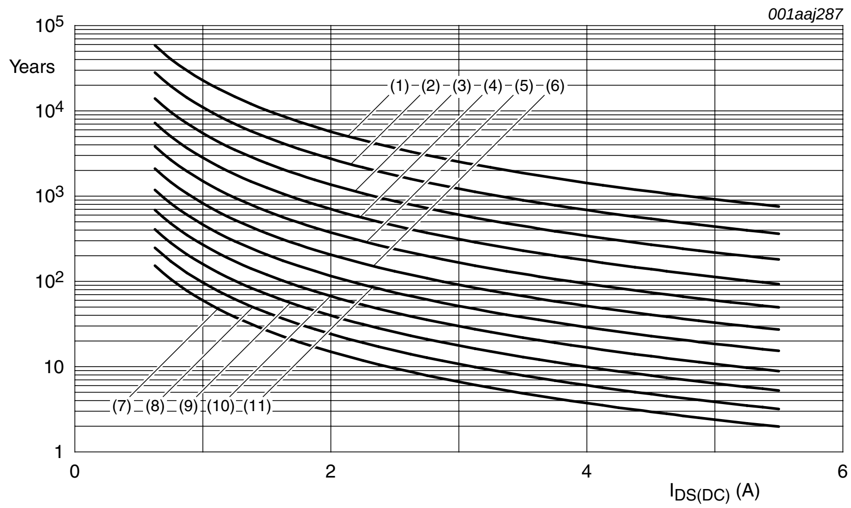
f (MHz)	Z_i (Ω)	Z_L (Ω)
300	0.977 – j3.327	5.506 + j1.774
325	0.977 – j2.983	5.366 + j1.858
350	0.978 – j2.681	5.223 + j1.930
375	0.979 – j2.414	5.078 + j1.990
400	0.979 – j2.174	4.932 + j2.040
425	0.980 – j1.956	4.786 + j2.079
450	0.981 – j1.758	4.640 + j2.108
475	0.982 – j1.576	4.495 + j2.128
500	0.982 – j1.407	4.352 + j2.138
525	0.983 – j1.250	4.212 + j2.140
550	0.984 – j1.103	4.074 + j2.135
575	0.985 – j0.964	3.940 + j2.122
600	0.986 – j0.834	3.809 + j2.102
625	0.987 – j0.709	3.682 + j2.077
650	0.988 – j0.591	3.558 + j2.045
675	0.990 – j0.478	3.438 + j2.009
700	0.991 – j0.370	3.323 + j1.968
725	0.992 – j0.266	3.211 + j1.923
750	0.993 – j0.165	3.103 + j1.874
775	0.995 – j0.068	3.000 + j1.822
800	0.996 + j0.026	2.900 + j1.766
825	0.997 + j0.117	2.804 + j1.708
850	0.999 + j0.206	2.711 + j1.648
875	1.000 + j0.292	2.623 + j1.586
900	1.002 + j0.376	2.538 + j1.521

Table 8. Typical impedance *...continued*

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 42 V.

f (MHz)	Z_i (Ω)	Z_L (Ω)
925	1.004 + j0.459	2.456 + j2.455
950	1.005 + j0.540	2.378 + j2.388
975	1.007 + j0.619	2.303 + j2.320
1000	1.009 + j0.696	2.230 + j2.250

7.5 Reliability



TTF (0.1 % failure fraction).

The reliability at pulsed conditions can be calculated as follows: TTF (0.1 %) × 1 / δ.

(1) T_j = 100 °C
(2) T_j = 110 °C
(3) T_j = 120 °C
(4) T_j = 130 °C
(5) T_j = 140 °C
(6) T_j = 150 °C
(7) T_j = 160 °C
(8) T_j = 170 °C
(9) T_j = 180 °C
(10) T_j = 190 °C
(11) T_j = 200 °C

Fig 13. Electromigration ($I_{DS(DC)}$)

8. Test information

Table 9. List of components

For test circuit, see Figure 14, Figure 15 and Figure 16.

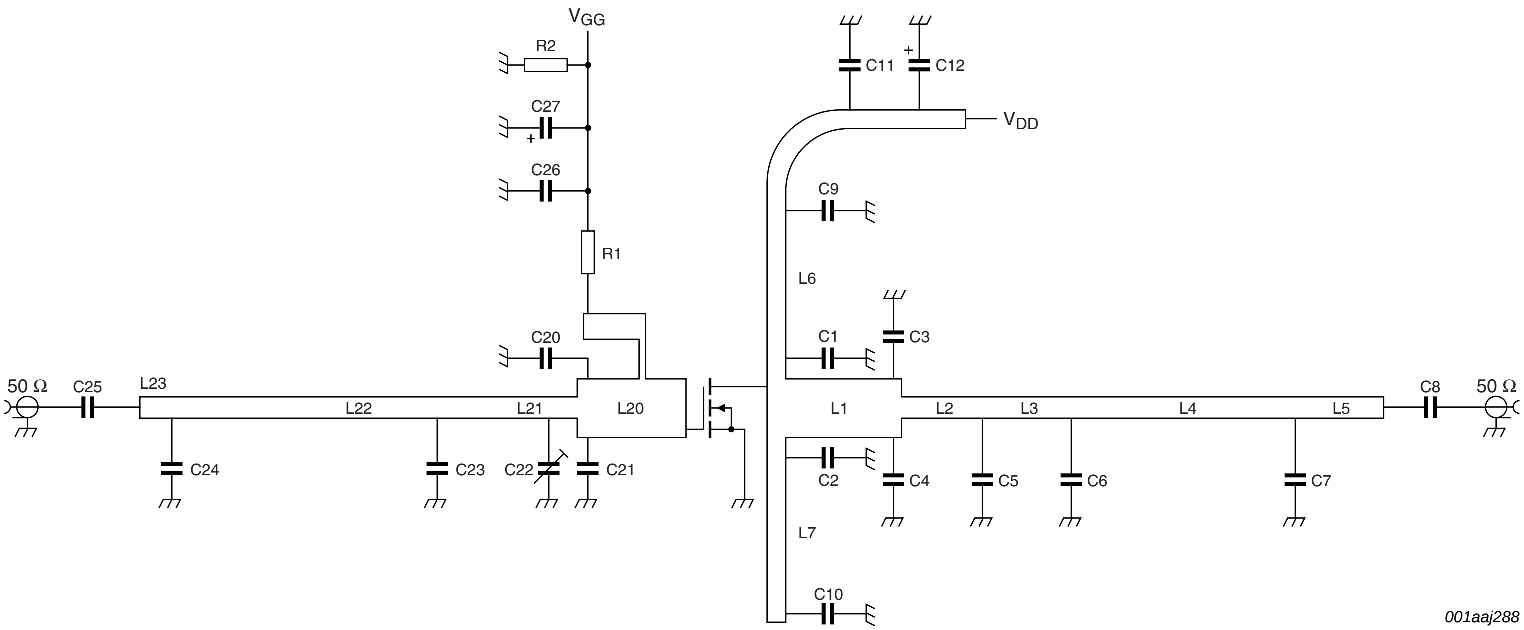
Component	Description	Value		Remarks
C1, C2	multilayer ceramic chip capacitor	5.1 pF	[1]	
C3, C4	multilayer ceramic chip capacitor	10 pF	[2]	
C5	multilayer ceramic chip capacitor	6.8 pF	[1]	
C6	multilayer ceramic chip capacitor	4.7 pF	[1]	
C7	multilayer ceramic chip capacitor	2.7 pF	[1]	
C8, C9, C10, C25, C26	multilayer ceramic chip capacitor	100 pF	[1]	
C11, C27	multilayer ceramic chip capacitor	10 μF		TDK C570X7R1H106KT000N or capacitor of same quality.
C12	electrolytic capacitor	470 μF; 63 V		
C20	multilayer ceramic chip capacitor	10 pF	[3]	
C21	multilayer ceramic chip capacitor	8.2 pF	[3]	
C22	trimmer	0.6 pF to 4.5 pF		Tekelec
C23	multilayer ceramic chip capacitor	6.8 pF	[3]	
C24	multilayer ceramic chip capacitor	3.9 pF	[3]	
L1	stripline	-	[4]	(W × L) 7 mm × 15 mm
L2	stripline	-	[4]	(W × L) 2.4 mm × 9 mm
L3	stripline	-	[4]	(W × L) 2.4 mm × 10 mm
L4	stripline	-	[4]	(W × L) 2.4 mm × 25 mm
L5	stripline	-	[4]	(W × L) 2.4 mm × 10 mm
L6	stripline	-	[4]	(W × L) 2.0 mm × 20 mm
L7	stripline	-	[4]	(W × L) 2.0 mm × 21 mm
L20	stripline	-	[4]	(W × L) 7 mm × 12 mm
L21	stripline	-	[4]	(W × L) 2.4 mm × 13 mm
L22	stripline	-	[4]	(W × L) 2.4 mm × 31 mm
L23	stripline	-	[4]	(W × L) 2.4 mm × 5 mm
R1	resistor	100 Ω		
R2	resistor	10 kΩ		

[1] American technical ceramics type 100B or capacitor of same quality.

[2] American technical ceramics type 180R or capacitor of same quality.

[3] American technical ceramics type 100A or capacitor of same quality.

[4] Printed-Circuit Board (PCB): Rogers 5880; ε_r = 2.2 F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 μm.



See Table 9 for a list of components.

Fig 14. Class-AB common-source broadband amplifier

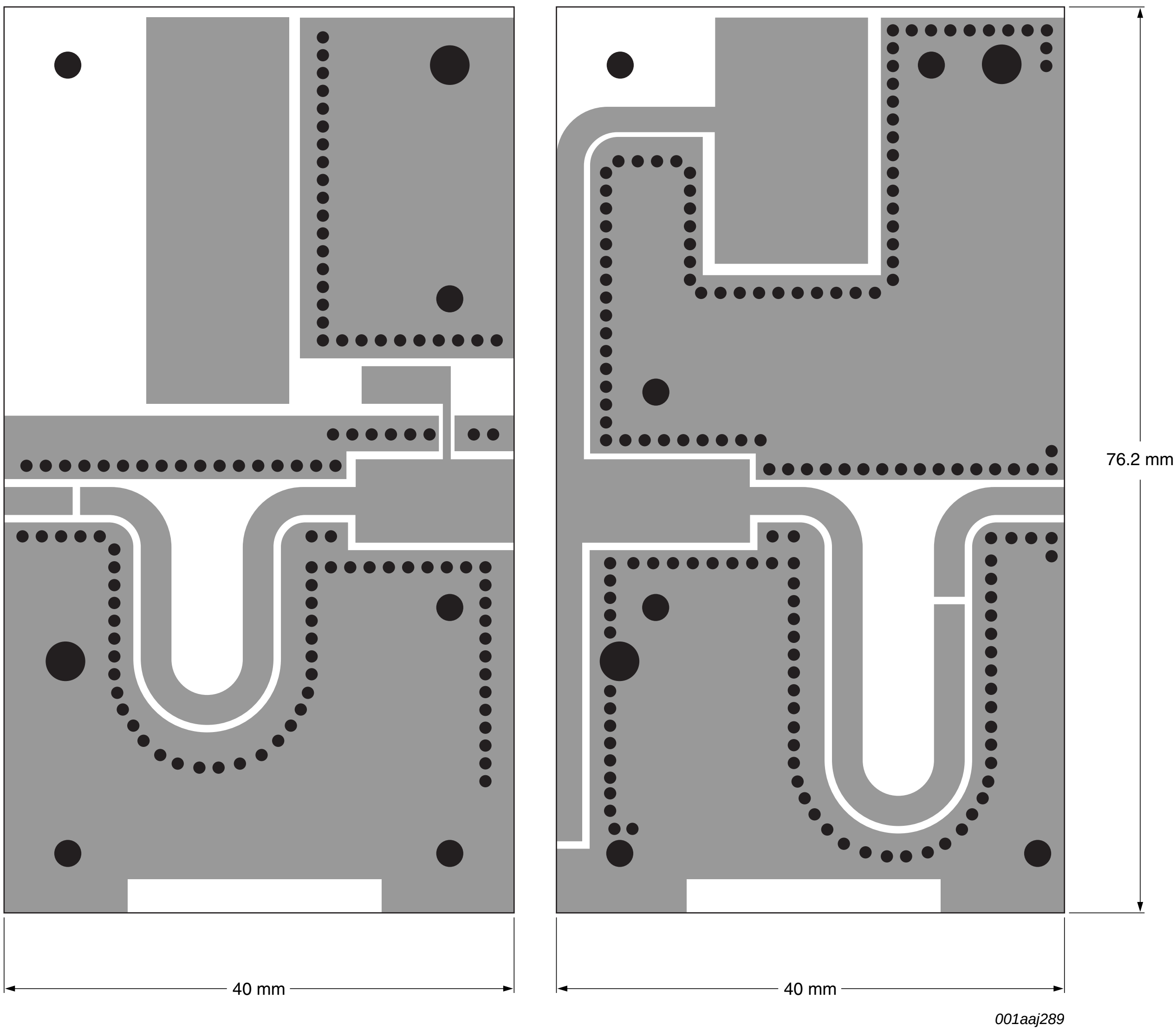
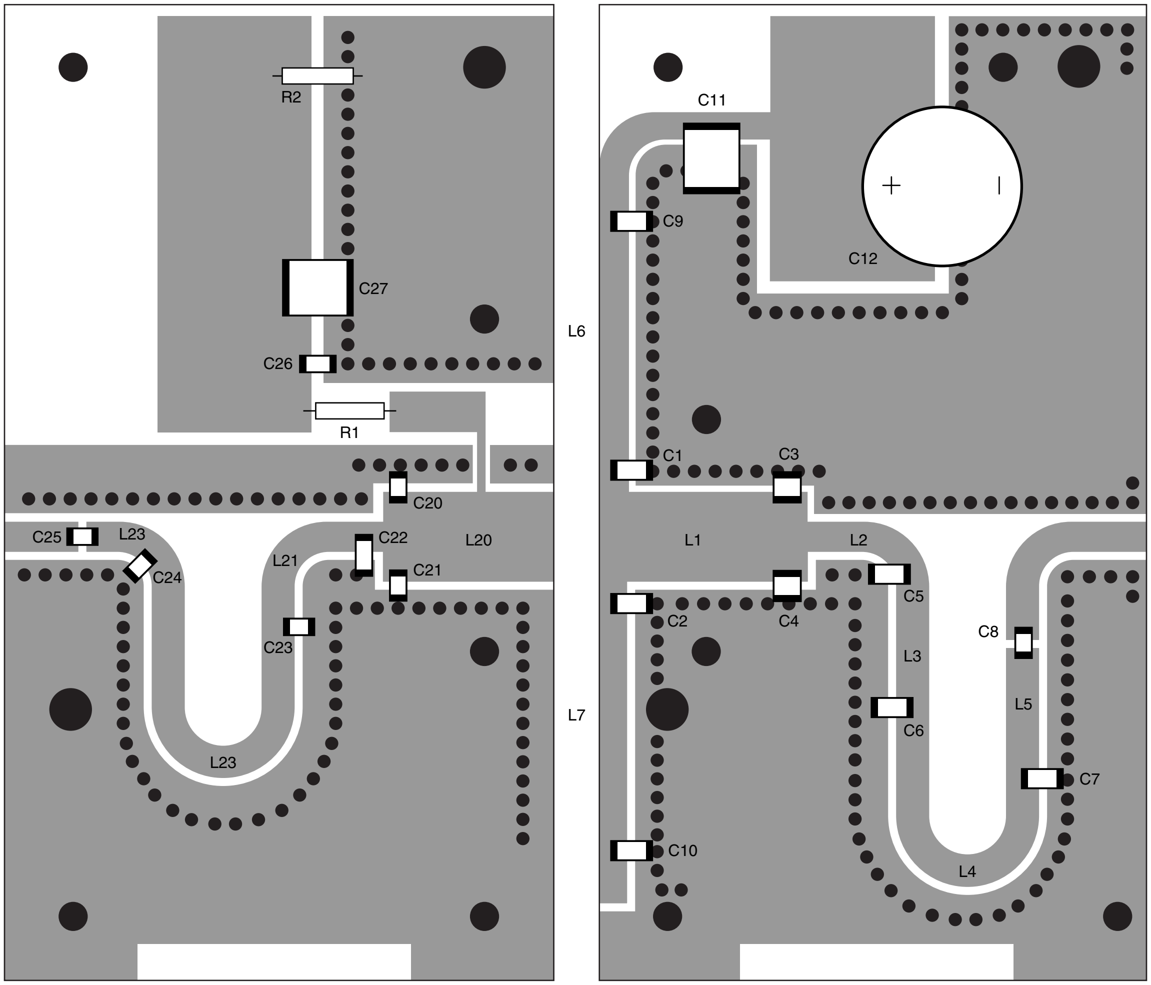


Fig 15. Printed-Circuit Board (PCB) for class-AB common source amplifier



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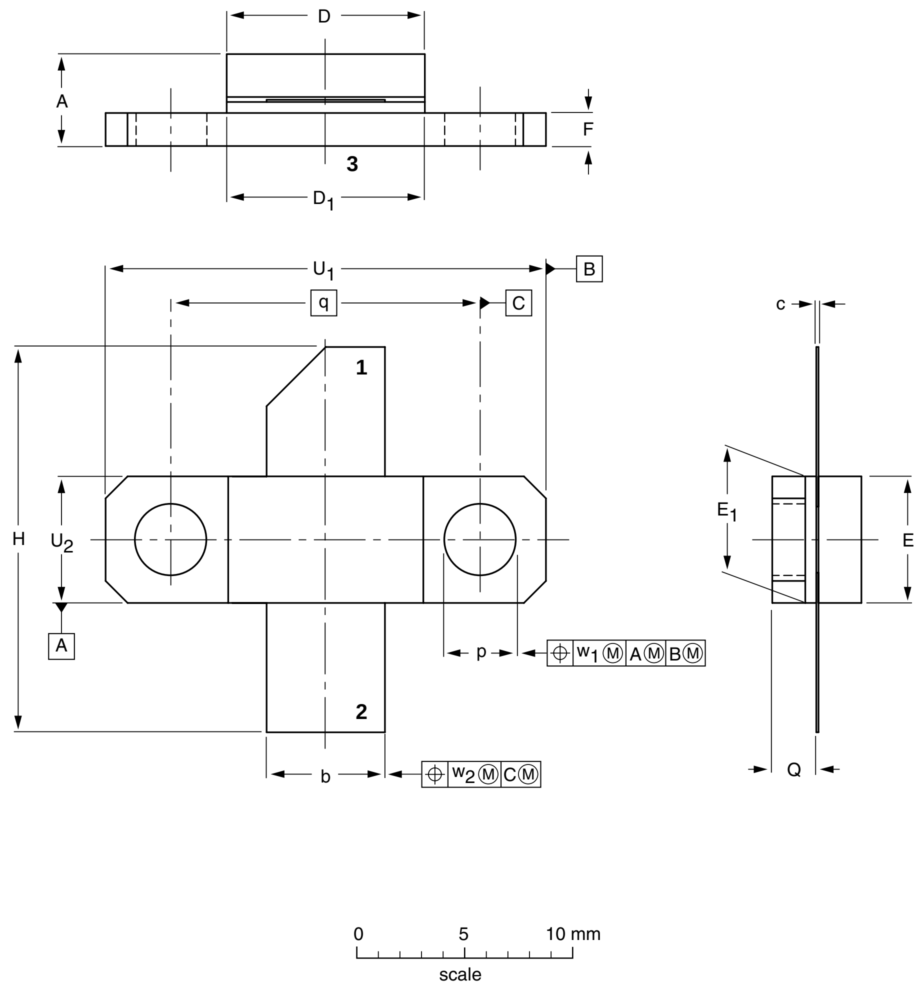
See Table 9 for a list of components.

Fig 16. Component layout for class-AB common source amplifier

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT467C**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

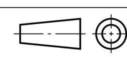
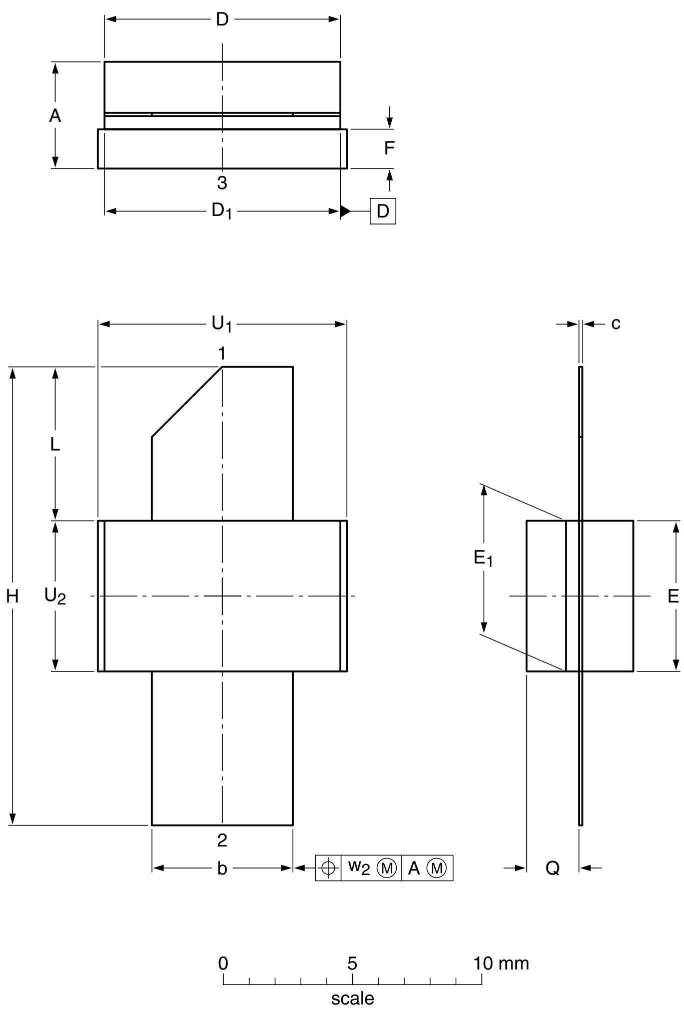
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						~~99-12-06~~ 99-12-28

Fig 17. Package outline SOT467C

Earless LDMOST ceramic package; 2 leads **SOT467B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	max	4.67	5.59	0.15	9.25	9.27	5.92	5.97	1.65	18.29	2.92	2.21	9.78	5.97	
	nom														0.25
	min	3.94	5.33	0.10	9.04	9.02	5.77	5.72	1.40	17.27	2.16	1.96	9.53	5.72	
inches	max	0.184	0.22	0.006	0.364	0.365	0.233	0.235	0.065	0.72	0.115	0.087	0.385	0.235	
	nom														0.01
	min	0.155	0.21	0.004	0.356	0.355	0.227	0.225	0.055	0.68	0.085	0.077	0.375	0.225	

Note

1. millimeter dimensions are derived from the original inch dimensions.

sot467b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT467B						~~08-12-09~~ 09-10-27

Fig 18. Package outline SOT467B

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
CCDF	Complementary Cumulative Distribution Function
DVB	Digital Video Broadcast
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
HF	High Frequency
IMD3	Third order InterModulation Distortion
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
OFDM	Orthogonal Frequency Division Multiplexing
PAR	Peak-to-Average power Ratio
PEP	Peak Envelope Power
RF	Radio Frequency
TTF	Time To Failure
UHF	Ultra High Frequency
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF871_BLF871S_4	20091119	Product data sheet	-	BLF871_3
Modifications:	• This document now describes both the BLF871 and the BLF871S.			
BLF871_3	20090921	Product data sheet	-	BLF871_2
BLF871_2	20090305	Preliminary data sheet	-	BLF871_1
BLF871_1	20081218	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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