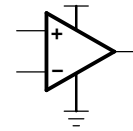


FAMILY OF LOW-POWER WIDE BANDWIDTH SINGLE SUPPLY OPERATIONAL AMPLIFIERS WITH SHUTDOWN

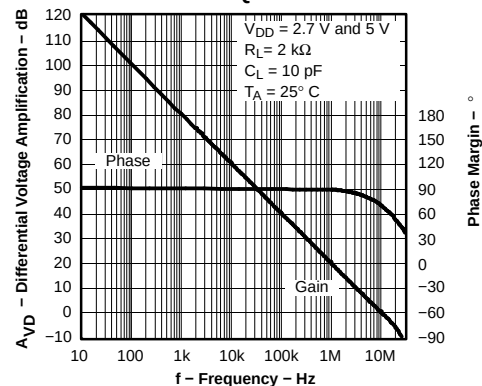
FEATURES

- CMOS Rail-To-Rail Output
- V_{ICR} Includes Positive Rail
- Wide Bandwidth . . . 11 MHz
- Slew Rate . . . 10 V/ μ s
- Supply Current . . . 800 μ A/Channel
- Input Noise Voltage . . . 27 nV/ $\sqrt{\text{Hz}}$
- Ultralow Power-Down Mode:
 $I_{DD(\text{SHDN})} = 4 \mu\text{A/Channel}$
- Supply Voltage Range . . . 2.7 V to 5.5 V
- Specified Temperature Range:
-40°C to 125°C . . . Industrial Grade
- Ultrasmall Packaging:
5 or 6 Pin SOT-23 (TLV2620/1)
8 or 10 Pin MSOP (TLV2622/3)
- Universal Opamp EVM (See SLOU060 for More Information)

Operational Amplifier



DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE
VS
FREQUENCY



DESCRIPTION

The TLV262x single supply operational amplifiers provide rail-to-rail output with an input range that includes the positive rail. The TLV262x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range (-40°C to 125°C) while adding the rail-to-rail output swing feature. The TLV262x also provides 11-MHz bandwidth from only 800 μ A of supply current. The maximum recommended supply voltage is 5.5 V, which, when coupled with a 2.7-V minimum, allows the devices to be operated from lithium ion cells. The combination of wide bandwidth, low noise, and low distortion makes it ideal for high speed and high resolution data converter applications. The positive input range allows it to directly interface to positive rail referred systems. All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes it compatible with Li-Ion powered systems and the operating supply voltage range of many micro-power micro-controllers available today including TI's MSP430.

AMPLIFIER SELECTION TABLE

DEVICE	V_{DD} [V]	$I_{DD/\text{ch}}$ [μ A]	V_{IO} [μ V]	I_{IB} [pA]	V_{ICR} [V]	GBW [MHz]	SLEW RATE [V/ μ s]	V_n , 1 kHz [nV/ $\sqrt{\text{Hz}}$]	I_o [mA]	SHUT- DOWN
TLV262x	2.7-5.5	750	250	1	1 V to $V_{DD} + 0.2$	11	10	27	28	Y
TLV263x	2.7-5.5	750	250	1	GND to $V_{DD} - 0.8$	10	9	27	28	Y
TLV278x	1.8-3.6	650	250	2.5	-0.2 to $V_{DD} + 0.2$	8	5	9	10	Y
TLC07x	4.5 - 16	1900	60	1.5	0.5 to $V_{DD} - 0.8$	10	19	7	55	Y
TLC08x	4.5 - 16	1900	60	3	GND to $V_{DD} - 1$	10	19	8.5	55	Y



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TLV2620 AND TLV2621 AVAILABLE OPTIONS⁽¹⁾

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE (D) ⁽²⁾	SOT-23		PLASTIC DIP (P)
			(DBV) ⁽³⁾	SYMBOL	
-40°C to 125°C	3500 µV	TLV2620ID TLV2621ID	TLV2620IDBV TLV2621IDBV	VBAI VBBI	TLV2620IP TLV2621IP

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2620IDR).
(3) The SOT23 package devices are only available taped and reeled. The **R** Suffix denotes quantities (3,000 pieces per reel). For smaller quantities (250 pieces per mini-reel), add a **T** suffix to the part number (e.g. TLV2620IDBVT).

TLV2622 AND TLV2623 AVAILABLE OPTIONS⁽¹⁾

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES						
		SMALL OUTLINE ⁽²⁾ (D)	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)
			(DGK) ⁽²⁾	SYMBOL	(DGS) ⁽²⁾	SYMBOL		
-40°C to 125°C	3500 µV	TLV2622ID TLV2623ID	TLV2622IDGK —	xxTIAKM —	— TLV2623IDGS	— xxTIALC	— TLV2623IN	TLV2622IP —

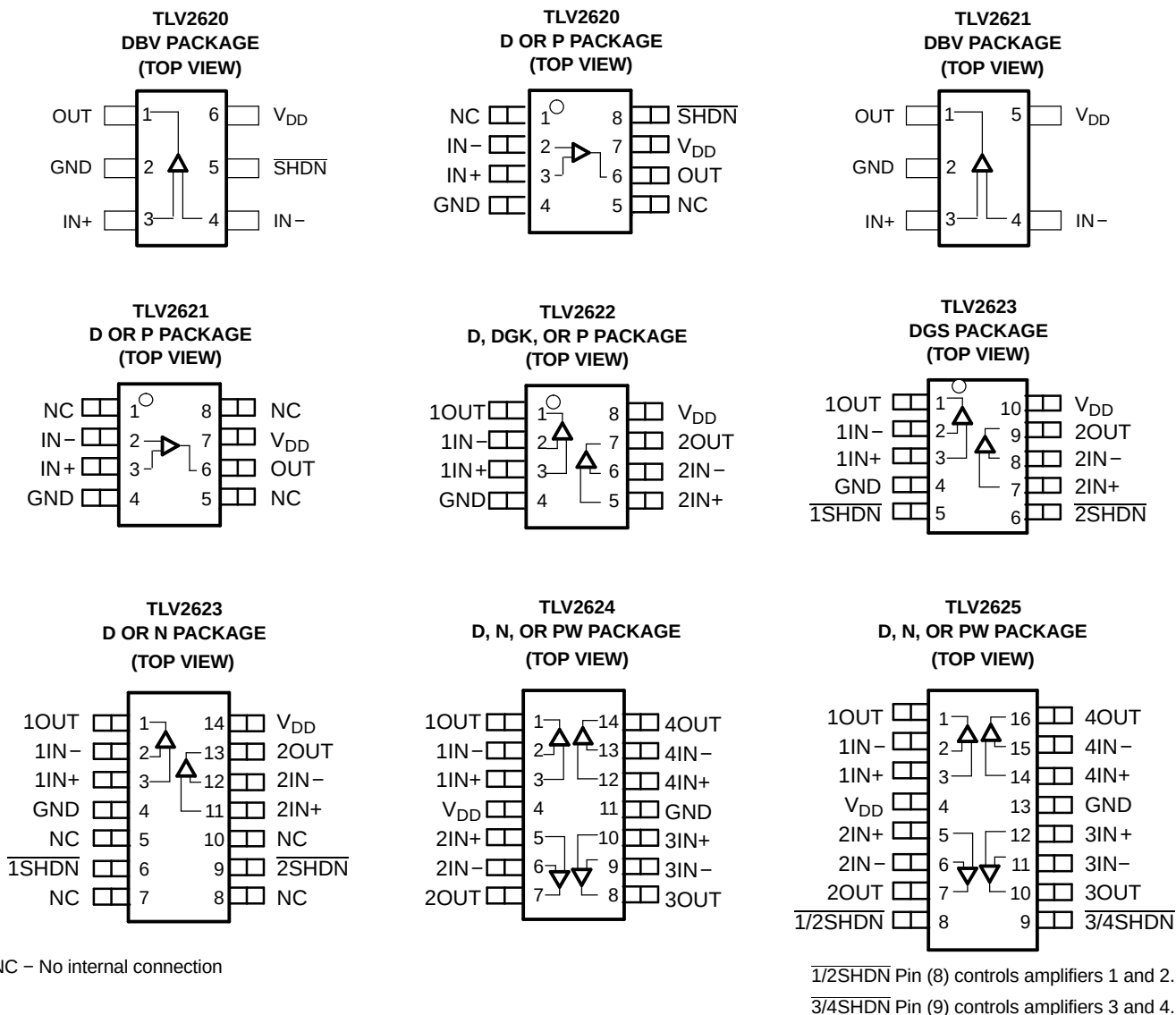
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2622IDR).

TLV2624 AND TLV2625 AVAILABLE OPTIONS⁽¹⁾

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE (D) ⁽²⁾	PLASTIC DIP (N)	TSSOP (PW)
-40°C to 125°C	3500 µV	TLV2624ID TLV2625ID	TLV2624IN TLV2625IN	TLV2624IPW TLV2625IPW

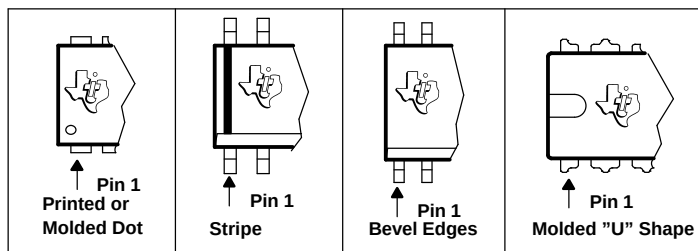
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2624IDR).

TLV262X PACKAGE PINOUTS⁽¹⁾



(1) SOT-23 may or may not be indicated.

TYPICAL PIN 1 INDICATORS



NOTE:

If there is not a Pin 1 indicator, turn device to enable reading the symbol from left to right. Pin 1 is at the lower left corner of the device.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

V _{DD}	Supply voltage ⁽²⁾	6 V
V _{ID}	Differential input voltage	±V _{DD}
V _I	Input voltage range ⁽²⁾	+1 to V _{DD} + 0.2 V
I _I	Input current (any input)	± 10 mA
I _O	Output current	±40 mA
	Continuous total power dissipation	See Dissipation Rating Table
T _A	Operating free-air temperature range: I-suffix	-40°C to 125°C
T _J	Maximum junction temperature	150°C
T _{stg}	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	θ _{JC} (°C/W)	θ _{JA} (°C/W)	T _A ≤ 25°C POWER RATING	T _A = 125°C POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.3	1022 mW	204.4 mW
D (16)	25.7	114.7	1090 mW	218 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DBV (6)	55	294.3	425 mW	85 mW
DGK (8)	54.2	259.9	481 mW	96.1 mW
DGS (10)	54.1	259.7	485 mW	97 mW
N (14, 16)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW
PW (16)	28.7	161.4	774 mW	154.9 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V _{DD}	Supply voltage	Single supply	2.7	5.5	V
		Split supply	±1.35	±2.75	
V _{ICR}	Common-mode input voltage range		1	V _{DD} +0.2	V
T _A	Operating free-air temperature	I-suffix	-40	125	°C
	Shutdown on/off voltage level ⁽¹⁾	V _{IL}	0.4		V
		V _{IH}	2		

- (1) Relative to GND.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A ⁽¹⁾	MIN	TYP	MAX	UNIT
DC PERFORMANCE								
V _{IO}	Input offset voltage	V _{IC} = V _{DD} /2, V _O = V _{DD} /2, R _S = 50 Ω		25°C	250	3500	μV	
				Full range	4500			
α _{VIO}	Temperature coefficient of input offset voltage			25°C	3		μV/°C	
CMRR	Common-mode rejection ratio	V _{IC} = 1 to V _{DD} , R _S = 50 Ω	V _{DD} = 2.7 V	25°C	77	98	dB	
				Full range	63			
			V _{DD} = 5 V	25°C	78	99		
				Full range	75			
A _{VD}	Large-signal differential voltage amplification	V _{DD} = 2.7 V, R _L = 2 kΩ, V _{O(PP)} = 1.7 V		25°C	90	100	dB	
				Full range	82			
		V _{DD} = 5 V, R _L = 2 kΩ, V _{O(PP)} = 4 V		25°C	95	100		
				Full range	90			
INPUT CHARACTERISTICS								
I _{IO}	Input offset current	V _{IC} = V _{DD} /2, V _O = V _{DD} /2, R _S = 50Ω		25°C	2	50	pA	
				Full Range	100			
I _{IB}	Input bias current			25°C	2	50		
				Full Range	200			
r _{I(d)}	Differential input resistance			25°C	100		GΩ	
C _{i(c)}	Common-mode input capacitance	f = 1 kHz		25°C	8		pF	
OUTPUT CHARACTERISTICS								
V _{OH}	High-level output voltage	V _{IC} = V _{DD} /2, I _{OH} = -1 mA	V _{DD} = 2.7 V	25°C	2.6	2.67	V	
				Full range	2.55			
			V _{DD} = 5 V	25°C	4.95	4.98		
				Full range	4.9			
		V _{IC} = V _{DD} /2, I _{OH} = -10 mA	V _{DD} = 2.7 V	25°C	2.3	2.43		
				Full range	2.2			
			V _{DD} = 5 V	25°C	4.7	4.8		
				Full range	4.6			
V _{OL}	Low-level output voltage	V _{IC} = V _{DD} /2, I _{OL} = 1 mA	V _{DD} = 2.7 V	25°C	0.03	0.1	V	
				Full range	0.15			
			V _{DD} = 5 V	25°C	0.025	0.05		
				Full range	0.1			
		V _{IC} = V _{DD} /2, I _{OL} = 10 mA	V _{DD} = 2.7 V	25°C	0.26	0.4		
				Full range	0.45			
			V _{DD} = 5 V	25°C	0.2	0.25		
				Full range	0.35			
I _O	Output current	V _{DD} = 2.7 V, V _O = 0.5 V from rail	Sourcing	25°C	14	mA		
			Sinking		19			
		V _{DD} = 5 V, V _O = 0.5 V from rail	Sourcing		28			
			Sinking		28			
I _{OS}	Short-circuit output current	Sourcing	V _{DD} = 2.7 V	25°C	50	mA		
			V _{DD} = 5 V		95			
		Sinking	V _{DD} = 2.7 V		50			
			V _{DD} = 5 V		95			

(1) Full range is -40°C to 125°C for the I-suffix.

ELECTRICAL CHARACTERISTICS (continued)

at specified free-air temperature, $V_{DD} = 2.7\text{ V}$, 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A ⁽¹⁾	MIN	TYP	MAX	UNIT
POWER SUPPLY								
I _{DD}	Supply current (per channel)	V _O = V _{DD} /2, $\overline{\text{SHDN}}$ = V _{DD}		25°C	800	1000		μA
				Full range	1300			
PSRR	Supply voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 2.7 V to 3.3 V, V _{IC} = V _{DD} /2	No load	25°C	80	98		dB
				Full range	75			
		V _{DD} = 2.7 V to 5 V, V _{IC} = V _{DD} /2		25°C	75	90		
				Full range	70			
DYNAMIC PERFORMANCE								
UGBW	Unity gain bandwidth	R _L = 2 kΩ, C _L = 10 pF		25°C	11			MHz
SR+	Positive slew rate at unity gain	R _L = 2 kΩ, C _L = 50 pF	V _{DD} = 2.7 V, V _{O(PP)} = 1.7 V	25°C	3.5	4.5		V/μs
				Full range	2.7			
			V _{DD} = 5 V, V _{O(PP)} = 3.5 V	25°C	5.4	7		
				Full range	3.4			
SR-	Negative slew rate at unity gain	R _L = 2 kΩ, C _L = 50 pF	V _{DD} = 2.7 V, V _{O(PP)} = 1.7 V	25°C	2.7	5		V/μs
				Full range	2.3			
			V _{DD} = 5 V, V _{O(PP)} = 3.5 V	25°C	4.5	6		
				Full range	3.2			
φ _m	Phase margin	R _L = 2 kΩ, C _L = 10 pF		25°C	63°			dB
	Gain margin				8			
NOISE/DISTORTION PERFORMANCE								
THD + N	Total harmonic distortion plus noise	V _{O(PP)} = V _{DD} /2, R _L = 2 kΩ, f = 10 kHz	A _V = 1	25°C	0.002%			nV/√Hz
			A _V = 10		0.019%			
			A _V = 100		0.095%			
V _n	Equivalent input noise voltage	f = 1 kHz	53					
		f = 10 kHz	27					
I _n	Equivalent input noise current	f = 1 kHz			0.9		fA/√Hz	
SHUTDOWN CHARACTERISTICS								
I _{DD(SHDN)}	Supply current, per channel in shutdown mode (TLV2620, TLV2623, TLV2625)	$\overline{\text{SHDN}}$ = 0.4 V		25°C	4	11		μA
				Full range	13			
t _(on)	Amplifier turnon time ⁽²⁾	R _L = 2 kΩ	V _{DD} = 2.7 V	25°C	4.5			μs
			V _{DD} = 5 V		1.5			
t _(off)	Amplifier turnoff time ⁽²⁾	R _L = 2 kΩ			200			ns

(2) Disable time and enable time are defined as the interval between application of the logic signal to $\overline{SHDN}$ and the point at which the supply current has reached half its final value.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
CMRR	Common-mode rejection ratio	vs Frequency	3
V_{OH}	High-level output voltage	vs High-level output current	4, 6
V_{OL}	Low-level output voltage	vs Low-level output current	5, 7
I_{DD}	Supply current	vs Supply voltage	8
I_{DD}	Supply current	vs Free-air temperature	9
PSRR	Power supply rejection ratio	vs Frequency	10
A_{VD}	Differential voltage amplification & phase	vs Frequency	11
	Gain-bandwidth product	vs Free-air temperature	12
SR	Slew rate	vs Supply voltage	13
		vs Free-air temperature	14, 15
ϕ_m	Phase margin	vs Load capacitance	16
V_n	Equivalent input noise voltage	vs Frequency	17
	Voltage-follower large-signal pulse response		18
	Voltage-follower small-signal pulse response		19
	Crosstalk	vs Frequency	20
$I_{DD(SHDN)}$	Shutdown supply current	vs Free-air temperature	21
$I_{DD(SHDN)}$	Shutdown supply current	vs Supply voltage	22
$I_{DD(SHDN)}$	Shutdown supply current/output voltage	vs Time	23

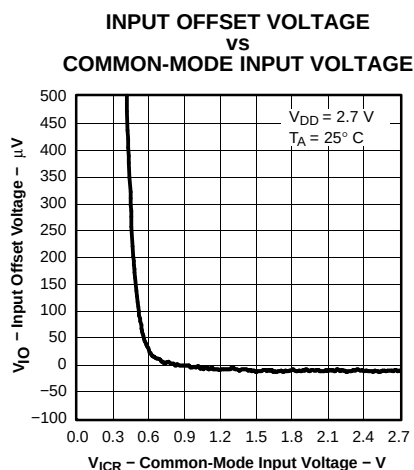


Figure 1.

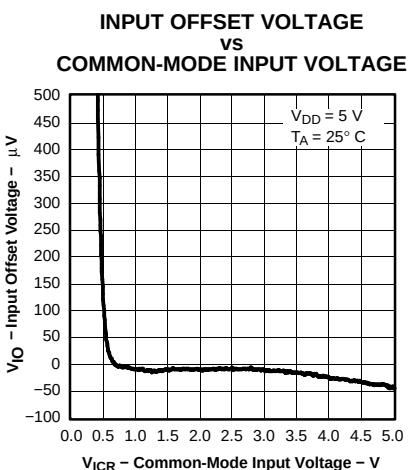


Figure 2.

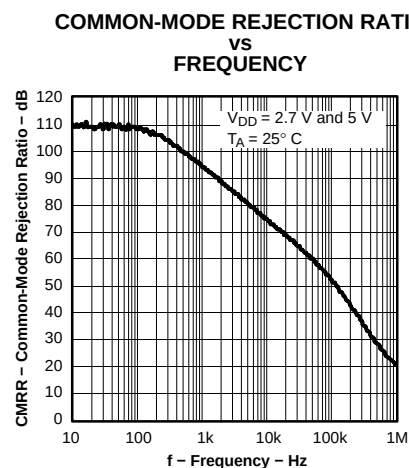


Figure 3.

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

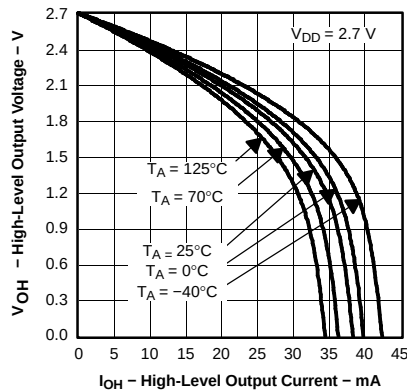


Figure 4.

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

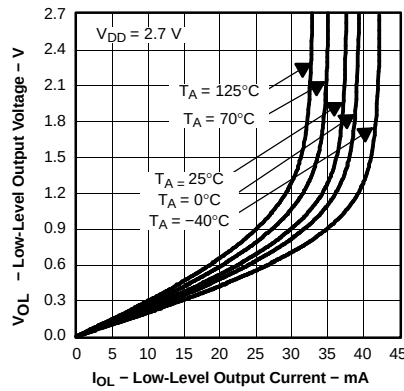


Figure 5.

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

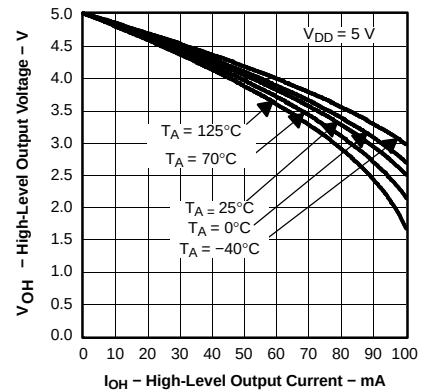


Figure 6.

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

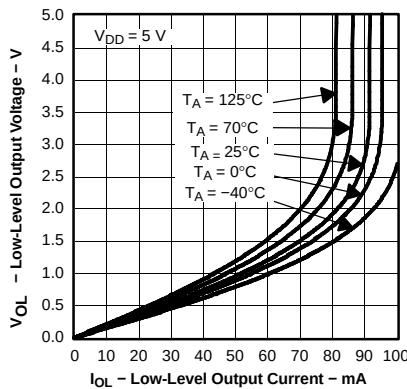


Figure 7.

**SUPPLY CURRENT
VS
SUPPLY VOLTAGE**

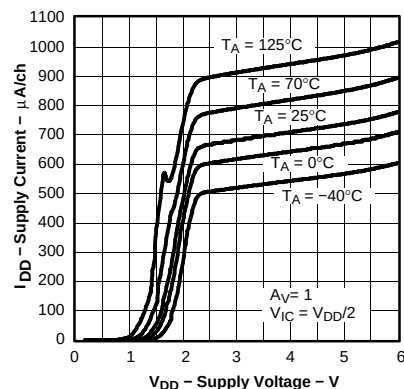


Figure 8.

**SUPPLY CURRENT
VS
FREE-AIR TEMPERATURE**

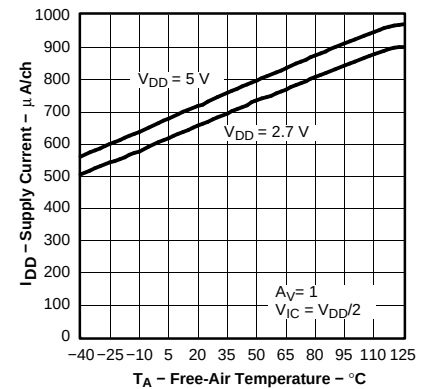


Figure 9.

**POWER SUPPLY REJECTION RATIO
VS
FREQUENCY**

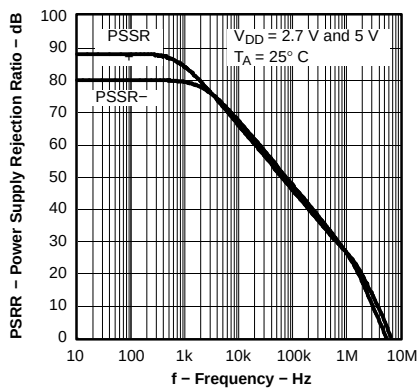


Figure 10.

**DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE
VS
FREQUENCY**

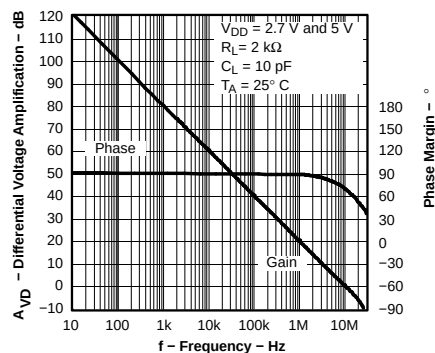


Figure 11.

**GAIN-BANDWIDTH PRODUCT
VS
FREE-AIR TEMPERATURE**

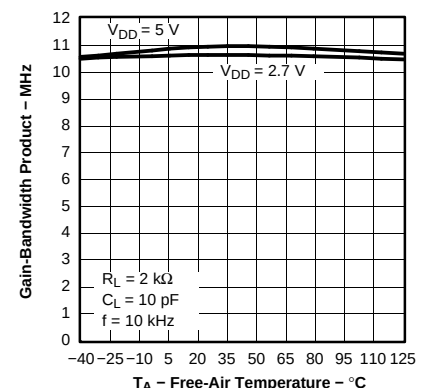


Figure 12.

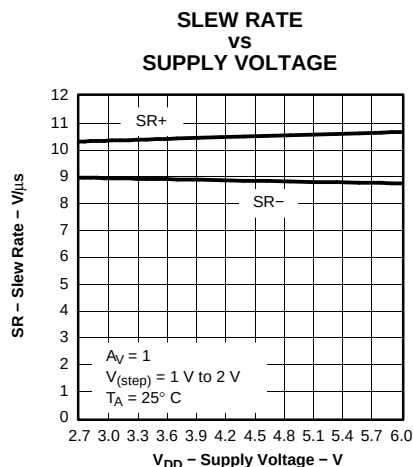


Figure 13.

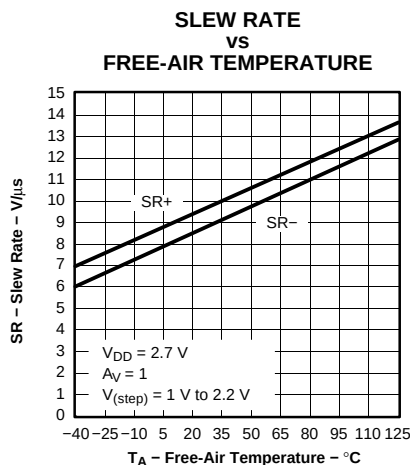


Figure 14.

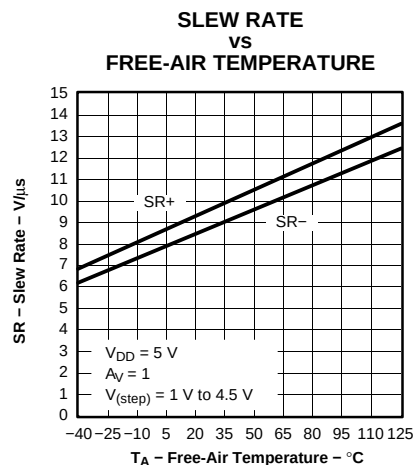


Figure 15.

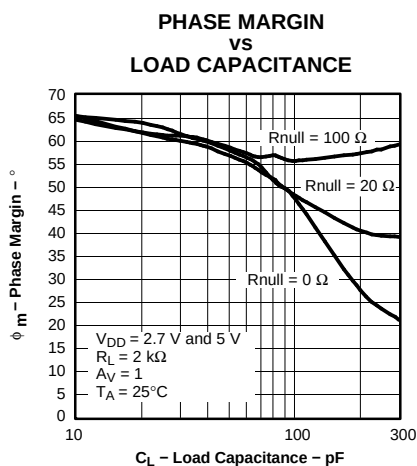


Figure 16.

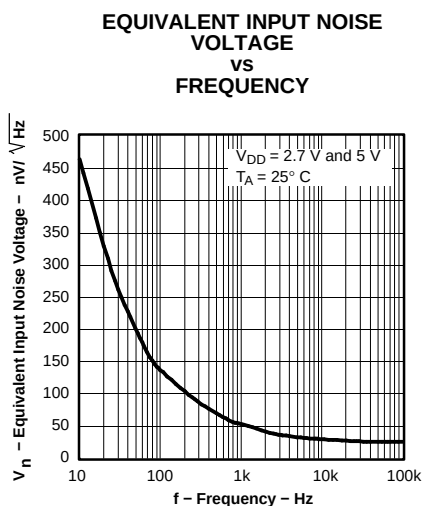


Figure 17.

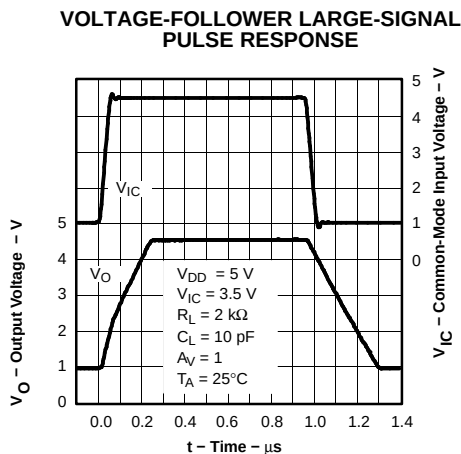


Figure 18.

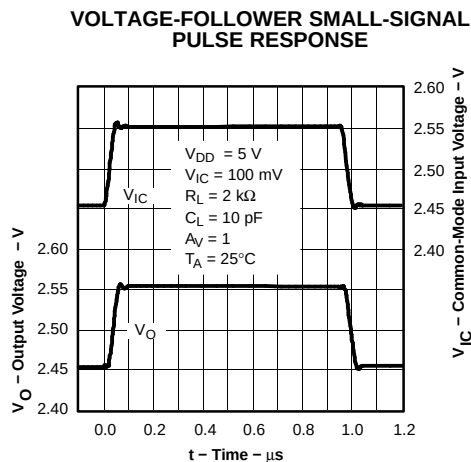


Figure 19.

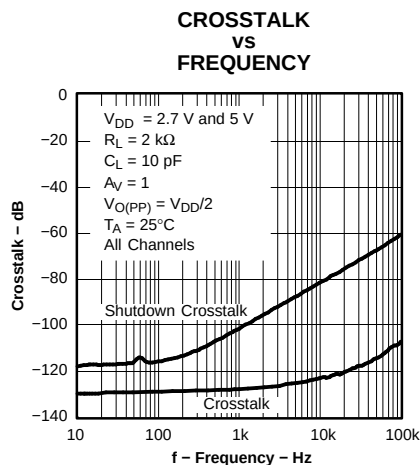


Figure 20.

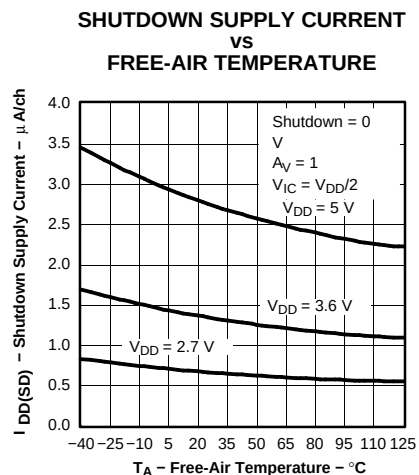


Figure 21.

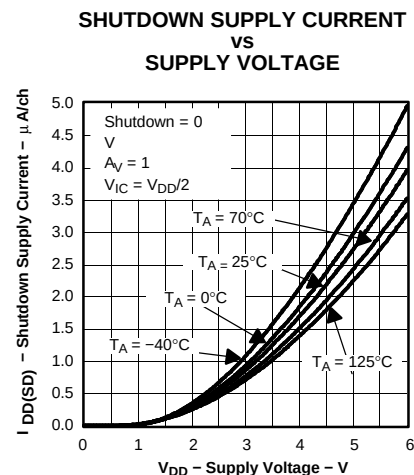


Figure 22.

**SHUTDOWN SUPPLY CURRENT/OUTPUT VOLTAGE
vs
TIME**

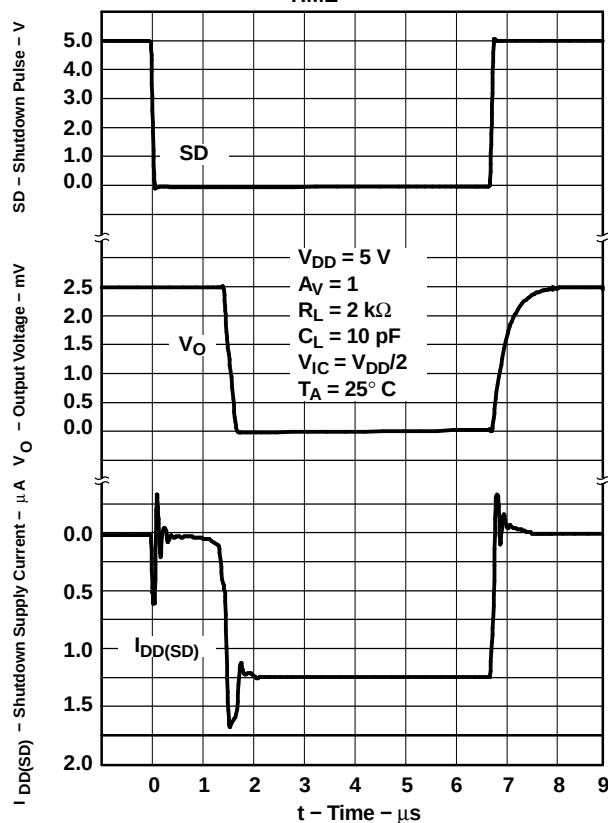


Figure 23.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2620IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBAI	Samples
TLV2620IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBAI	Samples
TLV2620IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBAI	Samples
TLV2620IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2620I	Samples
TLV2621IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBBI	Samples
TLV2621IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBBI	Samples
TLV2621IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBBI	Samples
TLV2621IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2621I	Samples
TLV2622ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2622I	Samples
TLV2622IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2622I	Samples
TLV2622IDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKM	Samples
TLV2622IDGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKM	Samples
TLV2622IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKM	Samples
TLV2622IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2622I	Samples
TLV2623IDGS	ACTIVE	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALC	Samples
TLV2623IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ALC	Samples
TLV2623IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2623I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2624ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2624I	Samples
TLV2624IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2624I	Samples
TLV2624IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2624I	Samples
TLV2624IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2624I	Samples
TLV2624IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2624I	Samples
TLV2624IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2624I	Samples
TLV2625IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2625I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

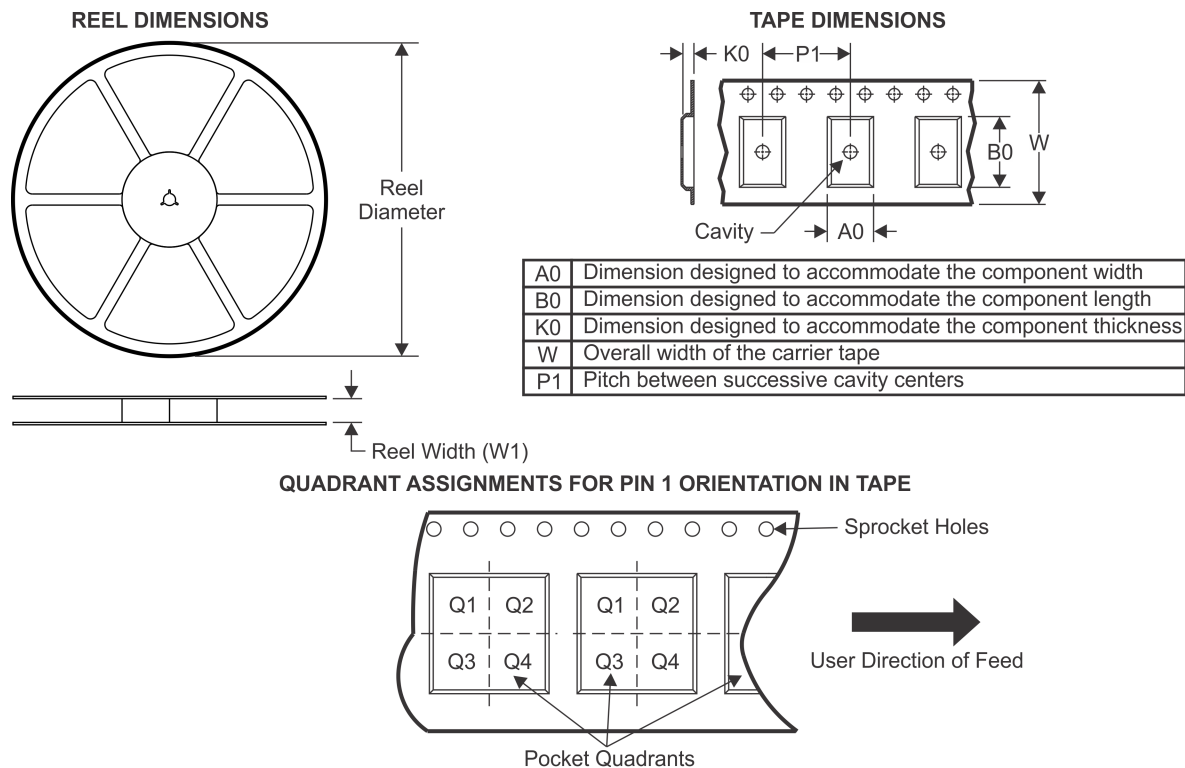
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

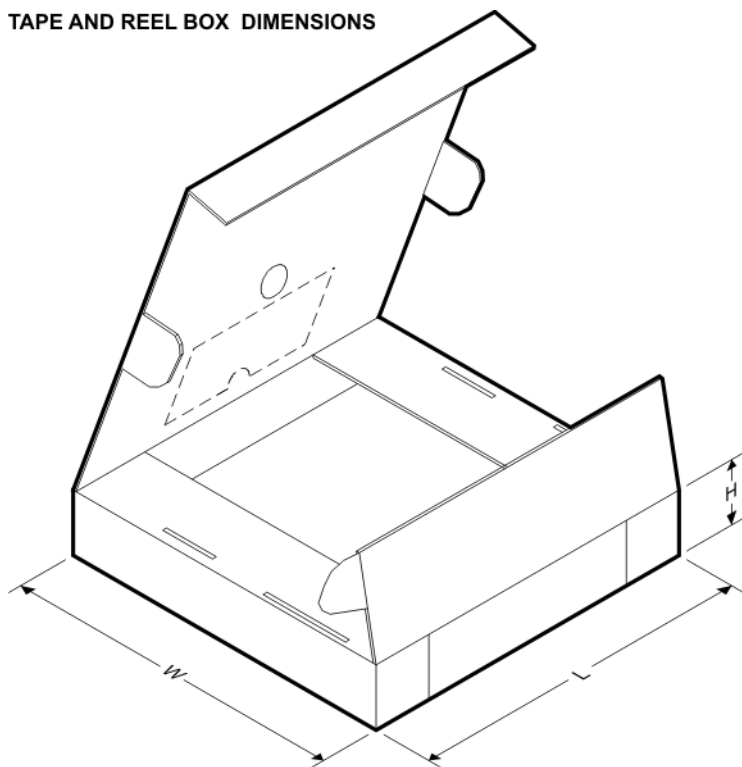
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2620IDBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2620IDBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2620IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2621IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2621IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2621IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2622IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2622IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2623IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2623IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2624IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2624IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2625IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

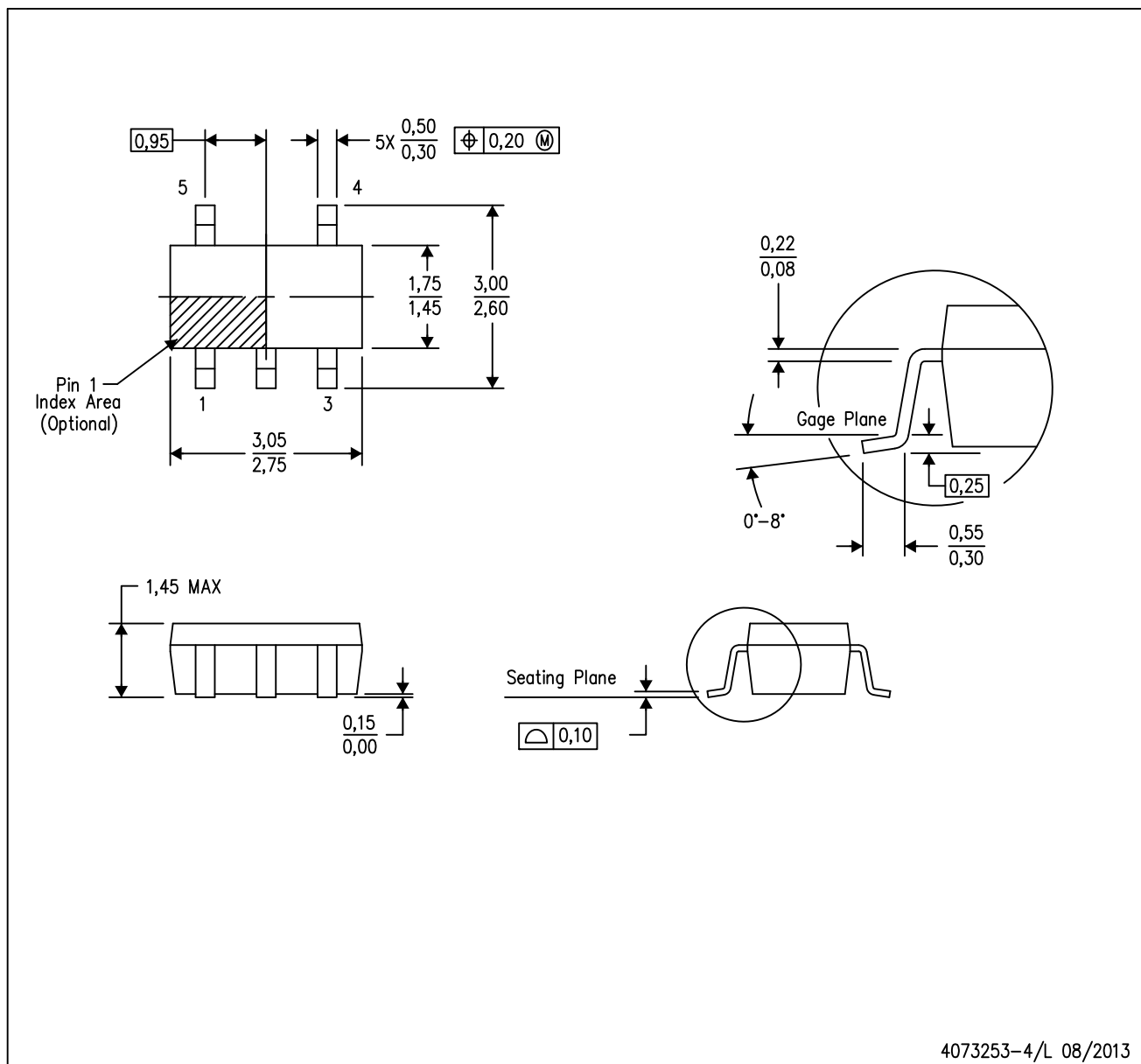


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2620IDBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TLV2620IDBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TLV2620IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2621IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2621IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2621IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2622IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2622IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2623IDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2623IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2624IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV2624IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TLV2625IDR	SOIC	D	16	2500	333.2	345.9	28.6

DBV (R-PDSO-G5)

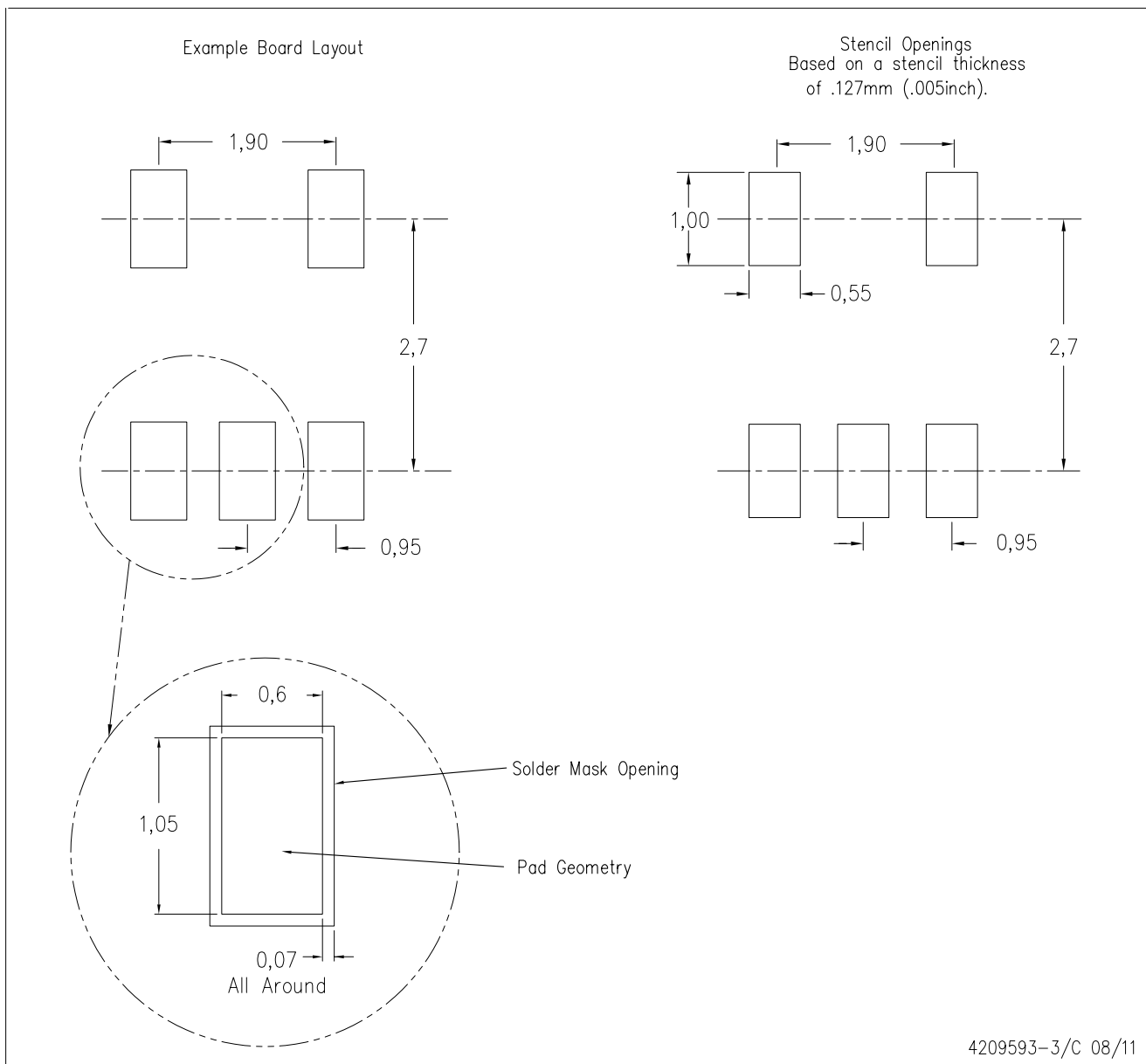
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

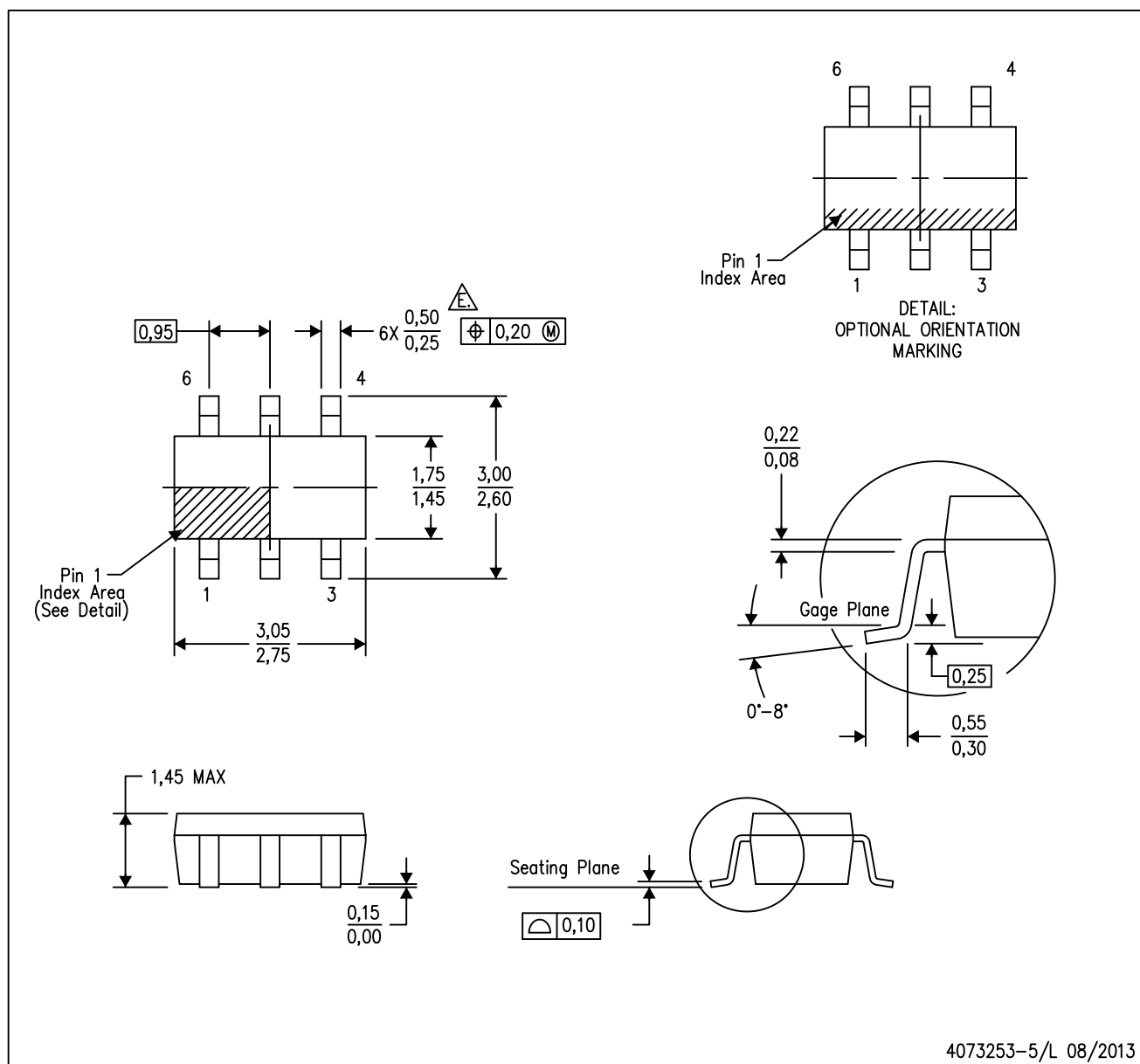
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DBV (R-PDSO-G6)

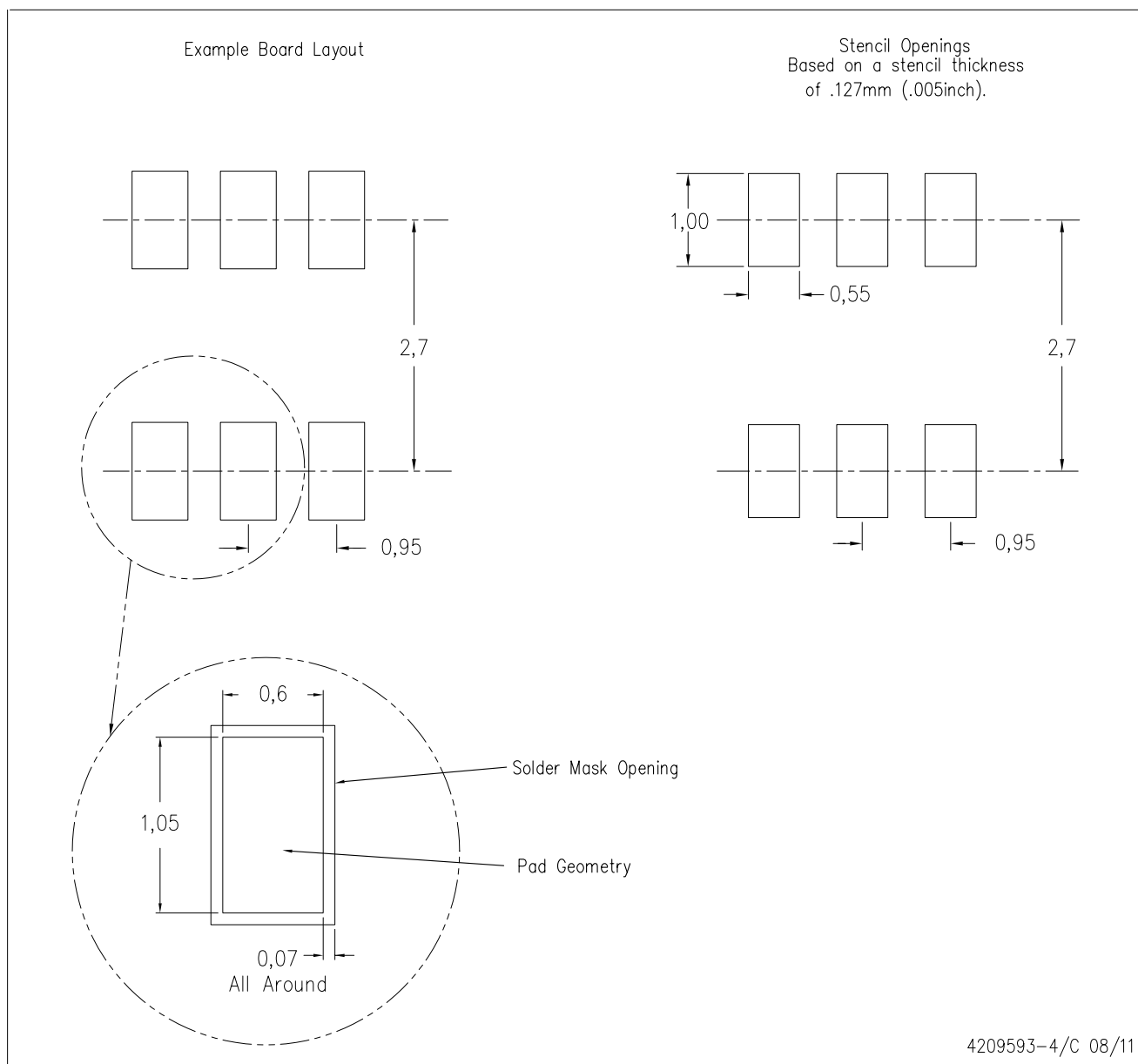
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
 - Δ Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

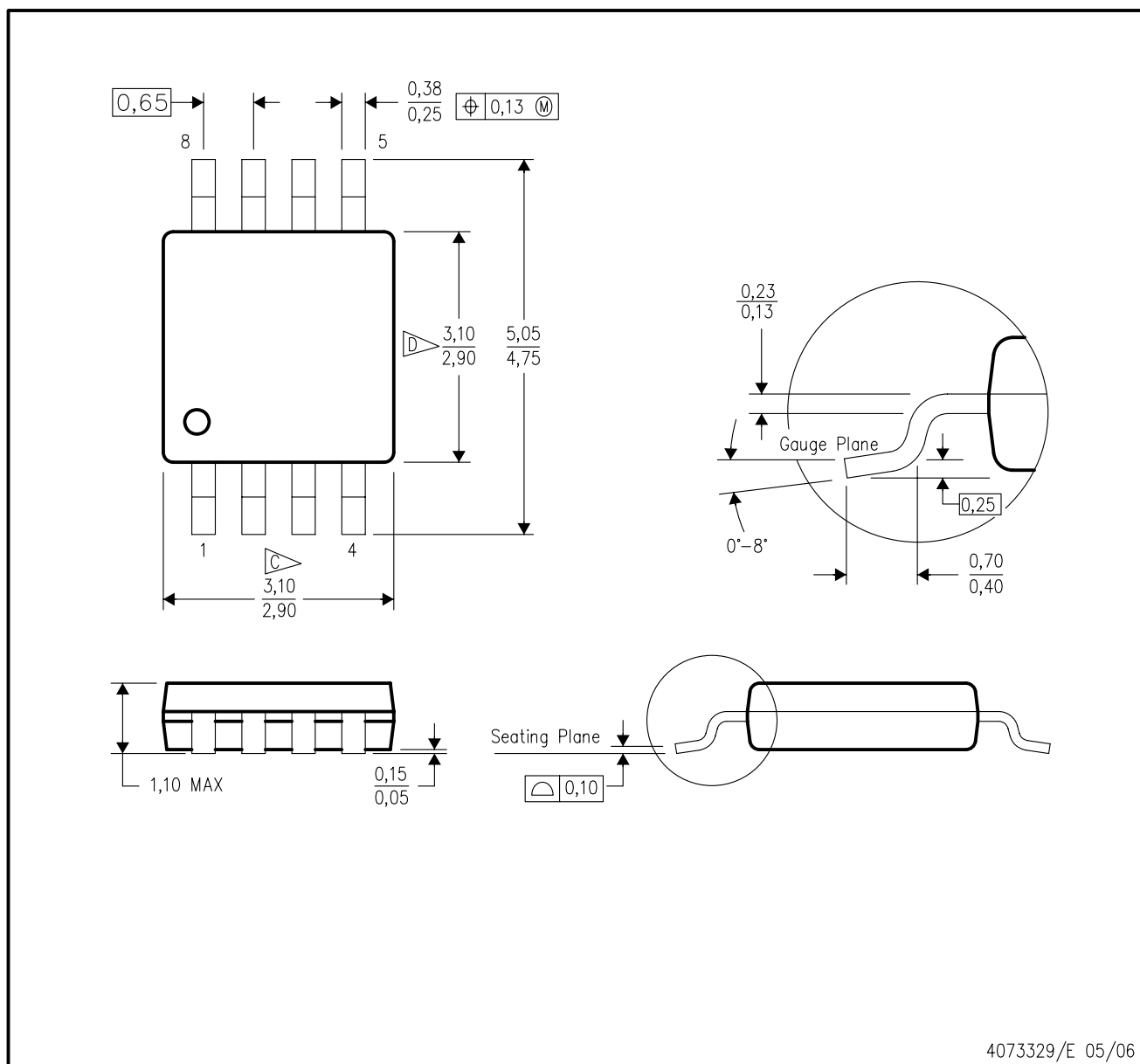
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

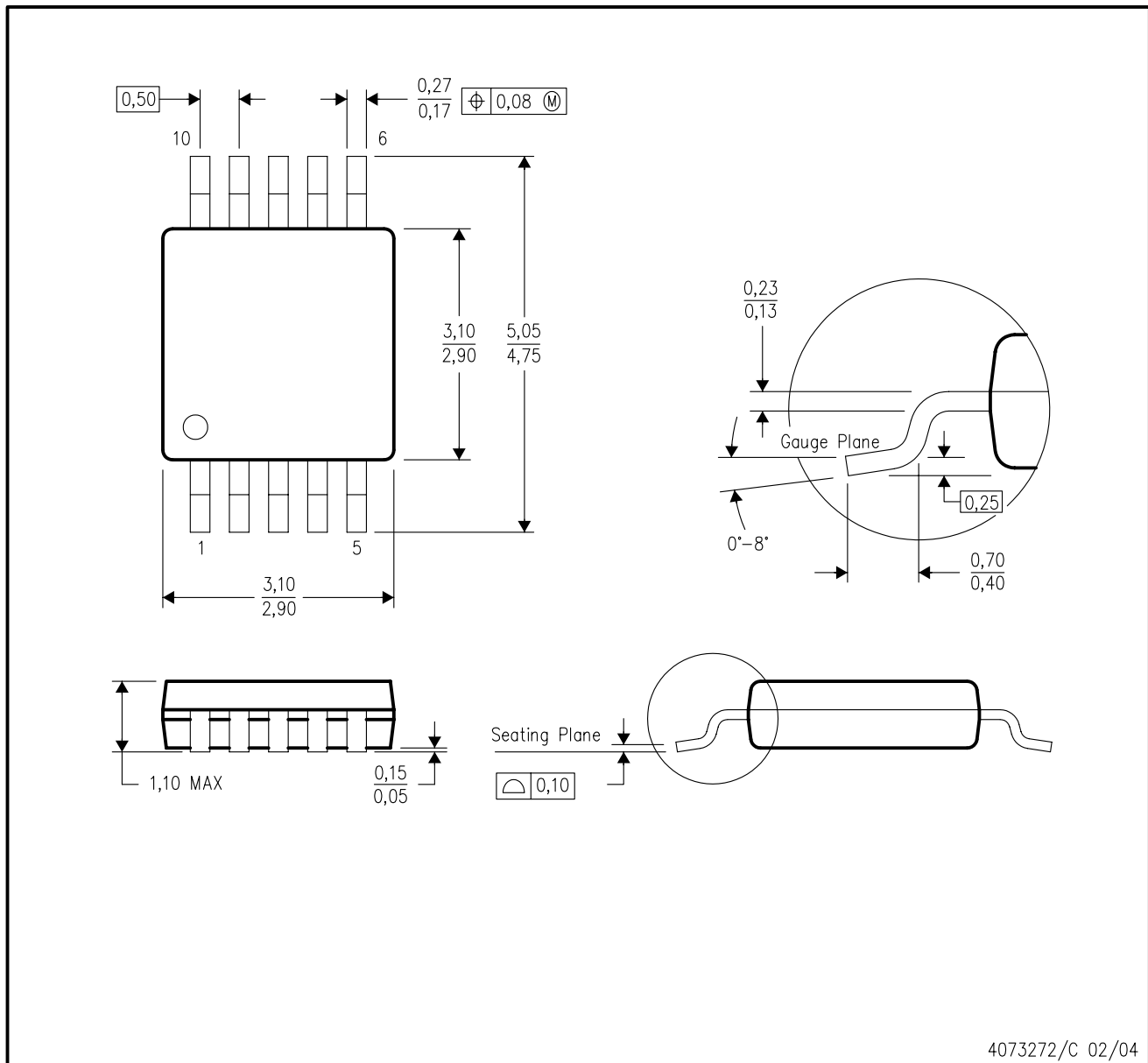


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE

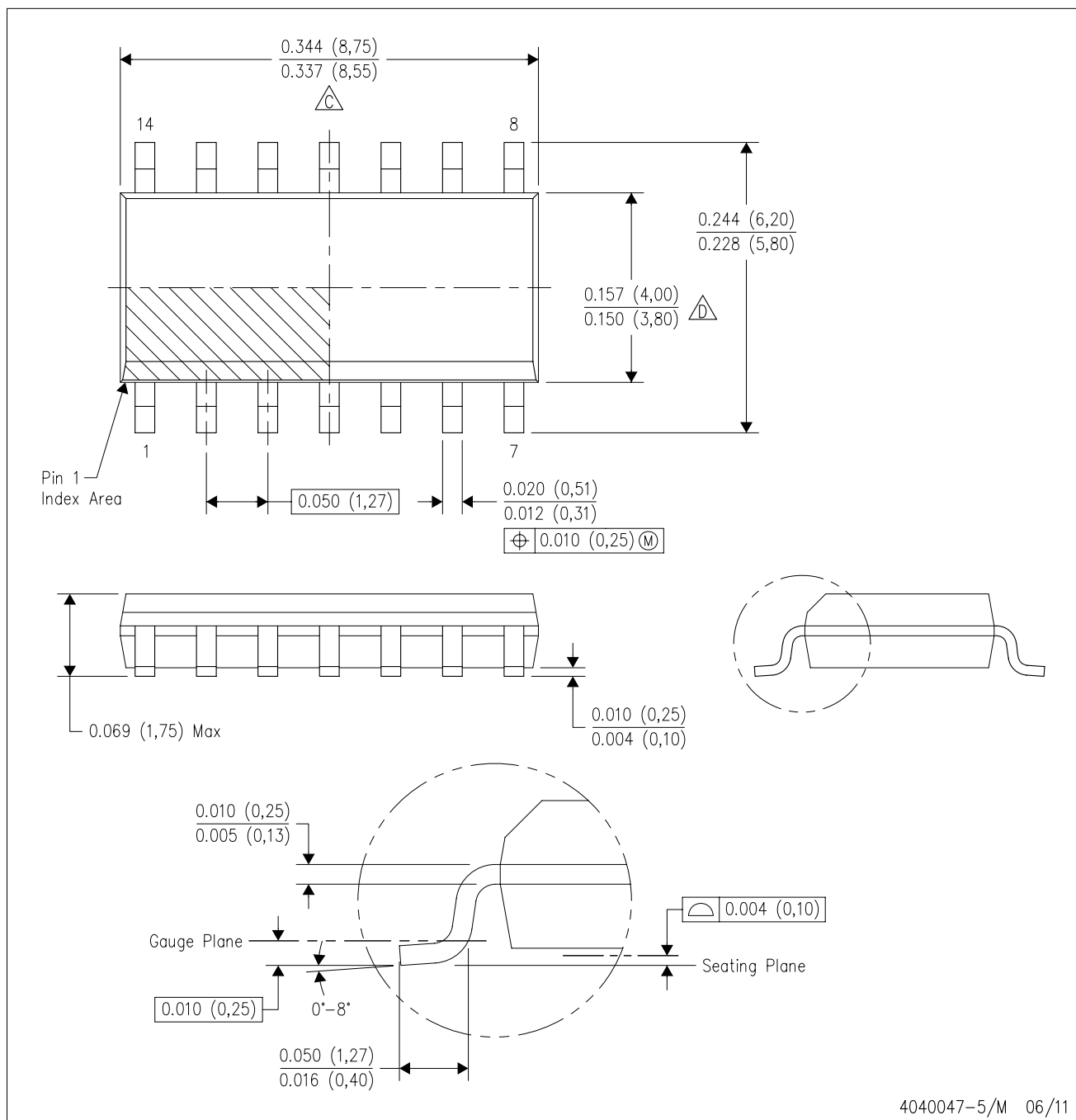


4073272/C 02/04

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation BA.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



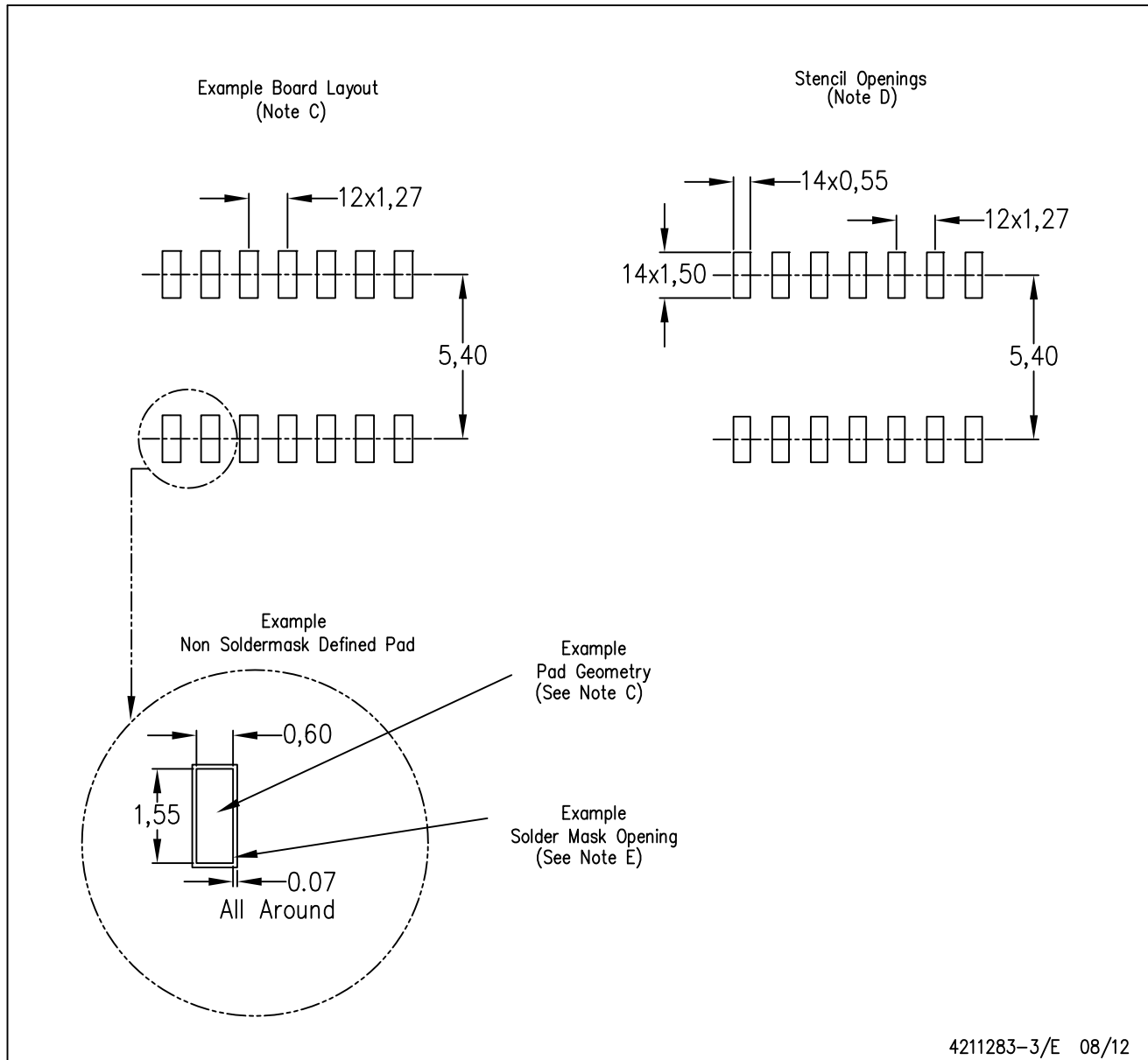
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

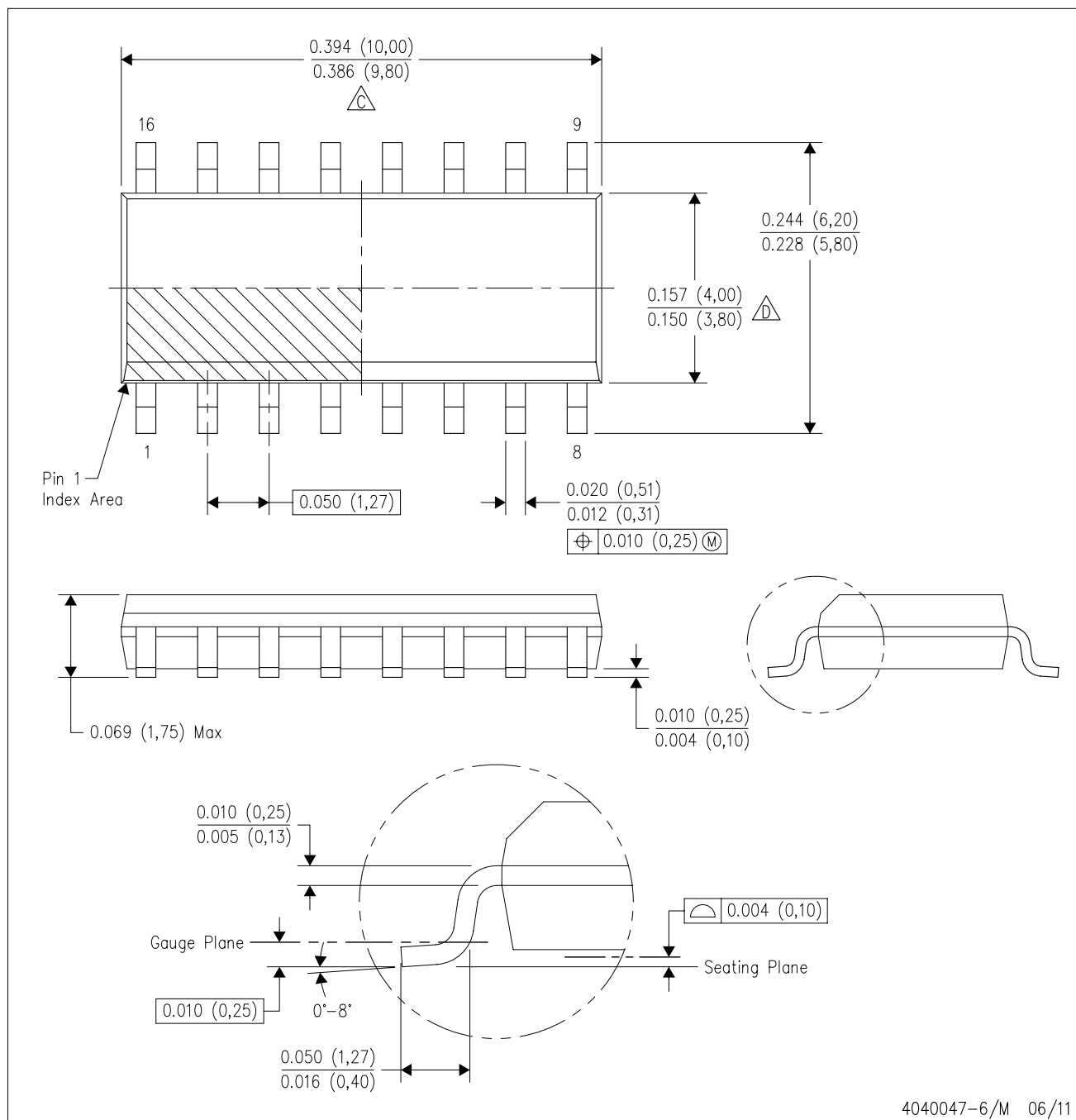
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G16)

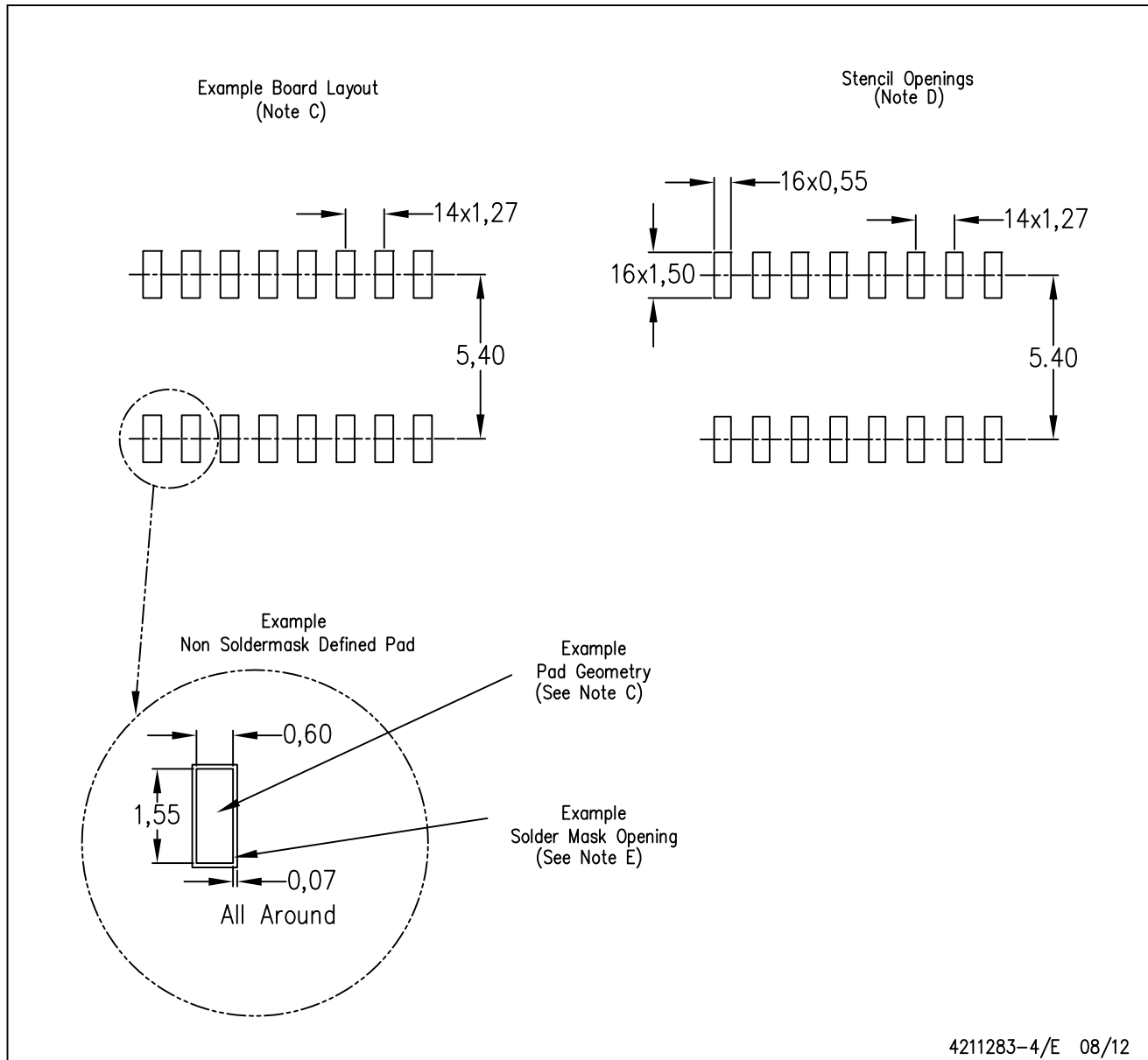
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

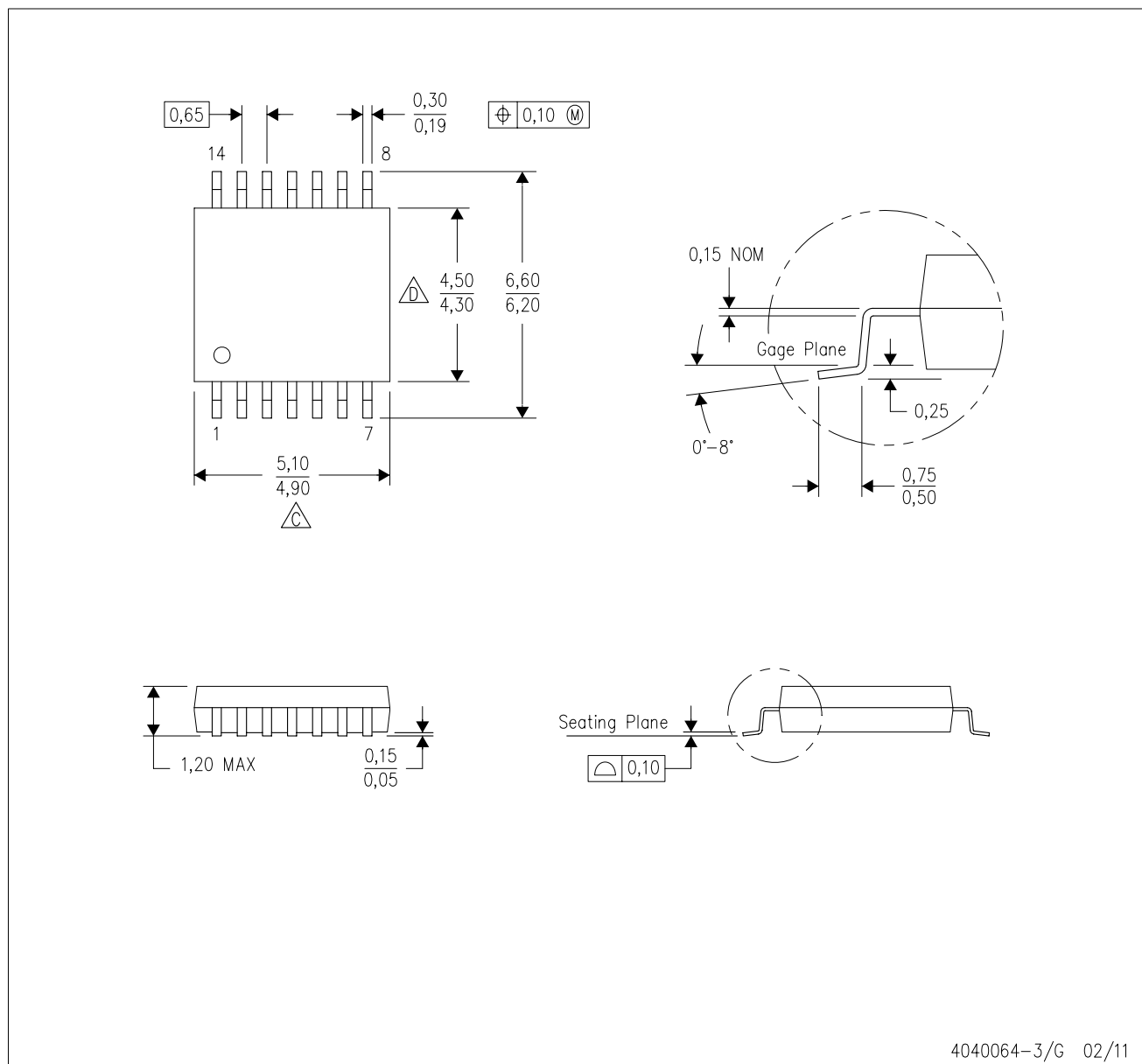
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

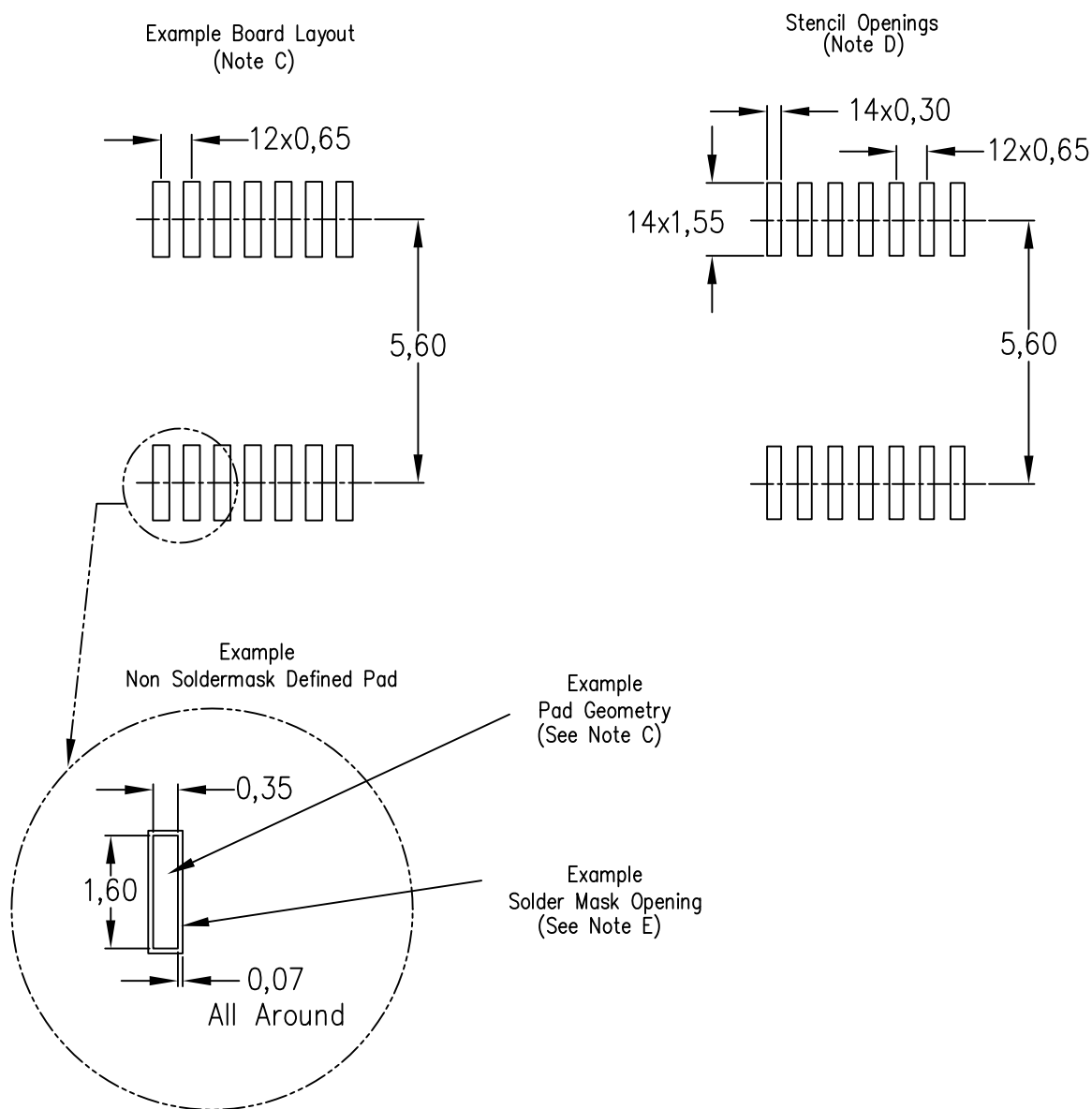
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

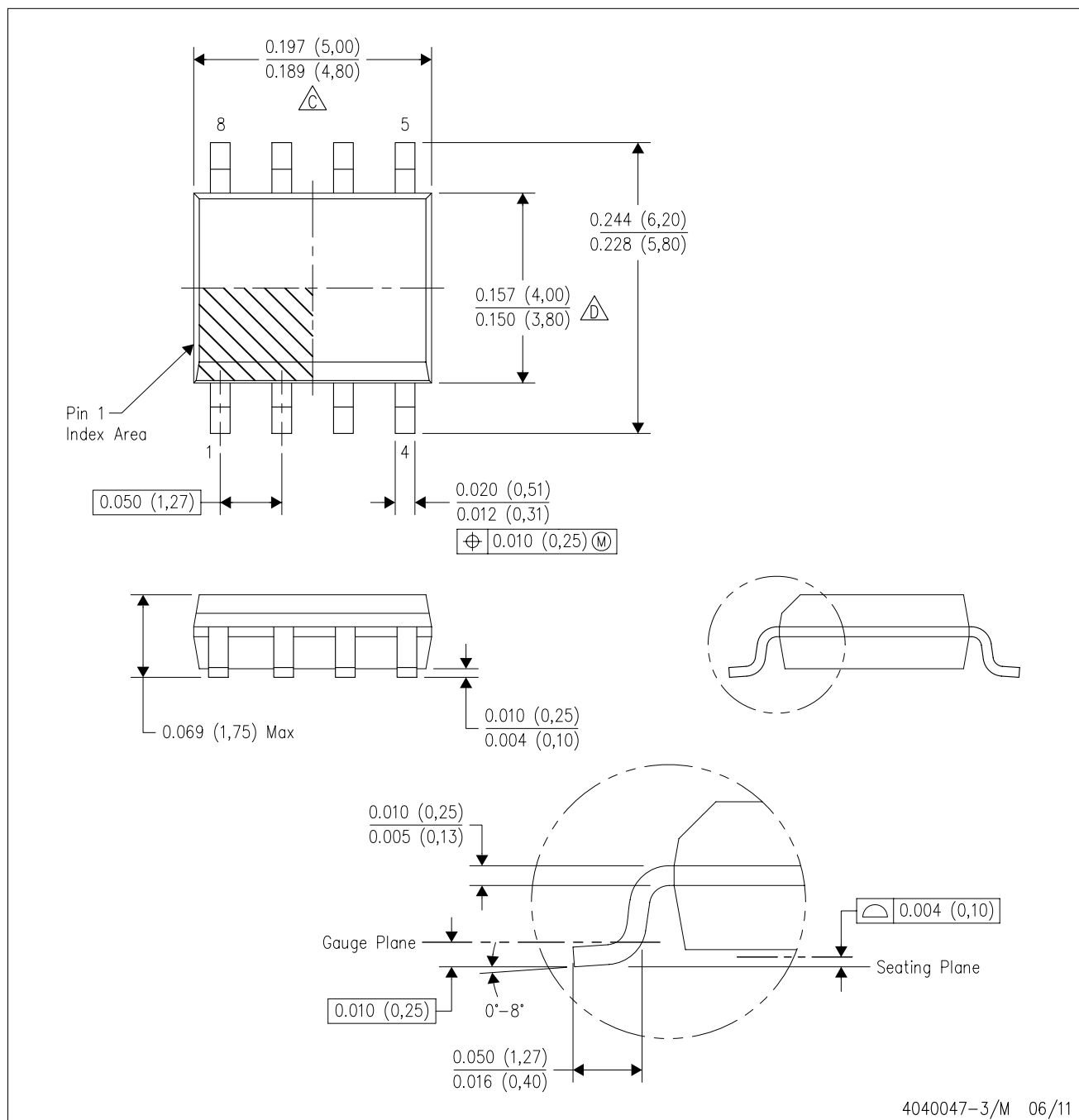


4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

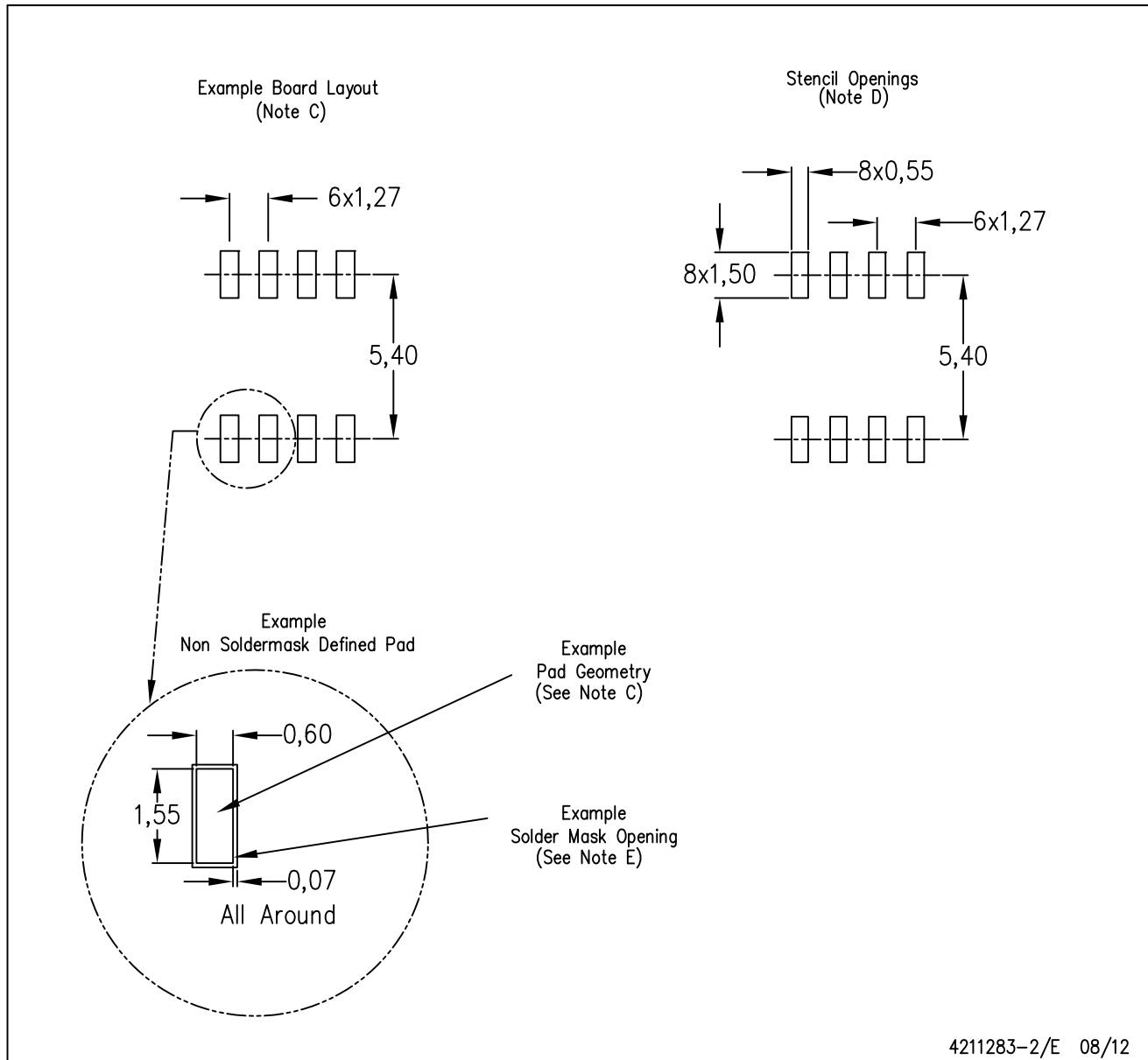
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com