

ZVS Full Bridge PWM Controller

ISL6551

The [ISL6551](#) is a zero voltage switching (ZVS) full-bridge PWM controller designed for isolated power systems. This part implements a unique control algorithm for fixed-frequency ZVS current mode control, yielding high efficiency with low EMI. The two lower drivers are PWM controlled on the trailing edge and employ resonant delay while the two upper drivers are driven at a fixed 50% duty cycle.

This IC integrates many features in 28 Ld SOIC package to yield a complete and sophisticated power supply solution. Control features include programmable soft-start for controlled start-up, programmable resonant delay for zero voltage switching, programmable leading edge blanking to prevent false triggering of the PWM comparator due to the leading edge spike of the current ramp, adjustable ramp for slope compensation, drive signals for implementing synchronous rectification in high output current, ultra high efficiency applications and current share support for paralleling up to 10 units, which helps achieve higher reliability and availability as well as better thermal management. Protective features include adjustable cycle-by-cycle peak current limiting for overcurrent protection, fast short-circuit protection (in hiccup mode), a latching shutdown input to turn off the IC completely on output overvoltage conditions or other extreme and undesirable faults, a non-latching enable input to accept an enable command when monitoring the input voltage and thermal condition of a converter and V_{DD} undervoltage lockout with hysteresis. Additionally, the ISL6551 includes high current high-side and low-side totem-pole drivers to avoid additional external drivers for moderate gate capacitance (up to 1.6nF at 1MHz) applications, an uncommitted high bandwidth (10MHz) error amplifier for feedback loop compensation, a precision bandgap reference with $\pm 1.5\%$ (ISL6551AB) or $\pm 1\%$ (ISL6551IB) tolerance across recommended operating conditions and a $\pm 5\%$ “in regulation” monitor.

In addition to the ISL6551, other external elements such as transformers, pulse transformers, capacitors, inductors and Schottky or synchronous rectifiers are required for a complete power supply solution. A detailed 200W telecom power supply reference design using the ISL6551 with companion Intersil ICs, Supervisor and Monitor ISL6550, and Half-bridge Driver HIP2100, is presented in application note [AN1002](#).

In addition, the ISL6551 can also be designed in push-pull converters using all of the features except the two upper drivers and adjustable resonant delay features.

Features

- High speed PWM (up to 1MHz) for ZVS full bridge control
- Current mode control compatible
- High current high-side and low-side totem-pole drivers
- Adjustable resonant delay for ZVS
- 10MHz error amplifier bandwidth
- Programmable soft-start
- Precision bandgap reference
- Latching shutdown input
- Non-latching enable input
- Adjustable leading edge blanking
- Adjustable dead time control
- Adjustable ramp for slope compensation
- Fast short-circuit protection (hiccup mode)
- Adjustable cycle-by-cycle peak current limiting
- Drive signals to implement synchronous rectification
- VDD undervoltage lockout
- Current share support
- $\pm 5\%$ “in regulation” indication
- Pb-free (RoHS compliant)

Applications

- Full-bridge and push-pull converters
- Power supplies for off-line and Telecom/Datacom
- Power supplies for high end microprocessors and servers

Related Literature

- [AN1002](#), 200W, 470kHz, Telecom Power Supply Using ISL6551 Full-Bridge Controller and ISL6550 Supervisor and Monitor.

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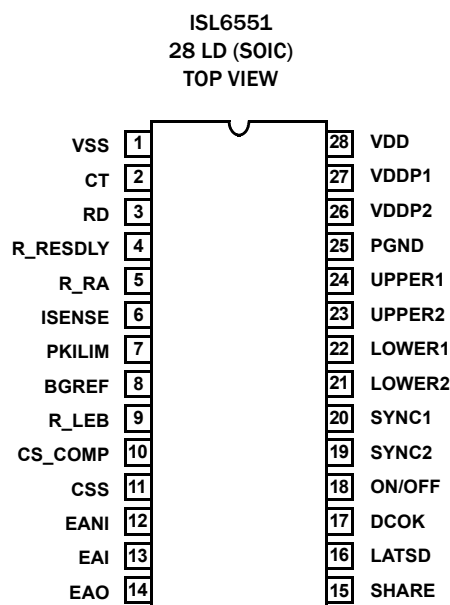
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL6551IBZ	ISL6551IBZ	0 to +85	28 Ld SOIC	M28.3
ISL6551ABZ	ISL6551ABZ	-40 to +105	28 Ld SOIC	M28.3

NOTES:

1. Add "-T" suffix for tape and reel.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for [ISL6551](#). For more information on MSL, please see tech brief [TB363](#).

Pin Configuration



Functional Pin Description

PIN #	PIN NAME	DESCRIPTION
1	VSS	Reference ground. All control circuits are referenced to this pin.
2	CT	Set the oscillator frequency, up to 1MHz.
3	RD	Adjust the clock dead time from 50ns to 1000ns.
4	R_RESPLY	Program the resonant delay from 50ns to 500ns.
5	R_RA	Adjust the ramp for slope compensation (from 50mV to 250mV).
6	ISENSE	The pin receives the current information via a current sense transformer or a power resistor.
7	PKILIM	Set the overcurrent limit with the bandgap reference as the trip threshold.
8	BGREF	Precision bandgap reference, 1.263V $\pm$ 2% overall recommended operating conditions.
9	R_LEB	Program the leading edge blanking from 50ns to 300ns.
10	CS_COMP	Set a low current sharing loop bandwidth with a capacitor.
11	CSS	Program the rise time and the clamping voltage with a capacitor and a resistor, respectively.
12	EANI	Noninverting input of Error Amp. It is clamped by the voltage at the CSS pin (Vclamp).
13	EAI	Inverting input of error amp. It receives the feedback voltage.
14	EA0	Output of error amp. It is clamped by the voltage at the CSS pin (Vclamp).
15	SHARE	This pin is the SHARE BUS connecting with other unit(s) for current share operation.
16	LATSD	The IC is latched off with a voltage greater than 3V at this pin and is reset by recycling VDD.
17	DCOK	Power-good indication with a $\pm$ 5% window.
18	ON/OFF	This is an Enable pin that controls the states of all drive signals and the soft-start.
19, 20	SYNC2, SYNC1	These are the gate control signals for the output synchronous rectifiers.
21, 22	LOWER2, LOWER1	Both lower drivers are PWM controlled on the trailing edge.
23, 24	UPPER2, UPPER1	Both upper drivers are driven at a fixed 50% duty cycle.
25	PGND	Power ground. High current return paths for both the upper and the lower drivers.
26, 27	VDDP2, VDDP1	Power is delivered to both the upper and the lower drivers through these pins.
28	VDD	Power is delivered to all control circuits including SYNC1 and SYNC2 via this pin.

Functional Block Diagram

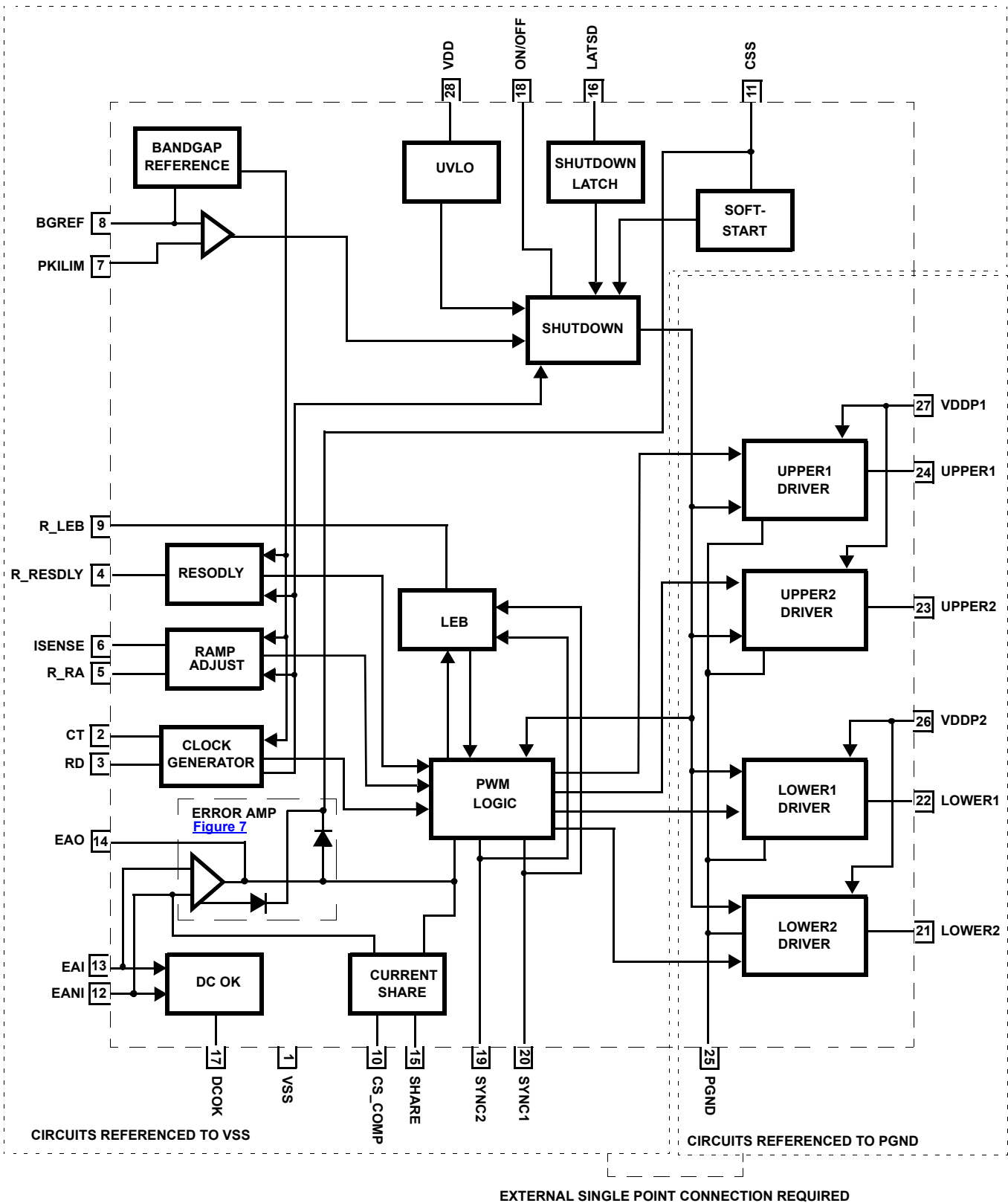


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

ISL6551

Absolute Maximum Ratings

Supply Voltage VDD, VDDP1, VDDP2	-0.3 to 16V
Enable Inputs (ON/OFF, LATSD)	VDD
Power Good Sink Current (IDCOK)	5mA
ESD Rating	
Human Body Model (Per MIL-STD-883 Method 3015.7)	3kV
Machine Model (Per EIAJ ED-4701 Method C-111)	250V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 4)	55	N/A
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Pb-free Reflow Profile	see TB493	

Recommended Operating Conditions

Ambient Temperature Range	
ISL6551IB	0°C to +85°C
ISL6551AB	-40°C to +105°C
Supply Voltage Range, VDD	10.8V to 13.2V
Supply Voltage Range, VDDP1 and VDDP2	<13.2V
Maximum Operating Junction Temperature	+125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.

Electrical Specifications These specifications apply for $V_{DD} = V_{DDP} = 12V$ and $T_A = 0^\circ C$ to $+85^\circ C$ (ISL6551IB) or $-40^\circ C$ to $+105^\circ C$ (ISL6551AB), Unless Otherwise Stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (VDD, VDDP1, VDDP2)						
Supply Voltage	VDD		10.8	12.0	13.2	V
Bias Current from VDD (ISL6551IB)	IDD	$V_{DD} = 12V$ (not including drivers current at VDDP)	5	13	18	mA
Bias Current from VDD (ISL6551AB)	IDD	$V_{DD} = 12V$ (not including drivers current at VDDP)	3		20	mA
Total Current from VDD and VDDP	ICC	$V_{DD} = V_{DDP} = 12V$, F = 1MHz, 1.6nF Load		60		mA
UNDER VOLTAGE LOCKOUT (UVLO)						
Start Threshold (ISL6551IB)	VDD _{ON}		9.2	9.6	9.9	V
Start Threshold (ISL6551AB)	VDD _{ON}		9.16		9.94	V
Stop Threshold (ISL6551IB)	VDD _{OFF}		8.03	8.6	8.87	V
Stop Threshold (ISL6551AB)	VDD _{OFF}		7.98		8.92	V
Hysteresis (ISL6551IB)	VDD _{HYS}		0.3	1	1.9	V
Hysteresis (ISL6551AB)	VDD _{HYS}		0.27		1.93	V
CLOCK GENERATOR (CT, RD)						
Frequency Range	F	$V_{DD} = 12V$ (Figure 5)	100		1000	kHz
Dead Time Pulse Width (Note 5)	DT	$V_{DD} = 12V$ (Figure 6)	50		1000	ns
BANDGAP REFERENCE (BGREF)						
Bandgap Reference Voltage (ISL6551IB)	VREF	$V_{DD} = 12V$, 399k Ω pull-up, 0.1 μF , after trimming	1.250	1.263	1.280	V
Bandgap Reference Voltage (ISL6551AB)	VREF	$V_{DD} = 12V$, 399k Ω pull-up, 0.1 μF , after trimming	1.244	1.263	1.287	V
Bandgap Reference Output Current	IREF	$V_{DD} = 12V$, see Block/Pin Functional Descriptions for details			100	μA
PWM DELAYS (Note 5)						
LOW1, 2 delay "Rising"	LOWR	With respect to RESDLY rising		5		ns
LOW1, 2 delay "Falling"	LOWF	Compare Delay at Verror = V_{ramp}		44		ns
SYNC1, 2 delay "Falling"	SYNCF	With respect to RESDLY falling and with 20pF load		18		ns
SYNC1,2 delay "Rising"	SYNCR	With respect to CLK rising and with 20pF load		20		ns

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER (EANI, EAI, EAO) (Note 5)						
Unity Gain Bandwidth	UGBW			10		MHz
DC Gain	DCG			79		dB
Maximum Offset Error Voltage	Vos				3.1	mV
Input Common Mode Range	Vcm	VDD = 12V	0.4		9	V
Common Mode Rejection Ratio	CMMR			82		dB
Power Supply Rejection Ratio	PSSR	1mA load		95		dB
Maximum Output Source Current	ISRC		2			mA
Maximum Lower Saturation Voltage	Vsatlow	Sinking 0.27mA			125	mV
RAMP ADJUST (R_RA) (Note 5)						
Ramp Frequency	F		100		1000	kHz
Linear Voltage Ramp, Minimum	LVR			50		mV
Linear Voltage Ramp, Maximum				250		mV
Overall Variation				25		%
PEAK CURRENT LIMIT (PKILIM)						
Peak Current Shutdown Threshold	IpkThr	BGREF = 0.1μF, 399kΩ pull-up	1.25	1.263	1.31	V
Peak Current Shutdown Delay (Note 5)	IpkDel			75		ns
SOFT-START (CSS)						
Charge Current	Iss	Vcss = 0.6V	8		12	μA
Discharge Current	Idis		1.6		5.2	mA
Cycle-by-cycle Current Limit (ISL6551IB)	Vclamp		2		8	V
Cycle-by-cycle Current Limit (ISL6551AB)	Vclamp		1.9		8.1	V
DRIVERS (UPPER1, UPPER2, LOWER1, LOWER2)						
Maximum Capacitive Load (each)	CL	VDD = VDDP = 12V, F = 1MHz, Thermal Dependence	1600			pF
Turn-on Rise Time (ISL6551IB)	tr	1.0nF Capacitive load		8.9	16	ns
Turn-on Rise Time (ISL6551AB)	tr	1.0nF Capacitive load		9.2	17	ns
Turn-off Fall Time (ISL6551IB)	tf	1.0nF Capacitive load		6.4	10	ns
Turn-off Fall Time (ISL6551AB)	tf	1.0nF Capacitive load			12	ns
Shutdown Delay (Note 5)	tSD	1.0nF Capacitive load		14.5		ns
Rising Edge Delay (Note 5)	tRD	1.0nF Capacitive load		16.4		ns
Falling Edge Delay (Note 5)	tFD	1.0nF Capacitive load		13.7		ns
Vsat_sourcing	Vsat_high	Sourcing 20mA			1.00	V
		Sourcing 200mA			1.35	V
Vsat_sinking (ISL6551IB)	Vsat_low	Sinking 20mA			0.035	V
		Sinking 200mA			0.31	V
Vsat_sinking (ISL6551AB)	Vsat_low	Sinking 20mA			0.04	V
		Sinking 200mA			0.5	V
SYNCHRONOUS SIGNALS (SYNC1, SYNC2)						
Maximum capacitive load (each)		VDD = 12, F = 1MHz	20			pF
PROGRAMMABLE DELAYS (RESPLY, LEB) (Note 5)						
Resonant Delay Adjust Range		(Figure 10)	50		500	ns
Resonant Delay	tRESPLY	R_RESPLY = 10k		55		ns
		R_RESPLY = 120k		488		ns

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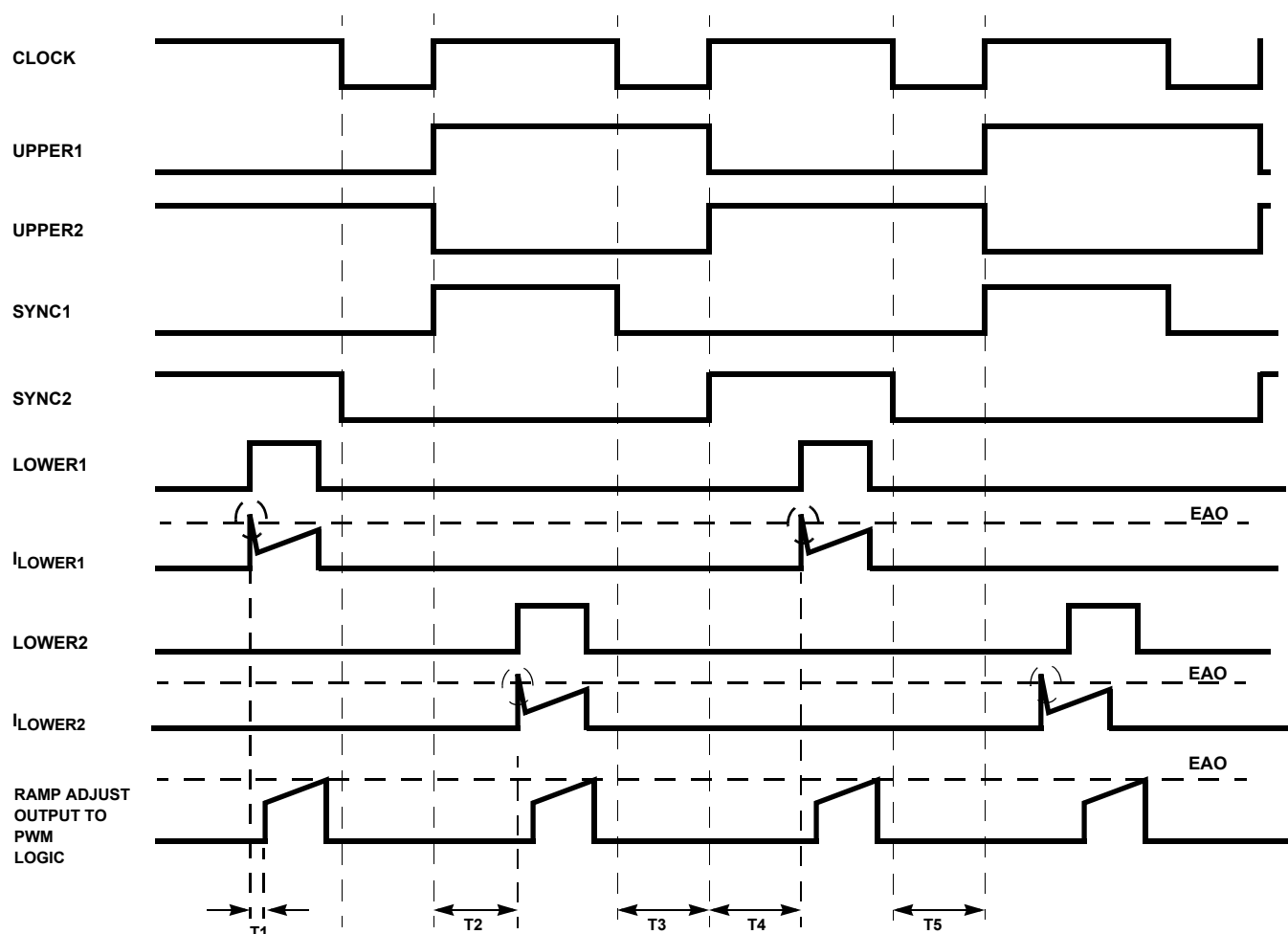
Electrical Specifications These specifications apply for $V_{DD} = V_{DDP} = 12V$ and $T_A = 0^\circ C$ to $+85^\circ C$ (ISL6551IB) or $-40^\circ C$ to $+105^\circ C$ (ISL6551AB), Unless Otherwise Stated. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Leading Edge Blanking Adjust Range		(Figure 11)	50		300	ns
Leading Edge Blanking	t _{LEB}	R_LEB = 20k		64		ns
		R_LEB = 140k		302		ns
		R_LEB = 12V		0		ns
LATCHING SHUTDOWN (LATSD)						
Fault Threshold	VIN		3			V
Fault_NOT Threshold	VINN				1.9	V
Time to Set latch (Note 5)	TSET			415		ns
ON/OFF (ON/OFF)						
Turn-off Threshold	OFF				0.8	V
Turn-on Threshold	ON		2			V
CURRENT SHARE (SHARE, CS_COMP) (Note 5)						
Voltage Offset Between Error Amp Voltage of Master and Slave	Vcs_offset	SHARE = 30k		30		mV
Maximum Source Current To External Reference	Ics_source	SHARE = 30k		190		μA
Maximum Correctable Deviation In Reference Voltage Between Master and Slave		SHARE = 30K, Rsource = 1k, OUTPUT REFERENCE = 1 to 5V, (See Figure 13)		190		mV
Share/Adjust Loop Bandwidth	CS BW	CS_COMP = 0.1μF		500		Hz
DCOK (DCOK)						
Sink Current	I _{DCOK}				5	mA
Saturation Voltage	V _{SATDCOK}	I _{DCOK} = 5mA			0.4	V
Input Reference	Vref_in		1		5	V
Threshold (relative to Vref_in)	OV	(Figure 14)		5		%
Recovery (relative to Vref_in)	OV	(Figure 14)		3		%
Threshold (relative to Vref_in)	UV	(Figure 14)		-5		%
Recovery (relative to Vref_in)	UV	(Figure 14)		-3		%
Transient Rejection (Note 5)	T _{Rej}	100mV transient on Vout (system implicit rejection and feedback network dependence (Figure 15))		250		μs

NOTE:

5. Established by design. Not 100% tested in production.

Drive Signals Timing Diagrams



NOTES:

t_1 = Leading edge blanking

$t_2 = t_4$ = Resonant delay

$t_3 = t_5$ = dead time

In the above figure, the values for t_1 through t_5 are exaggerated for demonstration purposes.

FIGURE 2. DRIVE SIGNALS TIMING DIAGRAMS

Timing Diagram Descriptions

The two upper drivers (UPPER1 and UPPER2) are driven at a fixed 50% duty cycle and the two lower drivers (LOWER1 and LOWER2) are PWM controlled on the trailing edge, while the leading edge employs resonant delay (t_2 and t_4). In current mode control, the sensed switch (FET) current (I_{LOWER1} and I_{LOWER2}) is processed in the Ramp Adjust and Leading Edge Blanking (LEB) circuits and then compared to a control signal (EAO). Spikes, due to parasitic elements in the bridge circuit, would falsely trigger the comparator generating the PWM signal. To prevent false triggering, the leading edge of the sensed current signal is blanked out by t_1 , which can be programmed at the R_LEB pin with a resistor. Internal switches gate the analog input to the PWM comparator, implementing the blanking function that eliminates response degrading delays

which would be caused if filtering of the current feedback was incorporated. The dead time (t_3 and t_5) is the delay to turn on the upper FET (UPPER1/UPPER2) after its corresponding lower FET (LOWER1/LOWER2) is turned off when the bridge is operating at maximum duty cycle in normal conditions, or is responding to load transients or input line dipping conditions. Therefore, the upper and lower FETs that are located at the same side of the bridge can never be turned on together, which eliminates shoot-through currents. SYNC1 and SYNC2 are the gate control signals for the output synchronous rectifiers. They are biased by VDD and are capable of driving capacitive loads up to 20pF at 1MHz clock frequency (500kHz switching frequency). External drivers with high current capabilities are required to drive the synchronous rectifiers, cascading with both synchronous signals (SYNC1 and SYNC2).

Shutdown Timing Diagrams

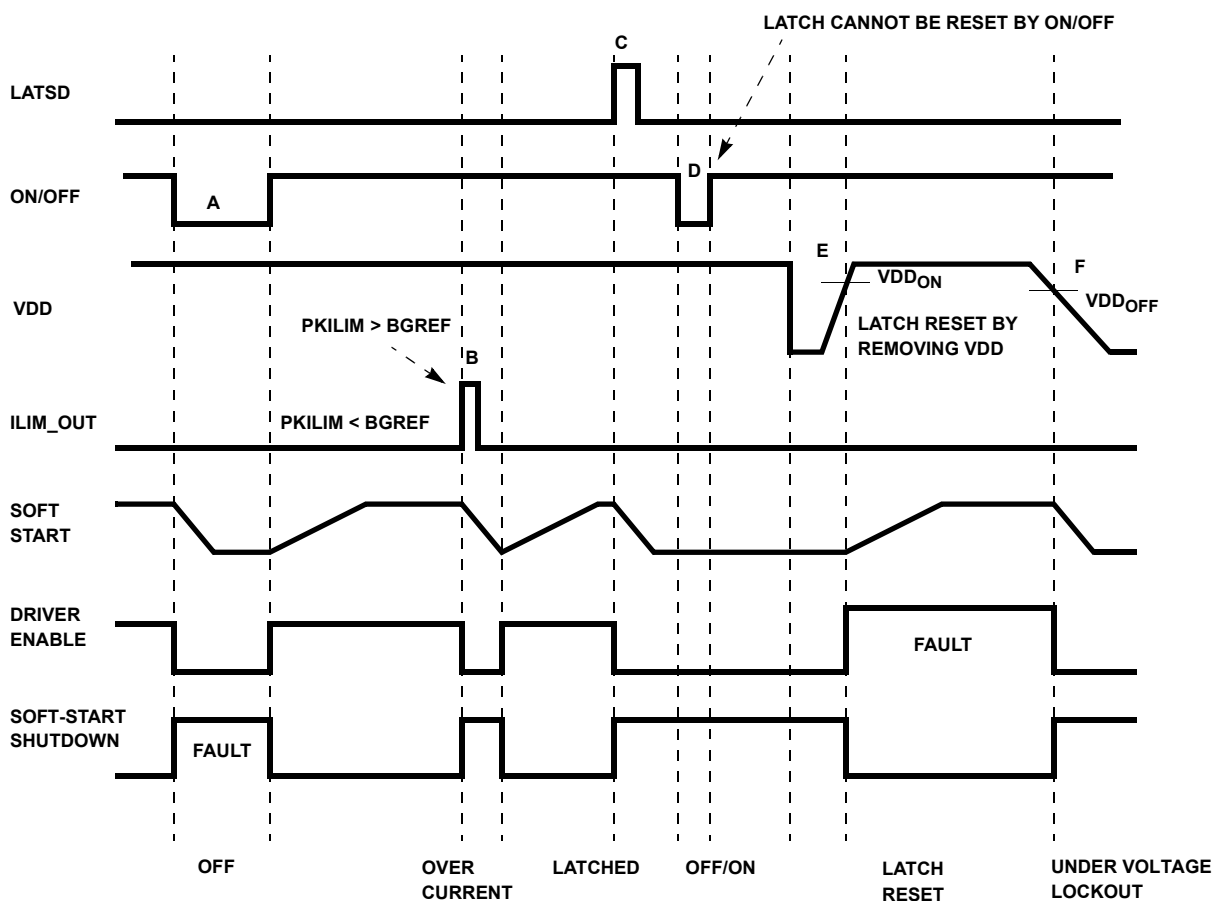


FIGURE 3. SHUTDOWN TIMING DIAGRAMS

Shutdown Timing Descriptions

A (ON/OFF) - When the ON/OFF is pulled low, the soft-start capacitor is discharged and all the drivers are disabled. When the ON/OFF is released without a fault condition, a soft-start is initiated.

B (OVERCURRENT) - If the output of the converter is over loaded, i.e., the PKILIM is above the bandgap reference voltage (BGREF), the soft-start capacitor is discharged very quickly and all the drivers are turned off. Thereafter, the soft-start capacitor is charged slowly and discharged quickly if the output is overloaded again. The soft-start will remain in hiccup mode as long as the overload conditions persist. Once the overload is removed, the soft-start capacitor is charged up and the converter is then back to normal operation.

C (LATCHING SHUTDOWN) - The IC is latched off completely as the LATSD pin is pulled high and the soft-start capacitor is reset.

D (ON/OFF) - The latch cannot be reset by the ON/OFF.

E (LATCH RESET) - The latch is reset by removing the VDD. The soft-start capacitor starts to be charged after VDD increases above the turn-on threshold VDD_{ON}.

F (VDD UVLO) - The IC is turned off when the VDD is below the turn-off threshold VDD_{OFF}. Hysteresis VDD_{HYS} is incorporated in the undervoltage lockout (UVLO) circuit.

Block/Pin Functional Descriptions

Detailed descriptions of each individual block in the functional block diagram on [page 5](#) are included in this section.

Application information and design considerations for each pin and/or each block are also included.

• IC Bias Power (VDD, VDDP1, VDDP2)

- The IC is powered from a 12V $\pm 10\%$ supply.
- VDD supplies power to both the digital and analog circuits and should be bypassed directly to the VSS pin with an 0.1 μ F low ESR ceramic capacitor.
- VDDP1 and VDDP2 are the bias supplies for the upper drivers and the lower drivers, respectively. They should be decoupled with ceramic capacitors to the PGND pin.
- Heavy copper should be attached to these pins for a better heat spreading.

• IC GNDs (VSS, PGND)

- VSS is the reference ground, the return of VDD, of all control circuits and must be kept away from nodes with switching noises. It should be connected to the PGND in only one location as close to the IC as practical. For a secondary side control system, it should be connected to the net after the output capacitors, i.e., the output return pinout(s). For a primary side control system, it should be connected to the net before the input capacitors, i.e., the input return pinout(s).
- PGND is the power return, the high-current return path of both VDDP1 and VDDP2. It should be connected to the SOURCE pins of two lower power switches or the RETURNS of external drivers as close as possible with heavy copper traces.
- Copper planes should be attached to both pins.

• Undervoltage Lockout (UVLO)

- UVLO establishes an orderly start-up and verifies that VDD is above the turn-on threshold voltage (VDD_{ON}). All the drivers are held low during the lockout. UVLO incorporates hysteresis VDD_{HYS} to prevent multiple startup/shutdowns while powering up.
- UVLO limits are not applicable to VDDP1 and VDDP2.

• Bandgap Reference (BGRF)

- The reference voltage VREF is generated by a precision bandgap circuit.
- This pin must be pulled up to VDD with a resistance of approximately 399k Ω for proper operation. For additional reference loads (no more than 1mA), this pull-up resistor should be scaled accordingly.
- This pin must also be decoupled with an 0.1 μ F low ESR ceramic capacitor.

• Clock Generator (CT, RD)

- This free-running oscillator is set by two external components as shown in [Figure 4](#). A capacitor at CT is charged and discharged by two equal constant current sources and fed into a window comparator to set the clock frequency. A resistor at RD sets the clock dead time. RD and CT should be tied to the VSS pin on their other ends as close as possible. The corresponding CT for a particular frequency can be selected from [Figure 5](#).
- The switching frequency (f_{sw}) of the power train is half of the clock frequency (F_{clock}), as shown in [Equation 1](#).

$$f_{sw} = \frac{F_{clock}}{2} \quad (EQ. 1)$$

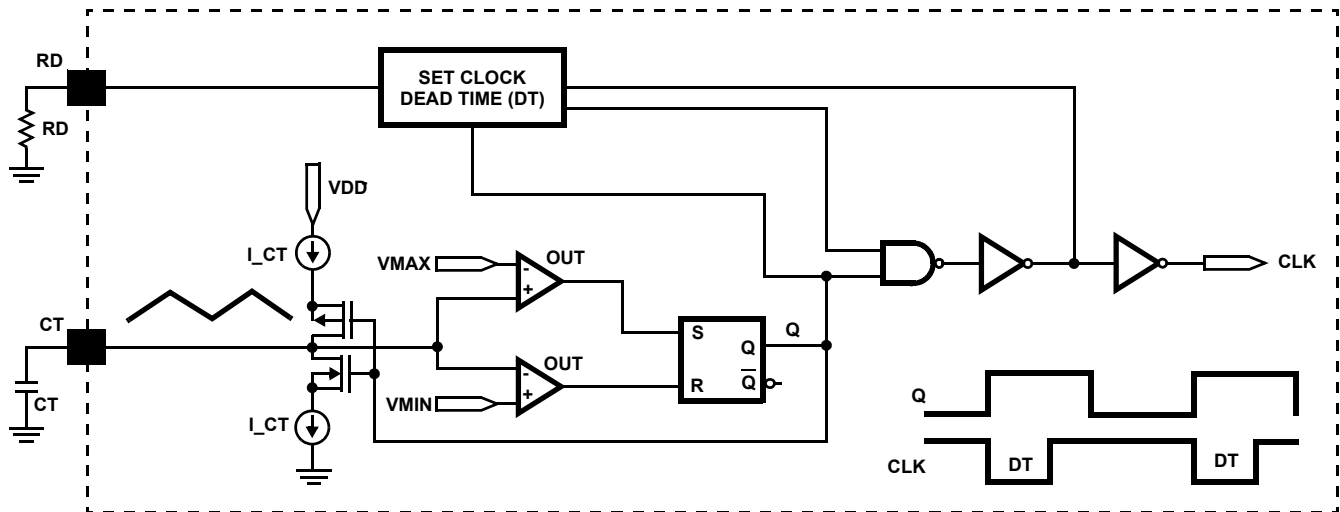


FIGURE 4. SIMPLIFIED CLOCK GENERATOR CIRCUIT

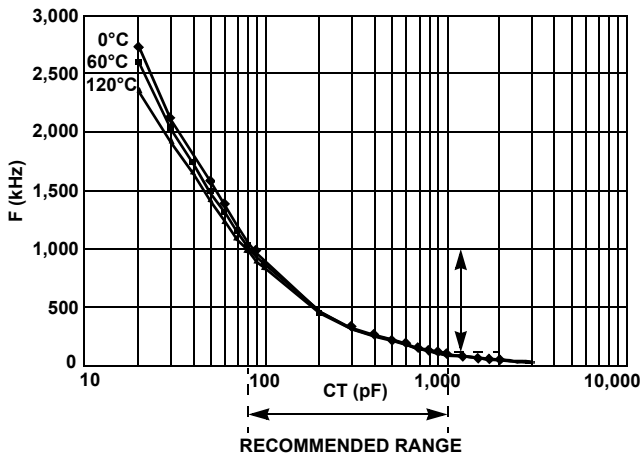


FIGURE 5. CT vs FREQUENCY

- Note that the capacitance of a scope probe (~12pF for single ended) would induce a smaller frequency at the CT pin. It can be easily seen at a higher frequency. An accurate operating frequency can be measured at the outputs of the bridge/synchronous drivers.
- The dead time is the delay to turn on the upper FET (UPPER1/UPPER2) after its corresponding lower FET (LOWER1/LOWER2) is turned off when the bridge is operating at maximum duty cycle in normal conditions, or is responding to load transients or input line dipping conditions. This helps to prevent shoot through between the upper FET and the lower FET that are located at the same side of the bridge. The dead time can be estimated using [Equation 2](#):

$$DT = \frac{M \times RD}{k\Omega} \quad (\text{ns}) \quad (\text{EQ. 2})$$

WHERE $M = 11.4$ ($VDD = 12V$), 11.1 ($VDD = 14V$) and 12 ($VDD = 10V$) and RD is in $k\Omega$. This relationship is shown in [Figure 6](#).

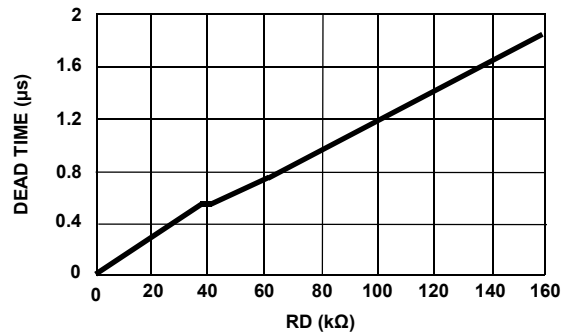


FIGURE 6. RD vs DEAD TIME ($VDD = 12V$)

• Error Amplifier (EAI, EANI, EAO)

- This amplifier compares the feedback signal received at the EAI pin to a reference signal set at the EANI pin and provides an error signal (EAO) to the PWM Logic. The feedback loop compensation can be programmed via these pins.
- Both EANI and EAO are clamped by the voltage (V_{clamp}) set at the CSS pin, as shown in [Figure 7](#). Note that the diodes in the functional block diagram represent the clamp function of the CSS in a simplified way.

• Soft-start (CSS)

- The voltage on an external capacitor charged by an internal current source I_{SS} is fed into a control pin on the error amplifier. This causes the Error Amplifier to: 1) limit the EAO to the soft-start voltage level; and 2) over ride the reference signal at the EANI with the soft-start voltage, when the EANI voltage is higher than the soft-start voltage. Thus, both the output voltage and current of the power supply can be controlled by the soft-start.
- The clamping voltage determines the cycle-by-cycle peak current limiting of the power supply. It should be set above the EANI and EAO voltages and can be programmed by an external resistor as shown in [Figure 7](#) using [Equation 3](#).

$$V_{clamp} = R_{css} \cdot I_{ss} \quad (V) \quad (\text{EQ. 3})$$

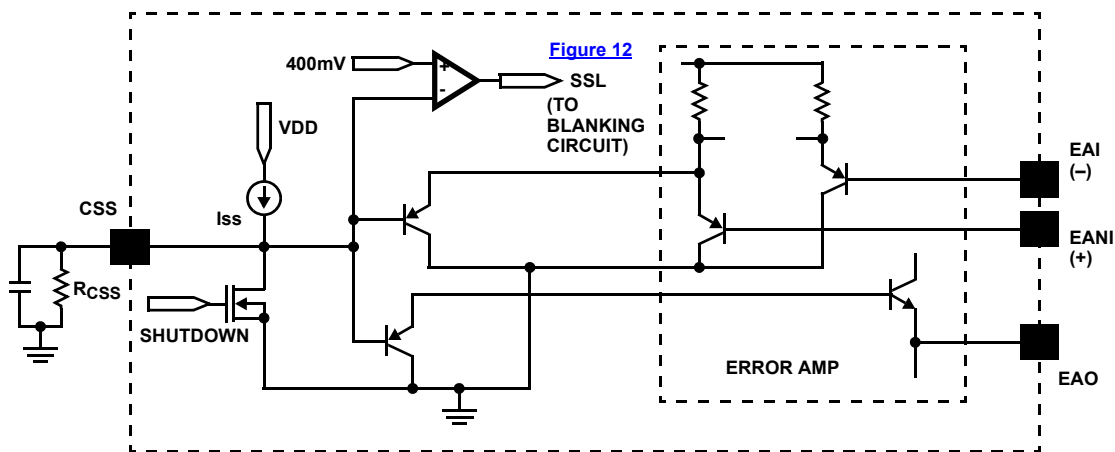


FIGURE 7. SIMPLIFIED CLAMP/SOFT-START

- Per [Equation 3](#), the clamping voltage is a function of the charge current I_{SS} . For a more predictable clamping voltage, the CSS pin can be connected to a reference-based clamp circuit as shown in [Figure 8](#). To make the V_{clamp} less dependent on the soft-start current (I_{SS}), the currents flowing through R_1 and R_2 should be scaled much greater than I_{SS} . The relationship of this circuit can be found in [Equation 4](#).

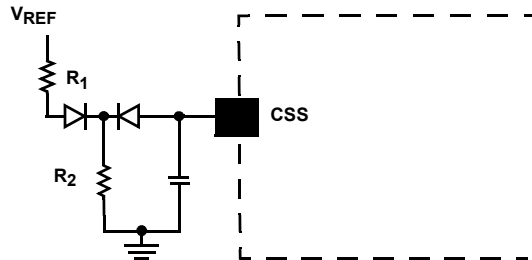


FIGURE 8. REFERENCE-BASED CLAMP CIRCUIT

$$V_{clamp} \approx I_{SS} \cdot \frac{R_1 \times R_2}{R_1 + R_2} + V_{ref} \cdot \frac{R_2}{R_1 + R_2} \quad (\text{EQ. 4})$$

- The soft-start rise time (T_{SS}) can be calculated with [Equation 5](#). The rise time (T_{rise}) of the output voltage is approximated with [Equation 6](#).

$$t_{ss} = \frac{V_{clamp} \times C_{ss}}{I_{SS}} \quad (\text{s}) \quad (\text{EQ. 5})$$

$$t_{rise} = \frac{E_{ANI} \times C_{ss}}{I_{SS}} \quad (\text{s}) \quad (\text{EQ. 6})$$

• Drivers (Upper1, Upper2, Lower1, Lower2)

- The two upper drivers are driven at a fixed 50% duty cycle and the two lower drivers are PWM controlled on the trailing edge while the leading edge employs resonant delay. They are biased by V_{DDP1} and V_{DDP2} , respectively.
- Each driver is capable of driving capacitive loads up to CL at 1MHz clock frequency and higher loads at lower frequencies on a layout with high effective thermal conductivity.
- The UVLO holds all the drivers low until the V_{DD} has reached the turn-on threshold V_{DDON} .
- The upper drivers require assistance of external level-shifting circuits such as Intersil's HIP2100 or pulse transformers to drive the upper power switches of a bridge converter.

• Peak Current Limit (PKILIM)

- When the voltage at PKILIM exceeds the BGREF voltage, the gate pulses are terminated and held low until the next clock cycle. The peak current limit circuit has a high-speed loop with propagation delay I_{pkDel} . Peak current shutdown initiates a soft-start sequence.
- The peak current shutdown threshold is usually set slightly higher than the normal cycle-by-cycle PWM peak current limit (V_{clamp}) and therefore will normally only be activated in a short-circuit condition. The limit can be set with a resistor

divider from the ISENSE pin. The resistor divider relationship is defined in [Equation 7](#).

- In general, the trip point is a little smaller than the BGREF due to the noise and/or ripple at the BGREF.

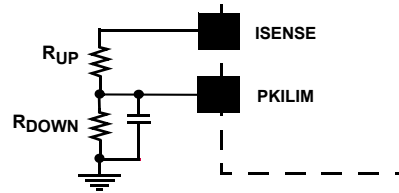


FIGURE 9. PEAK CURRENT LIMIT SET CIRCUIT

$$\frac{R_{DOWN}}{R_{DOWN} + R_{UP}} = \frac{BGREF}{ISENSE(max)} \quad (\text{EQ. 7})$$

• Latching Shutdown (LATSD)

- A high TTL level on LATSD latches the IC off. The IC goes into a low power mode and is reset only after the power at the V_{DD} pin is removed completely. The ON/OFF cannot reset the latch.
- This pin can be used to latch the power supply off on output overvoltage or other undesired conditions.

• ON/OFF (ON/OFF)

- A high standard TTL input (safe also for V_{DD} level) signals the controller to turn on. A low TTL input turns off the controller and terminates all drive signals including the SYNC outputs. The soft-start is reset.
- This pin is a non-latching input and can accept an enable command when monitoring the input voltage and the thermal condition of a converter.

• Resonant Delay (R_RESDLY)

- A resistor tied between R_RESDLY and V_{SS} determines the delay that is required to turn on a lower FET after its corresponding upper FET is turned off. This is the resonant delay, which can be estimated with [Equation 8](#).

$$t_{RESDLY} = 4.01 \times R_RESDLY / k\Omega + 13 \text{ (ns)} \quad (\text{EQ. 8})$$

- [Figure 10](#) illustrates the relationship of the value of the resistor (R_RESDLY) and the resonant delay (t_{RESDLY}). The percentages in the figure are the tolerances at the two end points of the curve.

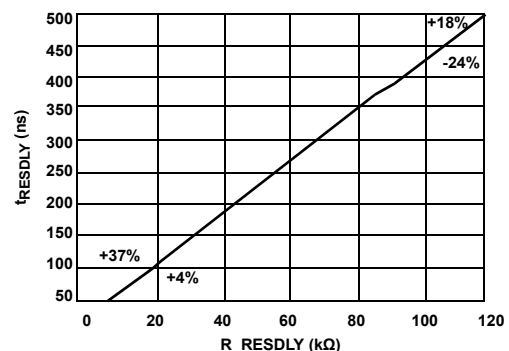


FIGURE 10. R_RESDLY vs $RESDLY$

• Leading Edge Blanking (R_LEB)

- In current mode control, the sensed switch (FET) current is processed in the Ramp Adjust and LEB circuits and then compared to a control signal (EAO voltage). Spikes, due to parasitic elements in the bridge circuit, would falsely trigger the comparator generating the PWM signal. To prevent false triggering, the leading edge of the sensed current signal is blanked out by a period that can be programmed with the R_LEB resistor. Internal switches gate the analog input to the PWM comparator, implementing the blanking function that eliminates response degrading delays, which would be caused if filtering of the current feedback was incorporated. The current ramp is blanked out during the resonant delay period because no switching occurs in the lower FETs. The leading edge blanking function will not be activated until the soft-start (CSS) reaches over 400mV, as illustrated in [Figures 7](#) and [12](#). The leading edge blanking (LEB) function can be disabled by tying the R_LEB pin to VDD, i.e., LEB = 1. Never leave the pin floating.

- The blanking time can be estimated with [Equation 9](#), whose relationship can be seen in [Figure 11](#). The percentages in the figure are the tolerances at the two endpoints of the curve.

$$t_{LEB} = 2 \times R_{LEB} / k\Omega + 15 \text{ (ns)} \quad (\text{EQ. 9})$$

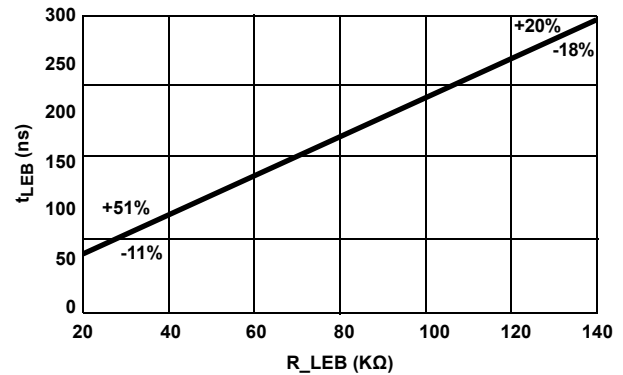


FIGURE 11. R_LEB vs t_LEB

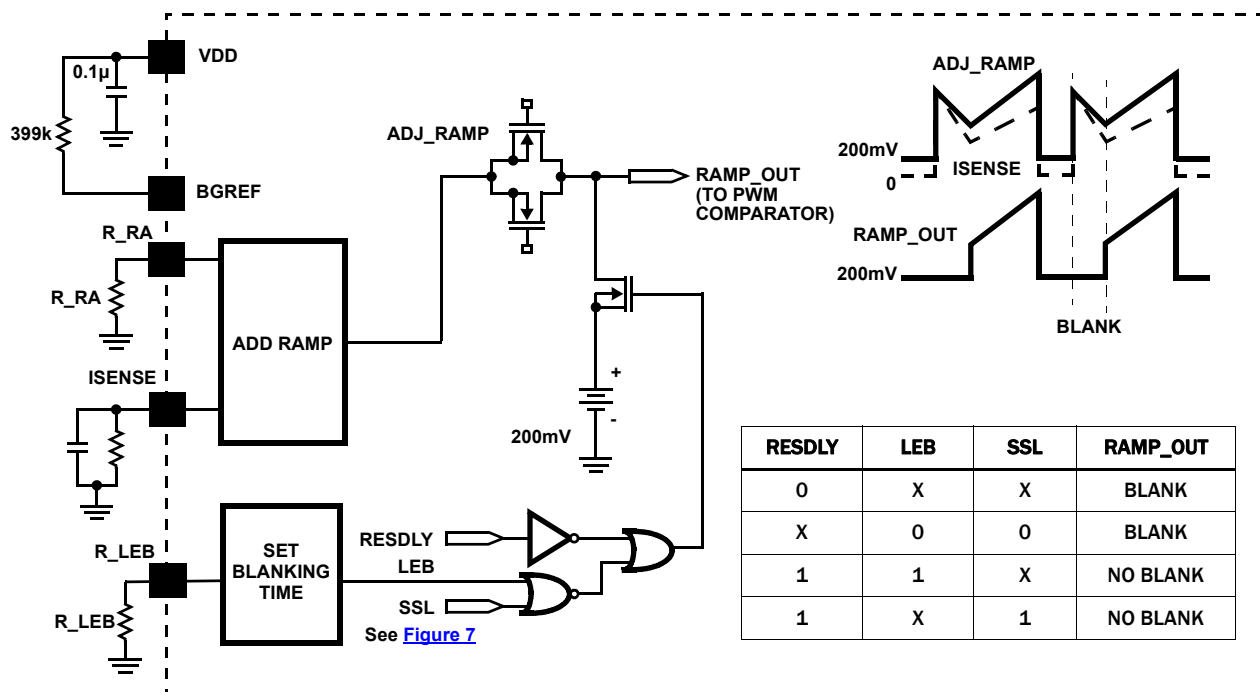


FIGURE 12. SIMPLIFIED RAMP ADJUST AND LEADING EDGE BLANKING CIRCUITS

• Ramp Adjust (R_RA, ISENSE)

- The ramp adjust block adds an offset component (200mV) and a slope adjust component to the ISENSE signal before processing it at the PWM Logic block, as shown in [Figure 12](#). This ensures that the ramp voltage is always higher than the OAGS (ground sensing opamp) minimum voltage to achieve a “zero” state.
- It is critical that the input signal to ISENSE decays to zero prior to or during the clock dead time. The level-shifting and capacitive summing circuits in the RAMP ADJUST block are reset during the dead time. Any input signal transitions that occur after the rising edge of CLK and prior to the rising edge of RESDLY can cause severe errors in the signal reaching the PWM comparator.
- Typical ramp values are hundreds of mV over the period on a 3V full scale current. Too much ramp makes the controller look like a voltage mode PWM and too little ramp leads to noise issues (jitter). The amount of ramp (V_{ramp}), as shown in [Figure 12](#), is programmed with the R_RA resistor and can be calculated with [Equation 10](#).

$$V_{ramp} = BGREF \times dt / (R_{RA} \times 500E-12) \text{ (V)} \quad (EQ. 10)$$

Where dt = Duty Cycle / f_{SW} - t_{LEB} (s). Duty cycle is discussed in detail in application note [AN1002](#).

- The voltage representation of the current flowing through the power train at ISENSE pin is normally scaled such that the desired peak current is less than or equal to $V_{clamp} - 200mV - V_{ramp}$, where the clamping voltage is set at the CSS pin.

• SYNC Outputs (SYNC1, SYNC2)

- SYNC1 and SYNC2 are the gate control signals for the output synchronous rectifiers. They are biased by V_{DD} and are capable of driving capacitive loads up to 20pF at 1MHz clock frequency (500kHz switching frequency). These outputs are turned off sooner than the turn-off at UPPER1 and UPPER2 by the clock dead time, DT.
- Inverting both SYNC signals or both LOWER signals is another possible way to control the drivers of the

synchronous rectifiers. When using these drive schemes, the user should understand the issues that might occur in his/her applications, especially the impacts on current share operation and light load operation. Refer to application note [AN1002](#) for more details.

- External high current drivers controlled by the synchronous signals are required to drive the synchronous rectifiers. A pulse transformer is required to pass the drive signals to the secondary side if the IC is used in a primary control system.

• Share Support (SHARE, CS_COMP)

- The unit with the highest reference is the master. Other units, as slaves, adjust their references via a source resistor to match the master reference sharing the load current. The source resistor is typically 1k Ω connecting the EANI pin and the OUTPUT REFERENCE (external reference or BGREF), as shown in [Figure 13](#). The share bus represents a 30k Ω resistive load per unit, up to 10 units.
- The output (ADJ) of “Operational Transconductance Amplifier (OTA)” can only pull high and it is floating while in master mode. This ensures that no current is sourced to the OUTPUT REFERENCE when the IC is working by itself.
- The slave units attempt to drive their error amplifier voltage to be within a predetermined offset (30mV typical) of the master error voltage (the share bus). The current-share error is nominally $(30mV/EAO) \times 100\%$ assuming no other source of error. With a 2.5V full load error amp voltage, the current-share error at full load would be -1.2% (slaves relative to master).
- The bandwidth of the current sharing loop should be much lower than that of the voltage loop to eliminate noise pickup and interactions between the voltage regulation loop and the current loop. A 0.1 μ F capacitor is recommended between CS_COMP and VSS pins to achieve a low current sharing loop bandwidth (100Hz to 500Hz).

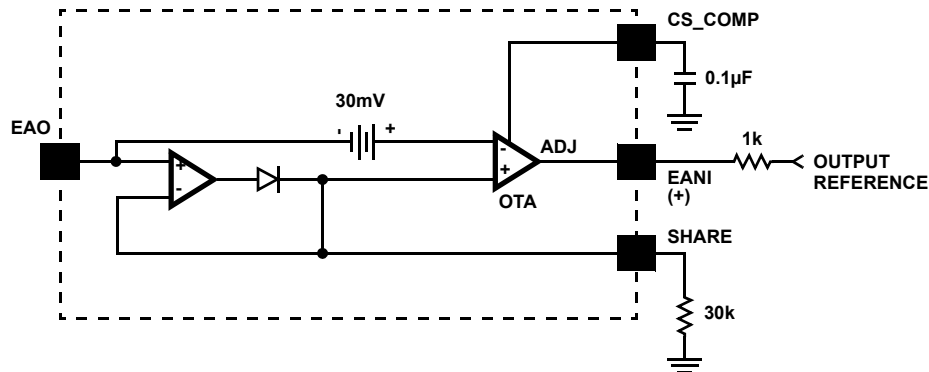


FIGURE 13. SIMPLIFIED CURRENT SHARE CIRCUIT

• Power-good (DCOK)

- DCOK pin is an open-drain output capable of sinking 5mA. It is low when the output voltage is within the UVOV window. The static regulation limit is $\pm 3\%$, while the $\pm 5\%$ is the dynamic regulation limit. It indicates power-good when the EAI is within -3% to $+5\%$ on the rising edge and within $+3\%$ to -5% on the falling edge, as shown in [Figure 14](#).

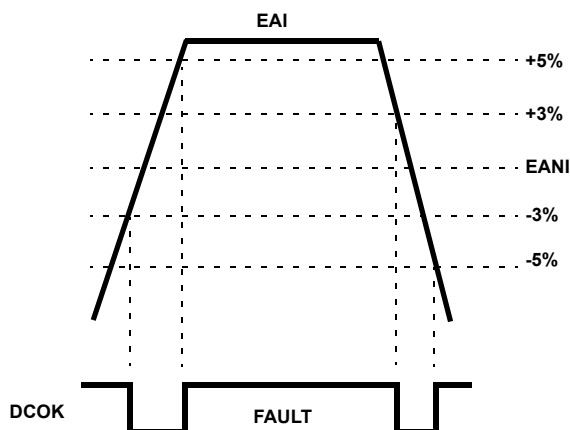


FIGURE 14. UNDERVOLTAGE-OVERVOLTAGE WINDOW

- The DCOK comparator might not be triggered even though the output voltage exceeds $\pm 5\%$ limits at load transients. This is because the feedback network of the error amplifier filters out part of the transients and the EAI only sees the remaining portion that is still within the limits, as illustrated in [Figure 15](#). The lower the “zero ($1/RC$)” of the error amplifier, the larger the portion of the transient is filtered out.

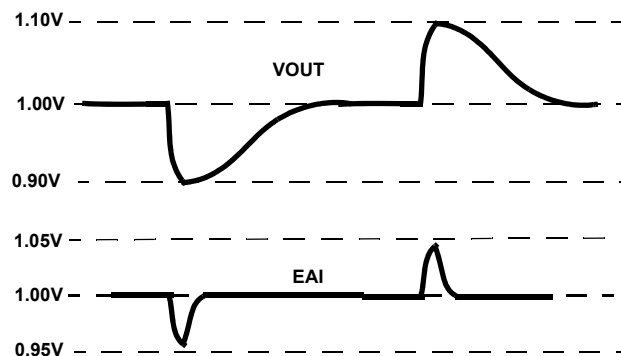
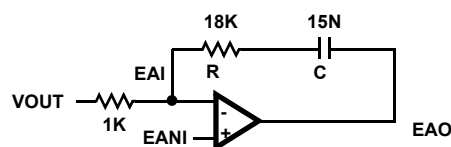


FIGURE 15. OUTPUT TRANSIENT REJECTION

Additional Applications Information

operation of the ISL6551, see Block/Pin Functional Descriptions.

[Table 1](#) highlights parameter setting for the ISL6551. Designers can use this table as a design checklist. For detailed

TABLE 1. PARAMETER SETTING HIGHLIGHTS/CHECKLIST

PARAMETER	PIN NAME	FORMULA OR SETTING HIGHLIGHT	UNIT	FIGURE #
Frequency	CT	Set 50% Duty Cycle Pulses with a fixed frequency	kHz	1, 5
Dead Time	RD	$DT = M \times RD / k\Omega$, where $M = 11.4$	ns	6
Resonant Delay	R_RESDLY	$t_{RESDLY} = 4.01 \times R_RESDLY / k\Omega + 13$	ns	10
Ramp Adjust	R_RA	$V_{ramp} = BGREF / (R_RA \times 500E-12) \times dt$	V	-
Current Sense	ISENSE	$< V_{clamp} - 200mV - V_{ramp}$	V	-
Peak Current	PKILIM	$< BGREF$ and slightly higher than V_{clamp}	V	9
Bandgap Reference	BGREF	$1.263V \pm 2\%$, 399k Ω pull-up, no more than 100 μA load	V	-
Leading Edge Blanking	R_LEB	$t_{LEB} = 2 \times R_LEB / k\Omega + 15$, never leave it floating	ns	11, 12
Current Share Compensation	CS_COMP	0.1 μ for a low current loop bandwidth (100Hz to 500Hz)	Hz	13
Soft-start and Output Rise Time	CSS	$t_{ss} = V_{clamp} \times C_{ss} / I_{ss}$, $t_{rise} = EANI \times CSS / I_{ss}$, $I_{ss} = 10\mu A \pm 20\%$	S	7
Clamp Voltage (Vclamp)	CSS	$V_{clamp} = I_{ss} \times R_{css}$, or reference based clamp	V	7, 8
Error Amplifier	EANI, EAI, EAO	$EANI, EAO < V_{clamp}$	V	-
Share Support	SHARE	30k load and a resistor (1k, typ) between EANI and OUTPUT REF.	-	-
Latching Shutdown	LATSD	Latch IC off at $> 3V$	V	-
Power-good	DCOK	$\pm 5\%$ with hysteresis, Sink up to 5mA, transient rejection	V	14, 15
IC Enable	ON/OFF	Turn-on/off at TTL level	V	-
Reference Ground	VSS	Connect to PGND in only one single point	-	-
Power Ground	PGND	Single point to VSS plane	-	-
Upper Drivers	UPPER1, UPPER2	Capacitive load up to 1.6nF at $f_{SW} = 500kHz$	-	-
Lower Drivers	LOWER1, LOWER2	Capacitive load up to 1.6nF at $f_{SW} = 500kHz$	-	-
Synchronous Drive Signals	SYNC1, SYNC2	Capacitive load up to 20pF at $f_{SW} = 500kHz$	-	-
Bias for Control Circuits	VDD	12V $\pm 10\%$, 0.1 μF decoupling capacitor	V	-
Biases for Bridge Drivers	VDDP1, VDDP2	Need decoupling capacitors	V	-

NOTE: $V_{DD} = 12V$ at room temperature, unless otherwise stated.

Figure 16 shows the block diagram of a power supply system employing the ISL6551 full bridge controller. The ISL6551 not only is a full bridge PWM controller but also can be used as a push-pull PWM controller. Users can design a power supply by selecting appropriate blocks in the “System Blocks Chart” based on the power system requirements. Figures 17A, 18A, 19A, 20A, 21A, 22A, 23, 24A, 25, 26A and 28A have been used in the

200W telecom power supply reference design, which can be found in the application note AN1002. To meet the specifications of the power supply, minor modifications of each block are required. To take full advantage of the integrated features of the ISL6551, “secondary side control” is recommended.

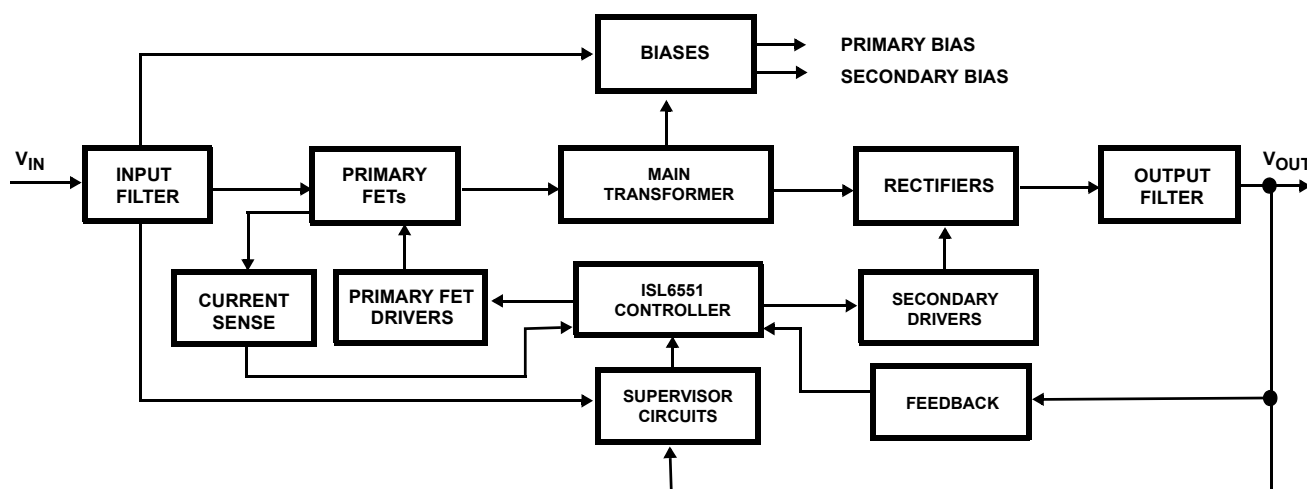


FIGURE 16. BLOCK DIAGRAM OF A POWER SUPPLY SYSTEM USING ISL6551 CONTROLLER

System Blocks Chart

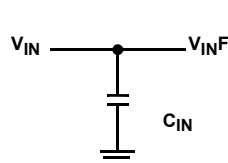


FIGURE 17A. GENERAL

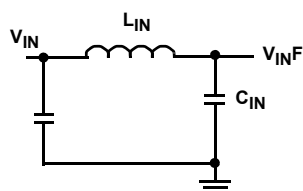


FIGURE 17B. EMI

FIGURE 17. INPUT FILTERS

General- Input capacitors are required to absorb the power switch (FET) pulsating currents.

EMI- For good EMI performance, the ripple current that is reflected back to the input line can be reduced by an input L-C filter, which filters the differential-mode noises and operates at two times the switching frequency, i.e., the clock frequency (F_{clock}). In some cases, an additional common-mode choke might be required to filter the common-mode noises.

Current Sense

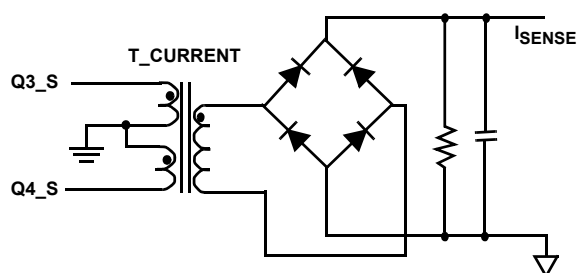


FIGURE 18A. TWO-LEG SENSE

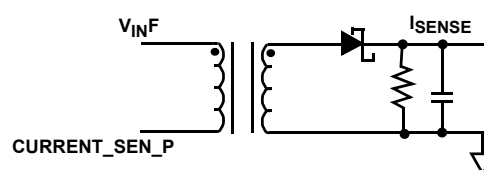


FIGURE 18B. TOP SENSE

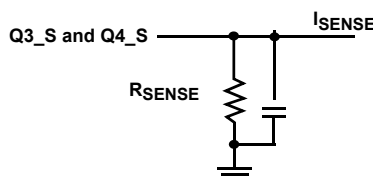


FIGURE 18C. RESISTOR SENSE (PRIMARY CONTROL)

FIGURE 18. CURRENT SENSE

Primary FETs

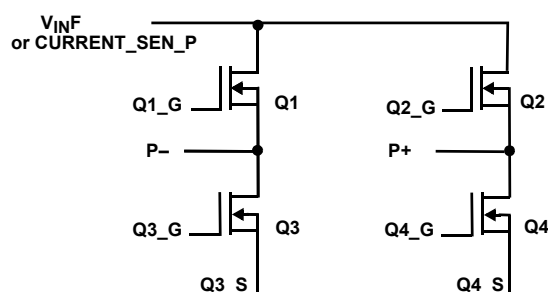


FIGURE 19A. FULL BRIDGE

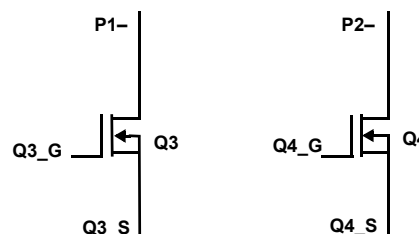


FIGURE 19B. PUSH-PULL

FIGURE 19. PRIMARY FETs

Two-leg Sense- Senses the current that flows through both lower primary FETs. Operates at the switching frequency.

Top Sense- Senses the sum of the current that flows through both upper primary FETs. Operates at the clock frequency.

Resistor Sense- This simple scheme is used in a primary side control system. The sum of the current that flows through both lower primary FETs is sensed with a low impedance power resistor. The sources of Q3 and Q4 and I_SENSE should be tied at the same point as close as possible.

BIASES

Linear Regulator- In a primary side control system, a linear regulator derived from the input line can be used for the start-up purpose and an extra winding coupled with the main transformer can provide the controller power after the start up.

DCM Flyback- Use a PWM controller to develop both primary and secondary biases with discontinuous current mode flyback topology

Full Bridge- Four MOSFETs are required for full bridge converters. The drain-to-source voltage rating of the MOSFETs is V_{IN} .

Push-pull- Only the two lower MOSFETs are required for push-pull converters. The two upper drivers are not used. The V_{DS} of the MOSFETs is $2 \times V_{IN}$.

Feedback

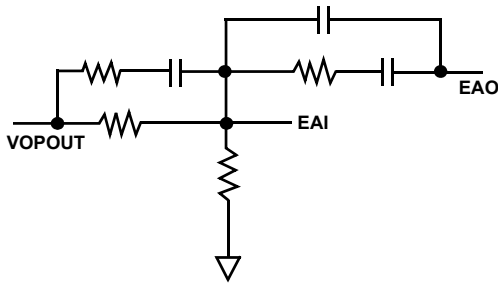


FIGURE 20A. SECONDARY CONTROL

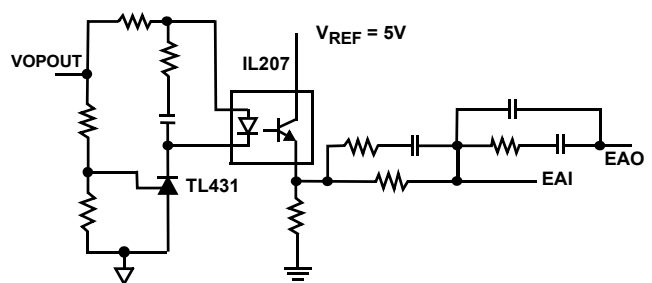


FIGURE 20B. PRIMARY CONTROL

FIGURE 20. FEEDBACK

Secondary Control- In secondary side control systems, only a few resistors and capacitors are required to complete the feedback loop.

Primary Control- This feedback loop configuration for primary side control systems requires an optocoupler for isolation. The bandwidth is limited by the optocoupler.

Rectifiers

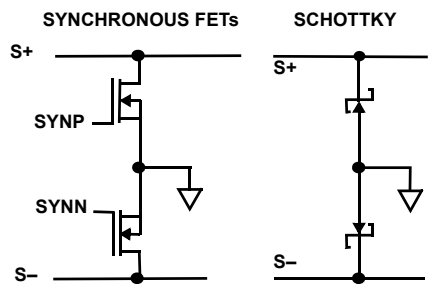


FIGURE 21A. CURRENT DOUBLER RECTIFIERS

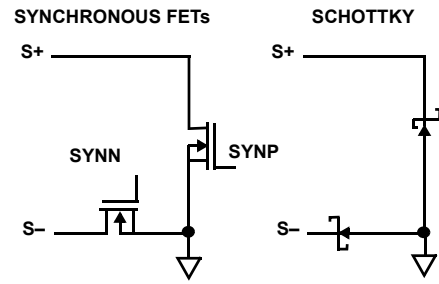


FIGURE 21B. CONVENTIONAL RECTIFIERS

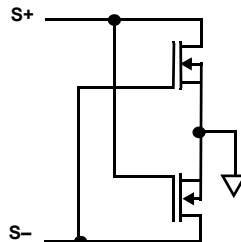


FIGURE 21C. SELF-DRIVEN RECTIFIERS

FIGURE 21. RECTIFIER

Current Doubler Rectifiers:

- Synchronous FETs are used for low output voltage, high output current and/or high efficiency applications.
- Schottky diodes are used for lower current applications. Pins S+ and S- are connected to the output filter and the main transformer with current doubler configurations.

Conventional Rectifiers:

- Synchronous FETs are used for low output voltage, high output current and/or high efficiency applications.
- Schottky diodes are used for lower current applications. Pins S+ and S- are connected to the main transformer with conventional configurations.

Self-driven Rectifiers- For low output voltage applications, both FETs can be driven by the voltage across the secondary winding. This can work with all kinds of main transformer configurations as shown in [Figures 22A through 22D](#).

Main Transformers

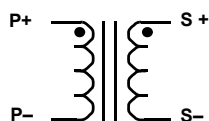


FIGURE 22A. FULL BRIDGE AND CURRENT DOUBLER

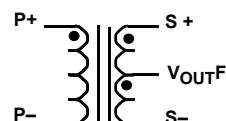


FIGURE 22B. CONVENTIONAL FULL BRIDGE

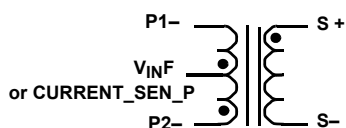


FIGURE 22C. PUSH-PULL AND CURRENT DOUBLER

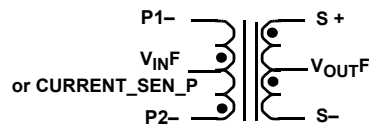


FIGURE 22D. CONVENTIONAL PUSH-PULL

FIGURE 22. MAIN TRANSFORMERS

Full Bridge and Current Doubler- No center tap is required. The secondary winding carries half of the load, i.e., only half of the load is reflected to the primary.

Conventional Full Bridge- Center tap is required on the secondary side and no center tap is required on the primary side. The secondary winding carries all the load, i.e., all the load is reflected to the primary.

Push-pull and Current Doubler- Center tap is required on the primary side and no center tap is required on the secondary side. The secondary winding carries half of the load, i.e., only half of the load is reflected to the primary.

Conventional Push-pull- Both primary and secondary sides require center taps. The secondary winding carries all the load, i.e., all the load is reflected to the primary.

Supervisor Circuits

INTEGRATED SOLUTION

- Intersil ISL6550 Supervisor And Monitor (SAM). Its QFN package requires less space than the SOIC package.
- Over-temperature protection (discrete)
- Input UV lockout (discrete)

DISCRETE SOLUTION

- Differential amplifier
- VCC undervoltage lockout
- Programmable output OV and UV
- Programmable output
- Status indicators (PGOOD and START)
- Precision reference
- Over-temperature protection
- Input UV lockout

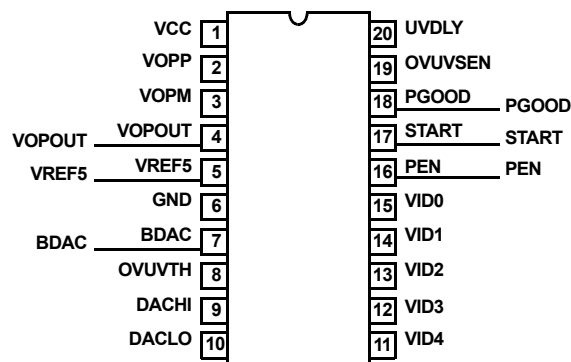


FIGURE 23. ISL6550 SOIC

The Integrated Solution- Is much simpler than a discrete solution. Over-temperature protection and input undervoltage lockout can be added for better system protection and performance.

The Discrete Solution- Requires a significant number of components to implement the features that the ISL6550 can provide.

Output Filter

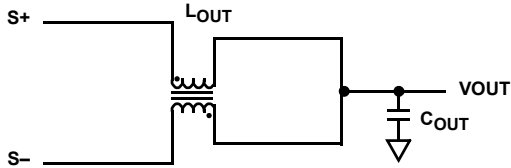


FIGURE 24A. CURRENT DOUBLER FILTER

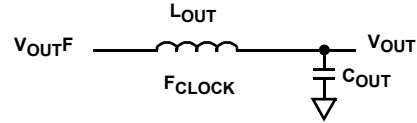


FIGURE 24B. CONVENTIONAL FILTER

FIGURE 24. OUTPUT FILTER

Current Doubler Filter- Two inductors are needed, but they can be integrated and coupled into one core. Each inductor carries half of the load operating at the switching frequency.

Conventional Filter- One inductor is needed. The inductor carries all the load operating at two times the switching frequency.

Controller

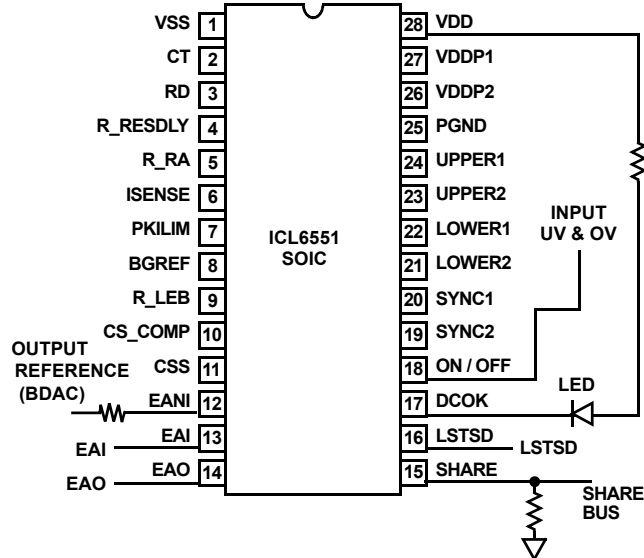


FIGURE 25. ISL6551 CONTROLLER

ISL6551 Controller- It can be used as a full bridge or push-pull PWM controller. Secondary Drivers.

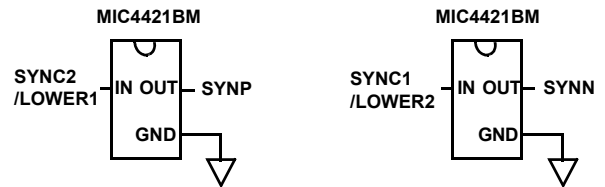
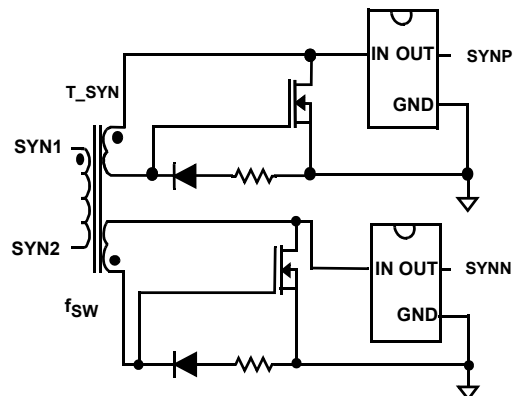


FIGURE 26A. INVERTING DRIVERS



FIGURE 26B. NONINVERTING DRIVERS



	INVERTING	NON INVERTING
SYN1	SYNC2/LOWER1	SYNC1
SYN2	SYNC1/LOWER2	SYNC2
IC	MIC4421BM	MIC4422BM

FIGURE 26C. PRIMARY CONTROL

Inverting Drivers- Inverting the SYNC signals or the LOWER signals with external high current drivers to drive the synchronous FETs.

Noninverting Drivers- Cascading SYNC signals with noninverting high current drivers to drive the synchronous FETs. There is a dead time between SYNC1 and SYNC2. For a higher efficiency, Schottky diodes are normally in parallel with the synchronous FETs to reduce the conduction losses during the dead time in high output current applications.

Primary FET Drivers

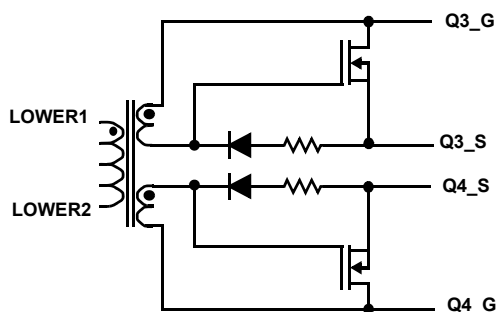


FIGURE 27A. PUSH-PULL MEDIUM CURRENT DRIVERS

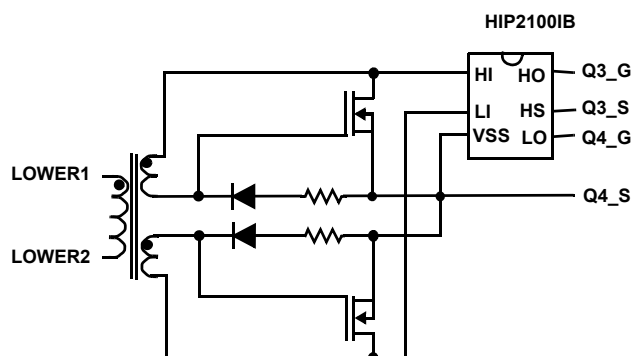


FIGURE 27B. PUSH-PULL HIGH CURRENT DRIVERS

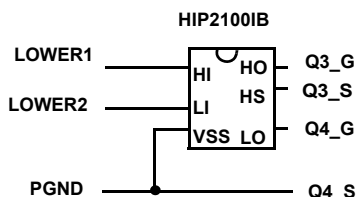


FIGURE 27C. PUSH-PULL PRIMARY CONTROL

FIGURE 27. PUSH-PULL DRIVERS

Push-pull Medium Current Drivers- Upper drivers are not used. No external drivers are required. Secondary control. Operate at the switching frequency.

Push-pull High Current Drivers- Upper drivers are not used. External high current drivers are required and less power is dissipated in the ISL6551 controller. Secondary control. Operate at the switching frequency.

Push-pull Primary Control- Upper drivers are not used. Both lower drivers can directly drive the power switches. External drivers are required in high gate capacitance applications.

Full Bridge Drivers

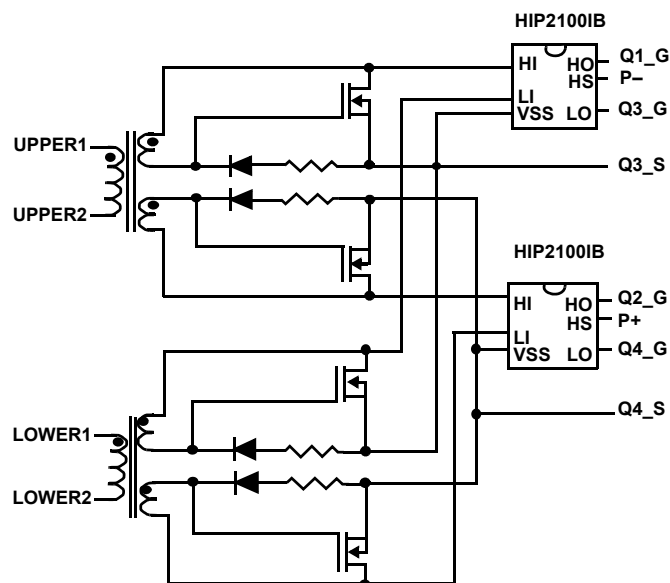


FIGURE 28A. FULL BRIDGE HIGH CURRENT DRIVERS

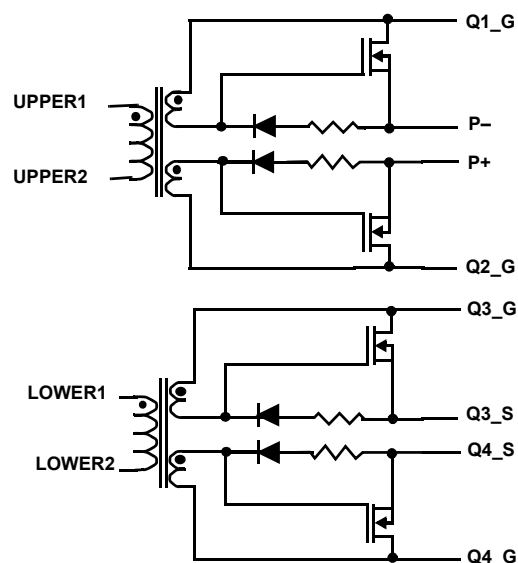


FIGURE 28B. FULL BRIDGE MEDIUM CURRENT DRIVERS

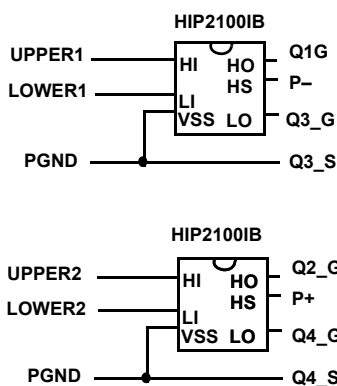


FIGURE 28C. FULL BRIDGE PRIMARY CONTROL

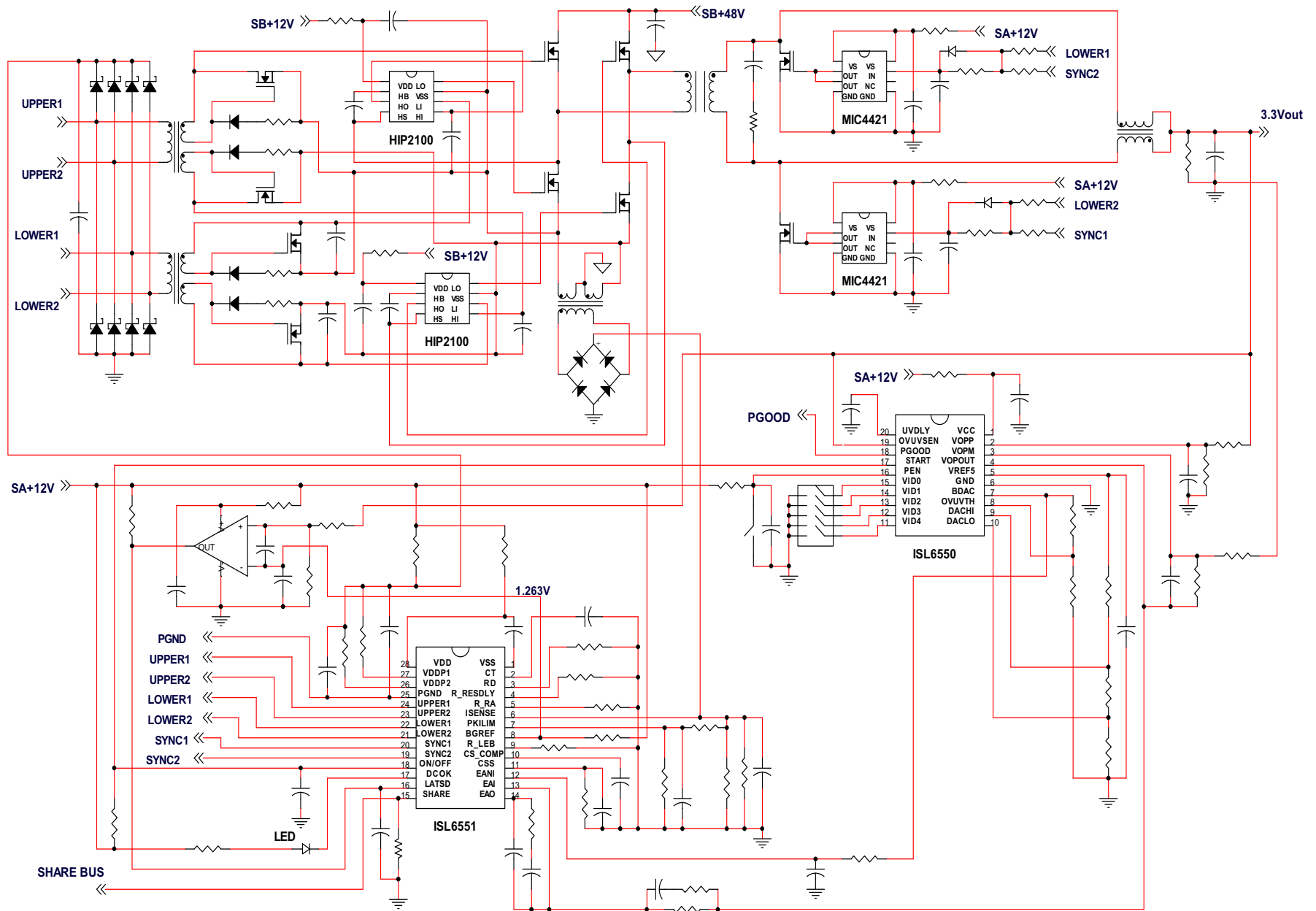
FIGURE 28. FULL BRIDGE DRIVERS

Full Bridge High Current Drivers- External high current drivers are required and less power is dissipated in the ISL6551 controller. Secondary control. Operate at the switching frequency.

Full Bridge Medium Current Drivers- No external drivers are required. Secondary control. Operate at the switching frequency.

Full Bridge Primary Control- Lower drivers can directly drive the power switches, while upper drivers require the assistance of level-shifting circuits such as a pulse transformer or Intersil's HIP2100 half-bridge driver. External high current drivers are not required in medium power applications, but level-shifting circuits are still required for upper drivers. Operate at the switching frequency.

Simplified Typical Application Schematics



Note: 200W TELECOMMUNICATION POWER SUPPLY (SEE [AN1002](#) FOR DETAILS)

ISL6551

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
April 30, 2015	FN9066.6	- Updated entire datasheet to Intersil new standard. -Removed obsolete package "QFN" throughout the datasheet. -Added Rev History and about intersil verbiage. -Updated M28.3 POD from rev 0 to rev 1 by adding land pattern.

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Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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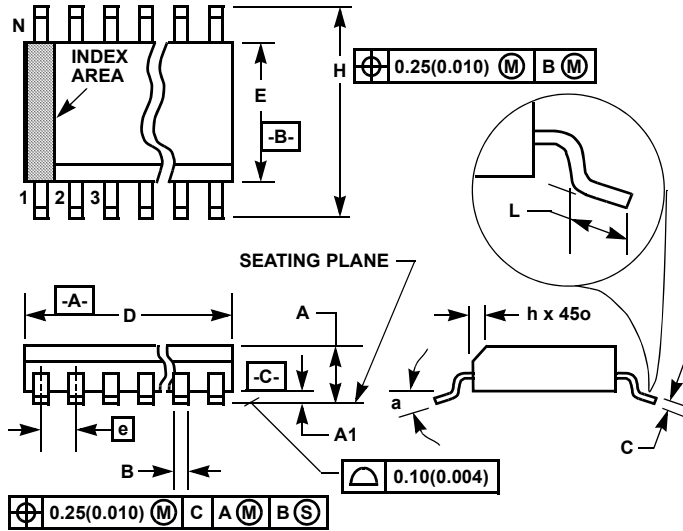
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Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C) 28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 1, 1/13

NOTES:

- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
- The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

TYPICAL RECOMMENDED LAND PATTERN

