

CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

The RCA-CD4060A consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-O's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\phi_1(\phi_0)$. All inputs and outputs are fully buffered.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

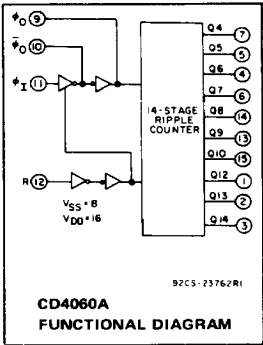
- 4-MHz operating frequency (typ.) at $V_{DD} - V_{SS} = 10\text{ V}$
- Common reset
- Fully static operation
- 10 buffered outputs available
- Quiescent current specified to 15 μA
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Oscillator Features:

- All active components on chip
- RC or crystal oscillator configuration

Applications:

- Timers
- Frequency dividers



MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})	-0.5 to +15 V
(Voltages referenced to V_{SS} Terminal)	
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to +60°C (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5\text{ V}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$. Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	VDD (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t _W f = 100 kHz	5 10	400 110	— —	500 125	— —	ns
Input-Pulse Rise & Fall Time, t _{rφ} , t _{fφ}	5 10	— —	15 7.5	— —	15 7.5	μs
Input-Pulse Frequency, f _φ	5 10	— —	1 3	— —	0.9 2.75	MHz
Reset Pulse Width, t _W	5 10	1000 500	— —	1250 600	— —	ns

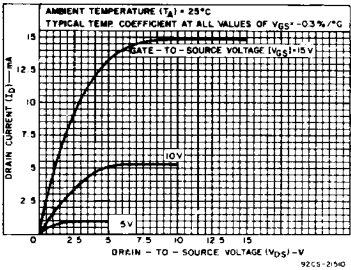


Fig. 1 — Typical n-channel drain characteristics.

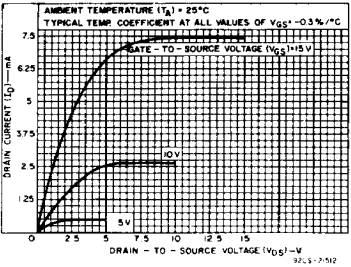


Fig. 2 — Minimum n-channel drain characteristics.

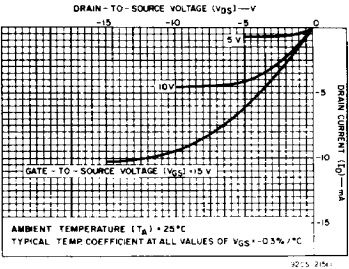


Fig. 3 — Typical p-channel drain characteristics.

CD4060A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85	
				Typ.	Limit			Typ.	Limit			
Quiescent Device Current I _L Max.	—	—	5	15	0.5	15	900	50	1	50	700	μA
	—	—	10	25	1	25	1500	100	2	100	1400	
	—	—	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage:	—	5	5	0 Typ.; 0.05 Max.								V
Low Level, V _{OL}	—	10	10	0 Typ.; 0.05 Max.								
High Level	—	0	5	4.95 Min.; 5 Typ.								V
V _{OH}	—	0	10	9.95 Min.; 10 Typ.								
Noise Immunity:	4.2	—	5	1.5 Min.; 2.25 Typ.								V
Inputs Low, V _{NL}	9	—	10	3 Min.; 4.5 Typ.								
Inputs High	0.8	—	5	1.5 Min.; 2.25 Typ.								V
V _{NH}	10	—	10	3 Min.; 4.5 Typ.								
Noise Margin:	4.5	—	5	1 Min.								V
Inputs Low, V _{NML}	9	—	10	1 Min.								
Inputs High,	0.5	—	5	1 Min.								V
V _{NMH}	1	—	10	1 Min.								
Output Drive Current: *	0.5	—	5	0.22	0.36	0.18	0.125	0.21	0.36	0.18	0.15	mA
n-Channel (Sink), I _{DN} Min.												
p-Channel (Source), I _{DP} Min.	4.5	—	5	-0.15	-0.25	-0.125	-0.085	-0.145	-0.25	-0.125	-0.1	mA
	9.5	—	10	-0.3	-0.5	-0.25	-0.175	-0.29	-0.5	-0.25	-0.2	
Input Leakage Current, I _{IL} , I _{IH}	Any Input — — 15			±10 ⁻⁵ Typ., ±1 Max.								μA

* Data not applicable to Terminal 9 or 10

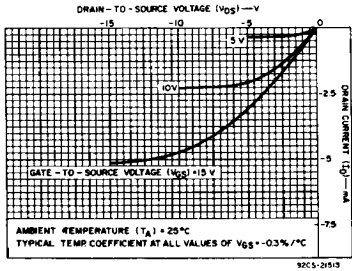


Fig. 4 - Minimum p-channel drain characteristics.

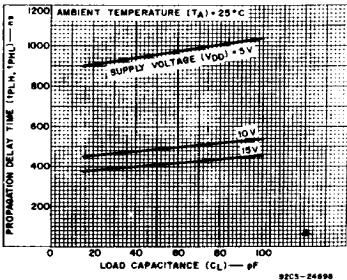


Fig. 5 - Typical propagation delay time vs. load capacitance (ϕ_1 to Q4 output).

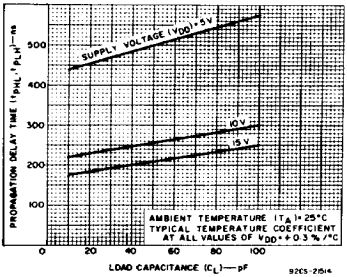


Fig. 6 - Typical propagation delay time vs. load capacitance (Q_n to Q_{n+1}).

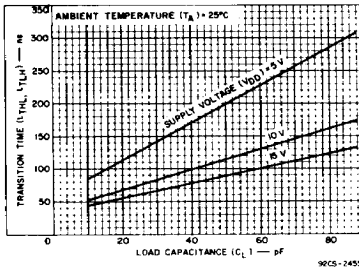


Fig. 8 - Typical output transition time vs. load capacitance.

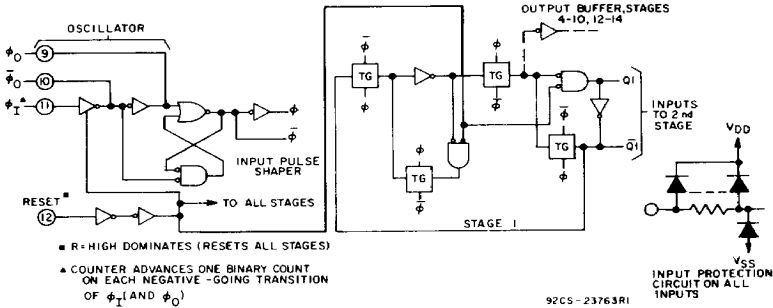


Fig. 7 - Logic diagram of CD4060A oscillator, pulse shaper, and 1 of 14 counter stages.

CD4060A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,

$C_L = 15\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS	
		D, F, K, H Packages			E Package				
		V _{DD} (V)	Min.	Typ.	Max.	Min.	Typ.		Max.
Input-Pulse Operation									
Propagation Delay Time, ϕ_1 to Q4 Out; t_{PHL} · t_{PLH}		5	—	900	1800	—	900	1900	ns
		10	—	450	900	—	450	950	
Propagation Delay Time, Q_n to Q_{n+1} ; t_{PHL} · t_{PLH}		5	—	450	900	—	450	950	ns
		10	—	225	450	—	225	475	
Transition Time, t_{THL} · t_{TLH}		5	—	150	300	—	150	350	ns
		10	—	75	150	—	75	175	
Min. Input-Pulse Width t_W	f=100 kHz	5	—	200	400	—	200	500	ns
		10	—	75	110	—	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$ · $t_{f\phi}$		5	—	—	15	—	—	15	μ s
		10	—	—	7.5	—	—	7.5	
Max. Input-Pulse Frequency, f_ϕ		5	1	1.75	—	0.9	1.75	—	MHz
		10	3	4	—	2.75	4	—	
Input Capacitance, C_i	Any Input	—	—	5	—	—	5	—	pF
Reset Operation									
Propagation Delay Time, t_{PHL}		5	—	500	1000	—	500	1250	ns
		10	—	250	500	—	250	600	
Minimum Reset Pulse Width, t_W		5	—	500	1000	—	500	1250	ns
		10	—	250	500	—	250	600	

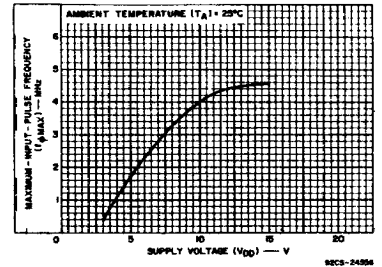


Fig. 9 – Typical maximum-input-pulse frequency vs. supply voltage.

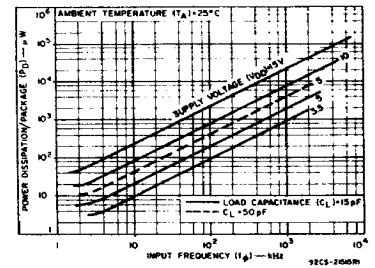


Fig. 10 – Typical dynamic power dissipation characteristics.

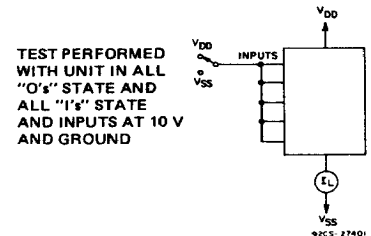


Fig. 11 – Quiescent device current test circuit.

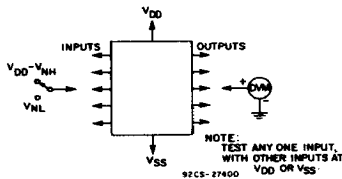


Fig. 12 – Noise-immunity test circuit.

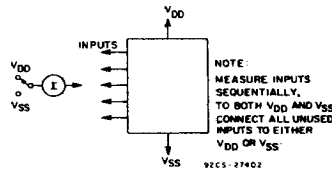


Fig. 13 – Input-leakage-current test circuit.