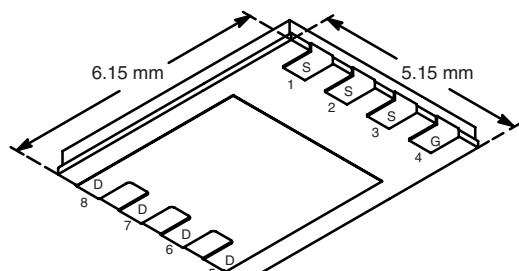


## N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
20	0.00160 at $V_{GS} = 10$ V	60	64.5 nC
	0.00175 at $V_{GS} = 4.5$ V	60	
	0.00225 at $V_{GS} = 2.5$ V	60	

PowerPAK® SO-8



Bottom View

Ordering Information: SiR404DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

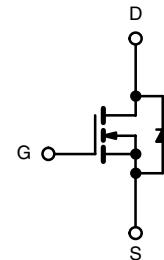
### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Gen III Power MOSFET
- 100 %  $R_g$  Tested
- 100 % UIS Tested
- 2.5 V and 3.3 V Gate Drive MOSFET for dc-to-dc Applications
- Compliant to RoHS Directive 2002/95/EC



### APPLICATIONS

- Fixed Telecom
- OR-ing
- POL



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	60 <sup>a</sup>	A
		60 <sup>a</sup>	
		45.6 <sup>b, c</sup>	
		36.6 <sup>b, c</sup>	
Pulsed Drain Current	$I_{DM}$	100	
Continuous Source-Drain Diode Current	$I_S$	60 <sup>a</sup>	
		5.6 <sup>b, c</sup>	
Single Pulse Avalanche Current	$I_{AS}$	50	
Single Pulse Avalanche Energy	$E_{AS}$	125	mJ
Maximum Power Dissipation	$P_D$	104	W
		66.6	
		6.25 <sup>b, c</sup>	
		4.0 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$R_{thJA}$	15	20	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	0.9	1.2	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$  s.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 54 °C/W.

## SiR404DP

Vishay Siliconix

**SPECIFICATIONS**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

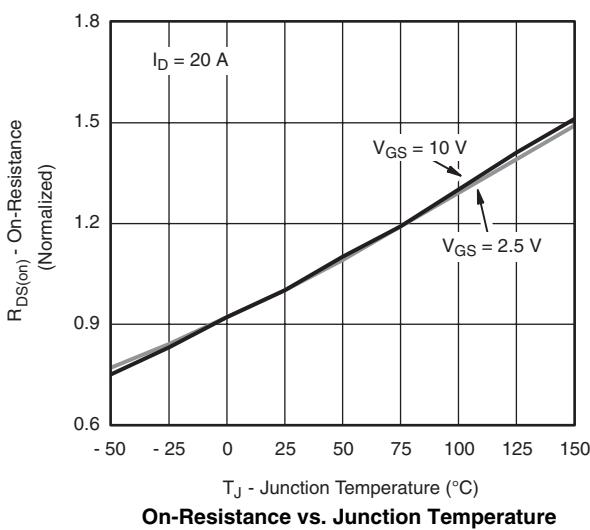
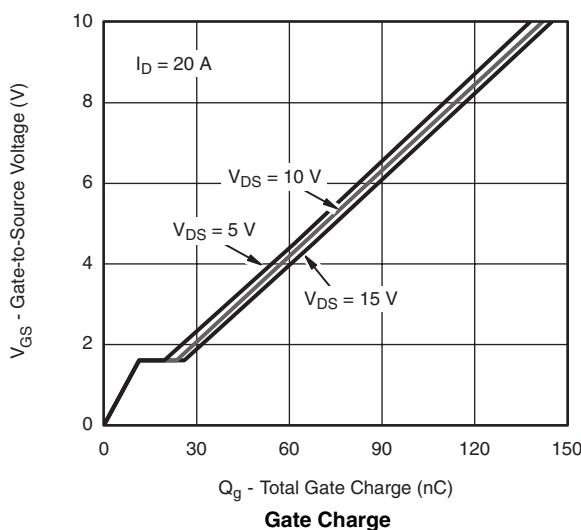
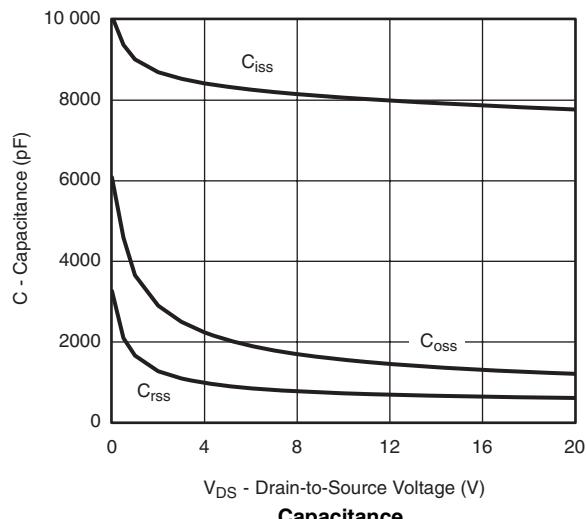
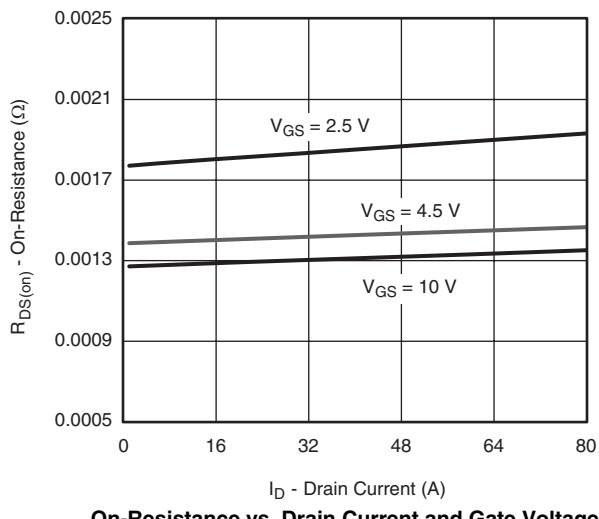
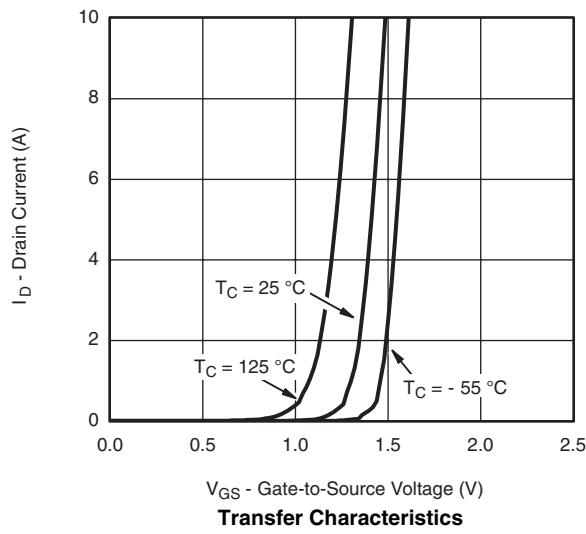
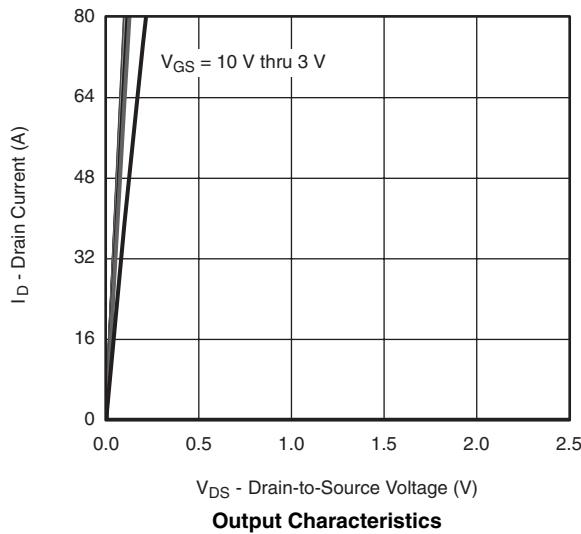
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		17		mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 4.4		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	0.6		1.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 12 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20 \text{ V}$ , $V_{GS} = 0 \text{ V}$		1		$\mu\text{A}$
		$V_{DS} = 20 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 55^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$ , $V_{GS} = 10 \text{ V}$	30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$		0.0013	0.00160	$\Omega$
		$V_{GS} = 4.5 \text{ V}$ , $I_D = 20 \text{ A}$		0.0014	0.00175	
		$V_{GS} = 2.5 \text{ V}$ , $I_D = 15 \text{ A}$		0.0018	0.00225	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$		150		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		8130		pF
Output Capacitance	$C_{oss}$			1570		
Reverse Transfer Capacitance	$C_{rss}$			735		
Total Gate Charge	$Q_g$	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 2.5 \text{ V}$ , $I_D = 20 \text{ A}$		36.5		nC
		$V_{DS} = 10 \text{ V}$ , $V_{GS} = 3.3 \text{ V}$ , $I_D = 20 \text{ A}$		47.5		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 4.5 \text{ V}$ , $I_D = 20 \text{ A}$		64.5	97	
Gate-Drain Charge	$Q_{gd}$			11.4		
Gate Resistance	$R_g$	$f = 1 \text{ MHz}$	0.2	1.0	2	$\Omega$
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 10 \text{ V}$ , $R_L = 1.0 \Omega$ $I_D \approx 10 \text{ A}$ , $V_{GEN} = 10 \text{ V}$ , $R_g = 1 \Omega$		14	28	ns
Rise Time	$t_r$			9	18	
Turn-Off Delay Time	$t_{d(\text{off})}$			68	120	
Fall Time	$t_f$			9	18	
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 10 \text{ V}$ , $R_L = 1.0 \Omega$ $I_D \approx 10 \text{ A}$ , $V_{GEN} = 4.5 \text{ V}$ , $R_g = 1 \Omega$		35	60	
Rise Time	$t_r$			20	40	
Turn-Off Delay Time	$t_{d(\text{off})}$			123	210	
Fall Time	$t_f$			26	50	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$			60	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				100	
Body Diode Voltage	$V_{SD}$	$I_S = 5 \text{ A}$		0.65	1.1	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10 \text{ A}$ , $dl/dt = 100 \text{ A}/\mu\text{s}$ , $T_J = 25^\circ\text{C}$		38	75	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			36	72	nC
Reverse Recovery Fall Time	$t_a$			21		ns
Reverse Recovery Rise Time	$t_b$			17		

Notes:

a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2 \%$ .

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

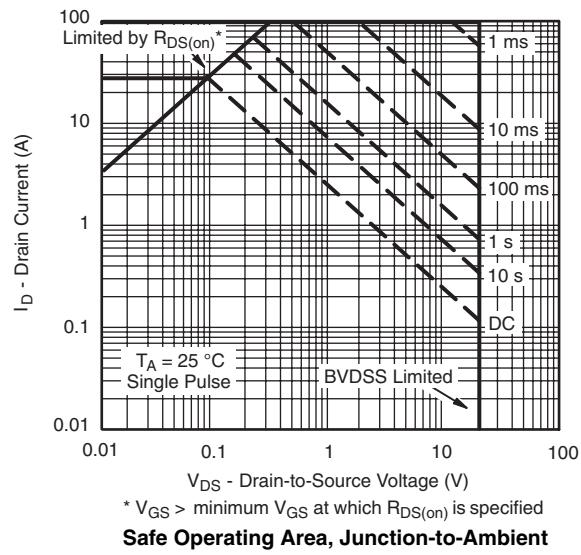
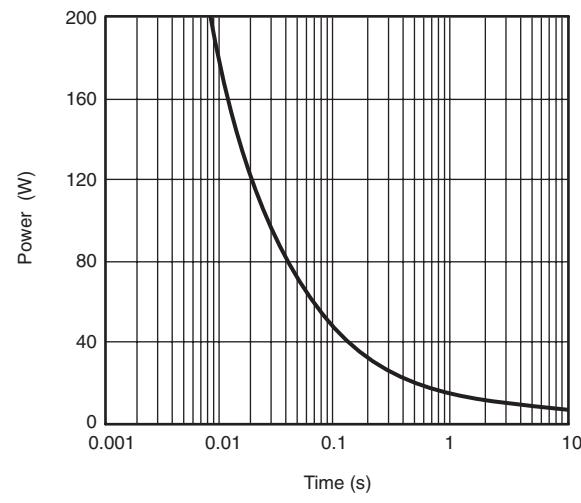
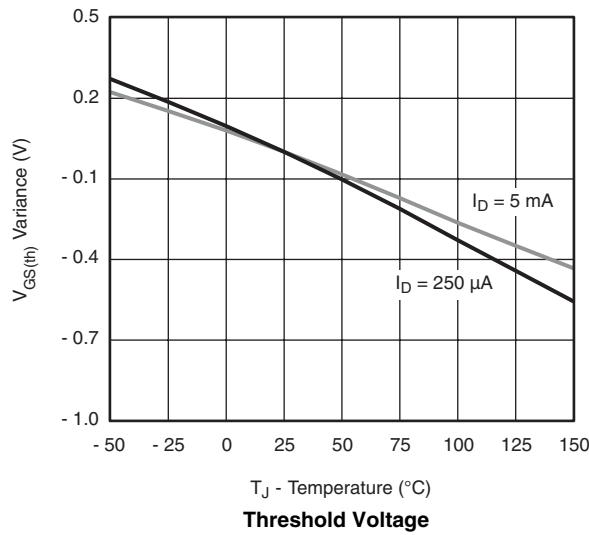
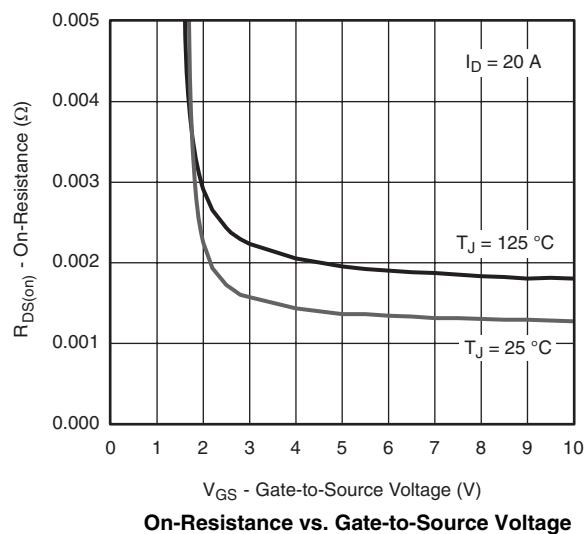
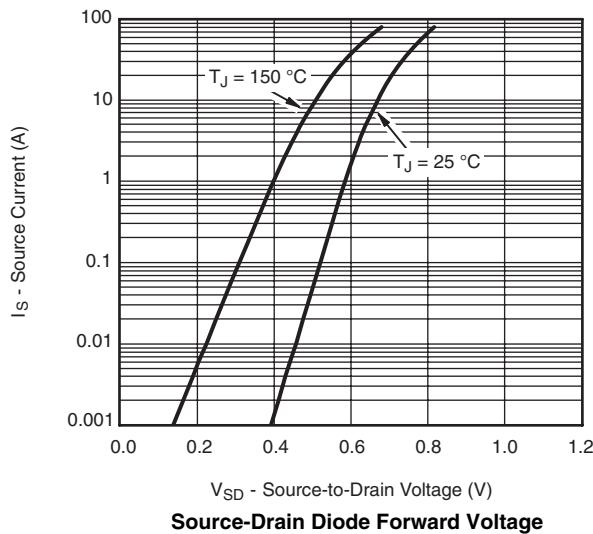
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted


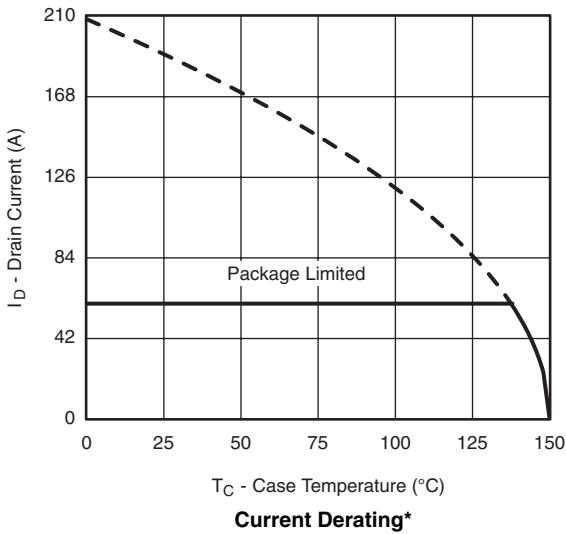
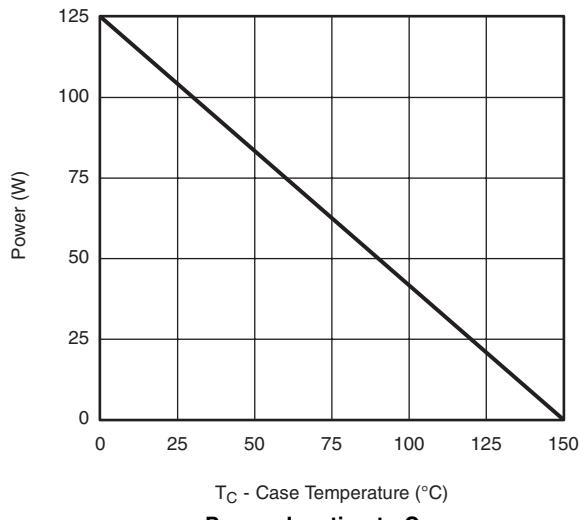
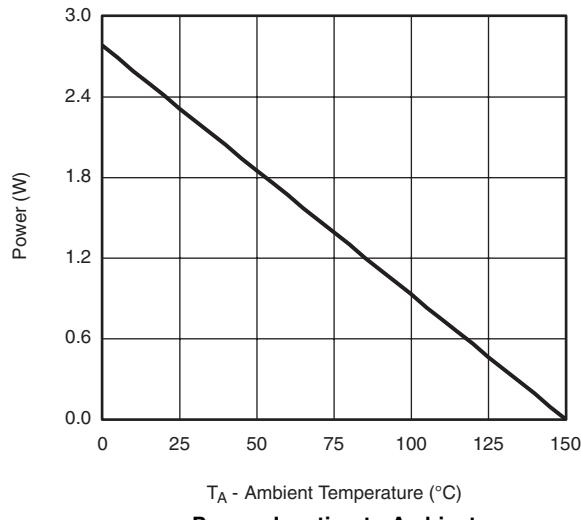
## SiR404DP

Vishay Siliconix



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted
**Current Derating\*****Power, Junction-to-Case****Power, Junction-to-Ambient**

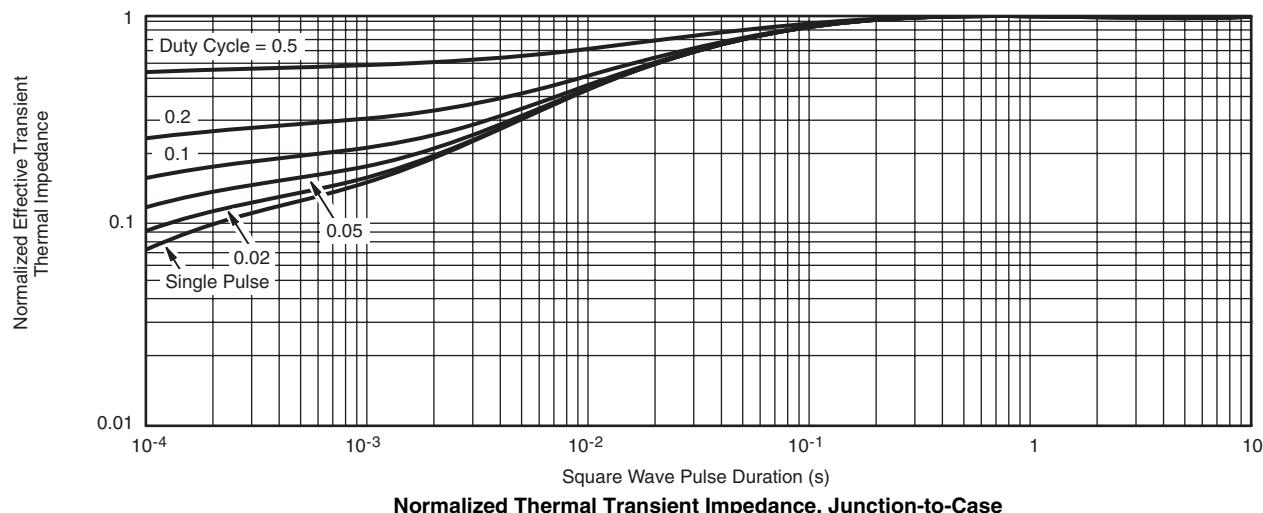
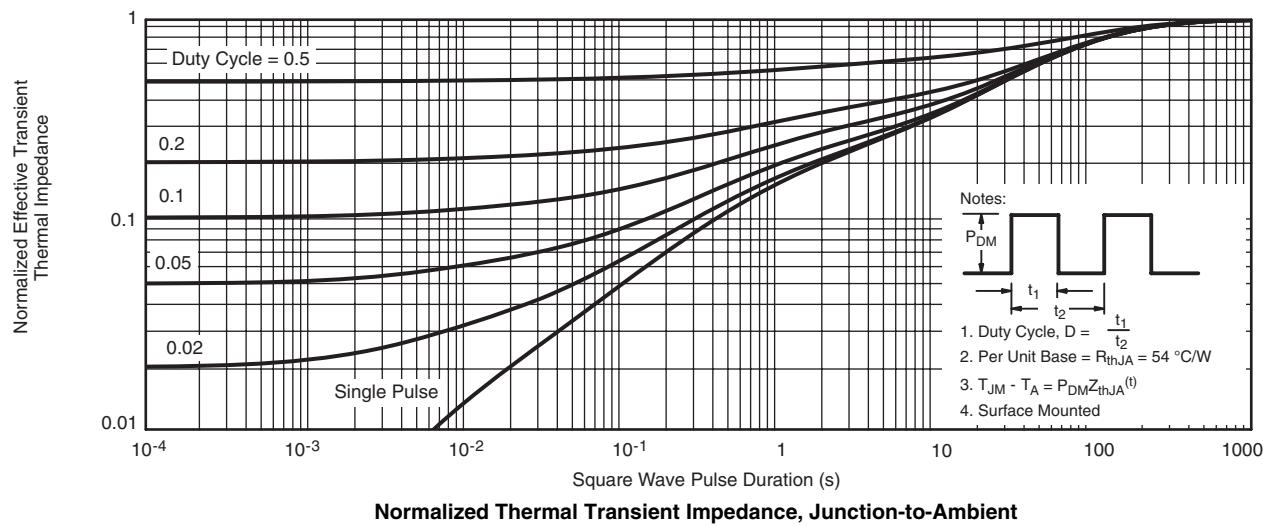
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## SiR404DP

Vishay Siliconix

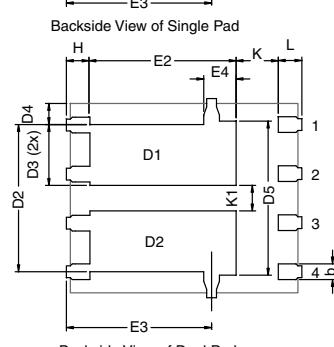
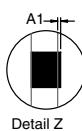
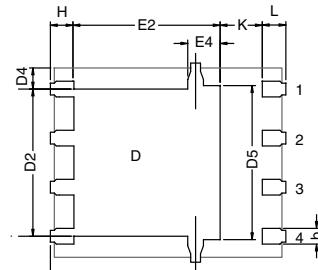
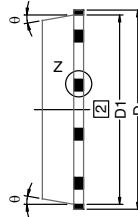
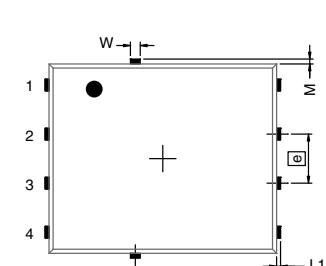


## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?64815](http://www.vishay.com/ppg?64815).

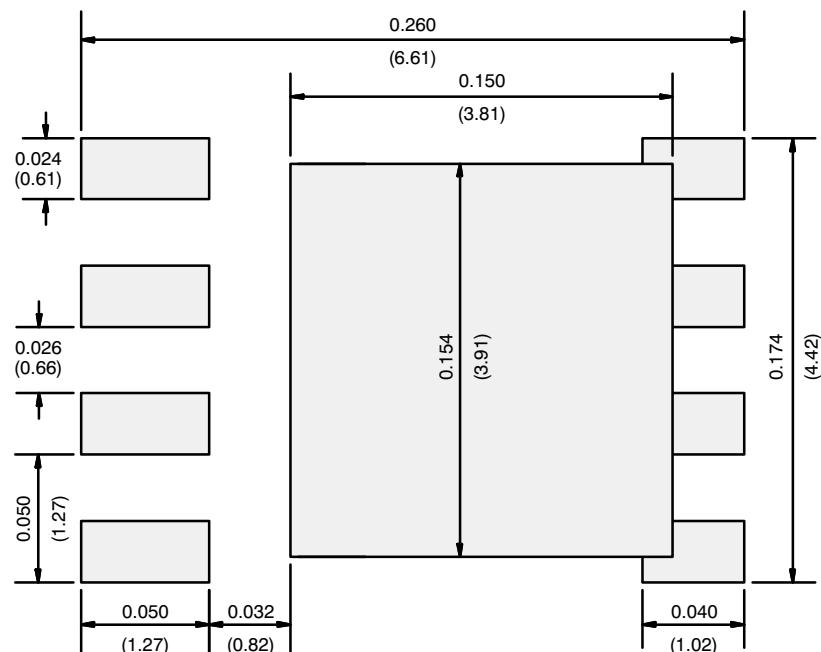
## PowerPAK® SO-8, (Single/Dual)


**Notes**

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
c	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.154	
D3	1.32	1.50	1.68	0.052	0.059	0.066	
D4	0.57 typ.			0.0225 typ.			
D5	3.98 typ.			0.157 typ.			
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	5.79	5.89	5.99	0.228	0.232	0.236	
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144	
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151	
E3	3.68	3.78	3.91	0.145	0.149	0.154	
E4 (for AL product)	0.58 typ.			0.023 typ.			
E4 (for other product)	0.75 typ.			0.030 typ.			
e	1.27 BSC			0.050 BSC			
K (for AL product)	1.45 typ.			0.057 typ.			
K (for other product)	1.27 typ.			0.050 typ.			
K1	0.56	-	-	0.022	-	-	
H	0.51	0.61	0.71	0.020	0.024	0.028	
L	0.51	0.61	0.71	0.020	0.024	0.028	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
$\theta$	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
M	0.125 typ.			0.005 typ.			

ECN: C13-0702-Rev. K, 20-May-13  
DWG: 5881

**RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single**

Recommended Minimum Pads  
Dimensions in Inches/(mm)

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**