STV9432TAP

100MHz OSD FOR MONITOR INCLUDING BEAM CURRENTS, VIDEO TIMING ANALYZER AND PWMs

- MULTIFUNCTION OSD FOR MONITOR
- INCLUDES FACILITIES FOR CUT-OFF VOLTAGE MONITORING:
  - THREE 8 BITS ADC INPUTS
  - ADC TRIGGER DURING RETRACE TIME OF A PROGRAMMED LINE
- INCLUDES FACILITIES FOR SCREEN SIZE & CENTERING AUTO SETUP
  - HS, VS, VIDEO TIMING MEASUREMENTS
- 100MHz MAX. PIXEL CLOCK, AVAILABLE FOR ANY LINE FREQUENCY BETWEEN 15 AND 140 kHz
- 12 x 18 CHARACTER ROM FONT INCLUDES:
  - 240 MONOCOLOR CHARACTERS
  - 16 MULTICOLOR CHARACTERS
- CHARACTER FLASHING
- UP TO 1K CHARACTERS TEXT DISPLAY
- ULTRA HIGH FREQUENCY PLL FOR
- JITTER-FREE DISPLAY
- FLEXIBLE DISPLAY:
  - ANY CHARACTER WIDTH AND HEIGHT
  - ANYWHERE IN THE SCREEN
- SINGLE BYTE CHARACTER CODES AND COLOR LOOK-UP TABLE FOR EASY PROGRAMMING AND FAST ACCESS
- CHARACTER FLIP OPERATIONS
- WIDE DISPLAY WINDOW ALLOWS PATTERN GENERATION FOR FACTORY ADJUSTMENTS
- I^2C BUS MCU INTERFACE
- FIVE 8 BITS PWM DAC OUTPUTS

DESCRIPTION

Connected to a host MCU via its serial I^2C Bus, the STV9432TAP is a multifunction slave peripheral device integrating the following blocks:

- On-screen Display. It includes a MASK PROGRAMMABLE ROM that holds the CUSTOM CHARACTER FONT, a 1Kbytes RAM that stores the code strings of the different lines of text to be displayed, and a set of registers to program character sizes and colors. A built-in digital PLL, operating at very high frequency, gives an accurrate display without visible jitter for a wide line frequency range from 15 to 140 kHz.
- Cut-off Monitoring Circuitry includes: 5 x 8 bits PWM DACs, 3 x 8 bits ADCs and a programmable ADC sampling trigger. It gives the possibility to measure the three beam currents, during the horizontal flyback, at a given line in the frame, provided that the three ADC inputs are connected to a beam current sensing circuitry. The values are stored in three BEAM CURRENT REGISTERS, and available for MCU read.
- Video Timing Analyzer. Using the Horizontal Sync, Vertical Sync, Horizontal Flyback, and "Video Active" inputs, a set of counters give the different timing measurements necessary to analyze the current Video timing characteristics in order to make the automatic set-up of screen size and centering. The measurements are initialized on the same programmable trigger line than in the above cut-off monitoring circuitry.

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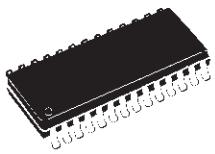
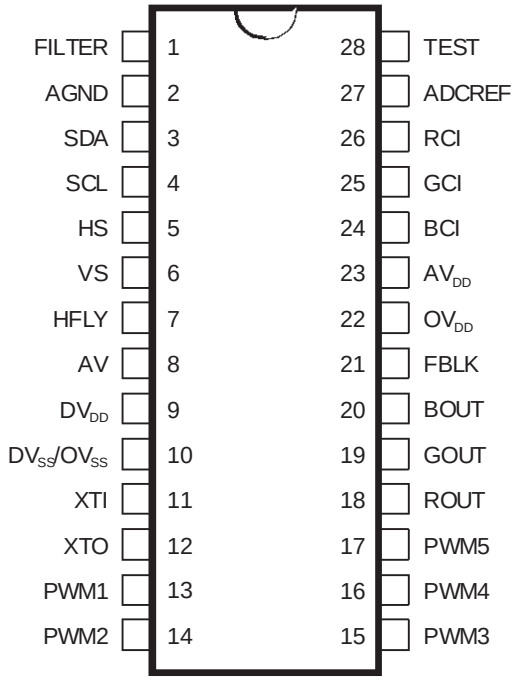


SO28

(Plastic Micropackage)
ORDER CODE: STV9432TAP

Version 4.0

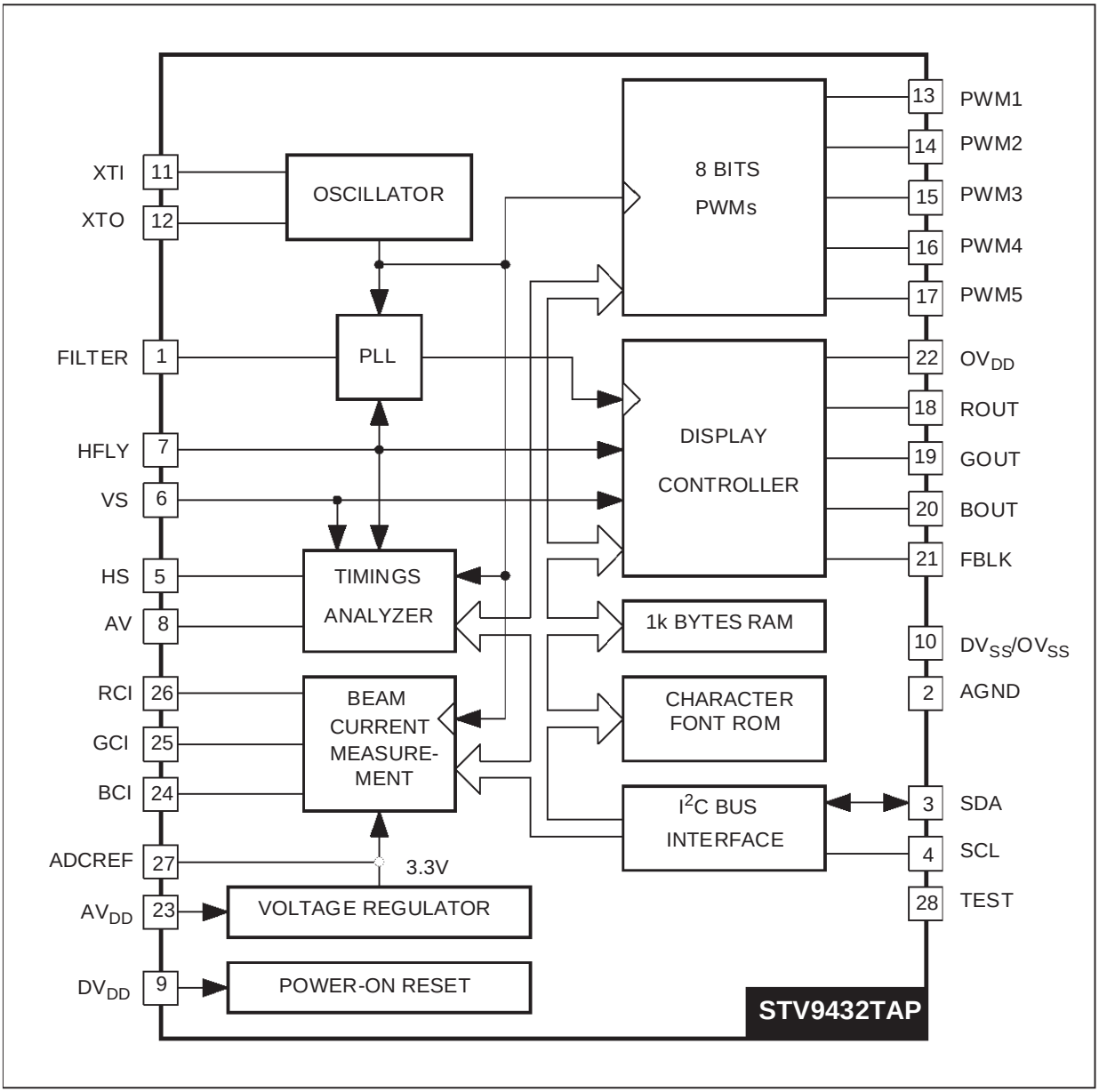
1 - PIN CONNECTIONS



2 - PIN DESCRIPTION

Pin Number	Symbol	Type	Description
1	FILTER	I/O	PLL Filter
2	AGND	Power	Analog Ground
3	SDA	I/O	I^2C Bus Serial Data
4	SCL	I	I^2C Bus Serial Clock
5	HS	I	Horizontal Sync Input
6	VS	I	Vertical Sync Input
7	HFLY	I	Horizontal Flyback Input
8	AV	I	Active Video Input
9	DV_{DD}	Power	Digital +5V Power Supply
10	DV_{SS}/OV_{SS}	Power	Digital and RGB Output Ground
11	XTI	I	Crystal Oscillator Input
12	XTO	O	Crystal Oscillator Output
13	PWM1	O	PWM DAC Output 1
14	PWM2	O	PWM DAC Output 2
15	PWM3	O	PWM DAC Output 3
16	PWM4	O	PWM DAC Output 4
17	PWM5	O	PWM DAC Output 5
18	ROUT	O	Red Output
19	GOUT	O	Green Output
20	BOUT	O	Blue Output
21	FBLK	O	Fast Blanking Output
22	OV_{DD}	Power	+5V Supply for the RGB Outputs
23	AV_{DD}	Power	Analog +5V Power Supply
24	BCI	I	Blue Beam Current Input
25	GCI	I	Green Beam Current Input
26	RCI	I	Red Beam Current Input
27	ADCREF	I/O	ADC Reference Voltage Pin
28	TEST	I/O	Pin to be connected to ground

3 - BLOCK DIAGRAM



4 - ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
AV_{DD}, DV_{DD}, OV_{DD}	Supply Voltage	-0.3, +6.0	V
V_{IN}	Input Voltage	V_{SS}-0.3, V_{DD}+0.3	V
T_{oper}	Operating Temperature	0, +70	^{o}C
T_{stg}	Storage Temperature	-40, +125	^{o}C

5 - ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = 0V, GND = 0V, T_A = 0 to 70°, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY					
AV_{DD}, DV_{DD}, OV_{DD}	Supply Voltage	4.75	5	5.25	V
AI_{DD}+ DI_{DD} + OI_{DD}	Analog and Digital Supply Current	-	-	150	mA
INPUTS (SCL, SDA)					
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.4			V
I_{IL}	Input Leakage Current	-1		+1	µA
INPUTS (HS, VS, AV, HFLY)					
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage HS, VS, AV HFLY	2.4 3.6			V
V_{HYST}	Schmidt Trigger Hysteresis		0.4		V
I_{PU}	Pull-up Source Current (V_{IN} = 0V)		100		µA
H_{SIN}	Horinzontal Synchro Input Range	15	-	140	kHz
OUTPUTS (SDA open drain)					
V_{OL}	Output Low Voltage (I_{OL} = 3mA)	0		0.4	V
OUTPUTS (R, G, B, FBLK)					
V_{OL}	Output Low Voltage (I_{OL} = 3mA)	0		0.4	V
V_{OH}	Output High Voltage (I_{OH} = 3mA)	$0.8V_{DD}$		V_{DD}	V
OSCILLATOR (XTI, XTO)					
I_{IL}	XTI Input Source Current (V_{IN} = 0V)	3		15	µA
I_{IH}	XTI Input Sink Current (V_{IN} = V_{DD})	3		15	µA
V_{IL}	XTI Input Low Voltage			1.4	V
V_{IH}	XTI Input High Voltage	$0.7V_{DD}$			V
V_{OL}	XTI Output Low Voltage (I_{OL} = 3mA)	0		0.4	V
V_{OH}	XTI Output High Voltage (I_{OH} = 3mA)	$0.8V_{DD}$		V_{DD}	V
ADCREF					
V_{REF}	Output Voltage Reference		3.3		V
8 BITS PWM DACs 1,2,3,4,5					
V_{OL}	Output Low Voltage (I_{OL} = 1.6mA)	0		0.4	V
V_{OH}	Output High Voltage (I_{OH} = -0.8mA)	V_{CC} - 0.5			V
t_{PWM}	PWM Period		256		t_{OSC}
POWER-ON RESET					
DV_{DDTH}	Supply Threshold Level		3.6		V
8 BITS ADC INPUTS (RCI, GCI, BCI)					
V_{IN}	Input Voltage	0		V_{ADCREF}	V
Z_{IN}	Input Impedance		100		k Ω
V_{OFF}	Input Offset Voltage			3	LSB
I_{LEAK}	Input Leakage Current		0	50	µA
ILE	Integral Linearity Error (Note 2)	-2		+2	LSB
DLE	Differential Linearity Error (Note 2)	-0.5		+0.5	LSB

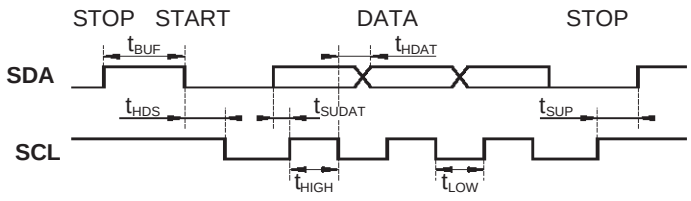
6 - TIMINGS

Symbol	Parameter	Min.	Typ.	Max.	Unit
OSCILLATOR					
f_{OSC}	Clock Frequency		8		MHz
f_{PXL}	Maximum Pixel Frequency			100	MHz
R, G, B, FBLK (C_{LOAD} = 30pF)					
t_R	Rise Time (see Note 1)		5		ns
t_F	Fall Time (see Note 1)		5		ns
t_{SKEW}	Skew between R, G, B, FBLK		5		ns
I^2C INTERFACE: SDA AND SCL (see Figure 1)					
f_{SCL}	SCL Clock Frequency	0		400	kHz
t_{BUF}	Time the bus must be free between 2 access	500			ns
t_{HDS}	Hold Time for Start Condition	500			ns
t_{SUP}	Set up Time for Stop Condition	500			ns
t_{LOW}	The Low Period of Clock	400			ns
t_{HIGH}	The High Period of Clock	400			ns
t_{HDAT}	Hold Time Data	0			ns
t_{SUDAT}	Set up Time Data	500			ns
t_F	Fall Time of SDA			20	ns
t_R	Rise Time of both SCL and SDA	Depend on the pull-up resistor and the load capacitance			
ANALYZER (HS, HFLY, AV)					
t_{HLOW}	Low Pulse Width (see Note 3)	2		4091	t_{HTIM}
t_{HHIGH}	High Pulse Width	2		4091	t_{HTIM}
Hs	Hs Frequency			Hfly	
ANALYZER (VS)					
t_{VLOW}	Low Pulse Width	2		4091	Lines
t_{VHIGH}	High Pulse Width	2		4091	Lines

Notes:

- These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches coming from corners of our processes and also temperature characterization.
- The ADC measurements are dependant on the noise. The test is done by correlation in order to screen out marginal devices.
- $t_{HTIM} = 3t_{OSC} : 40$.

Figure 1.



7 - SERIAL INTERFACE

The 2-wires serial interface is an I^2C interface. To be connected to the I^2C bus, a device must own its slave address; the slave address of the STV9432TAP is BA (in hexadecimal).

A6	A5	A4	A3	A2	A1	A0	RW
1	0	1	1	1	0	1	

7.1 - Data Transfer in Write Mode

The host MCU can write data into the STV9432TAP registers or RAM.

To write data into the STV9432TAP, after a start, the MCU must send (Figure 2):

- First, the I^2C address slave byte with a low level for the R/W bit,
- The two bytes of the internal address where the MCU wants to write data,
- The successive bytes of data.

All bytes are sent MSB bit first and the write data transfer is closed by a stop.

7.2 - Data Transfer in Read Mode

The host MCU can read data from the STV9432TAP register, RAM or ROM.

To read data from the STV9432TAP (Figure 3), the MCU must send 2 different I^2C sequences. The first one is made of I^2C slave address byte with R/W bit at low level and the 2 internal address bytes.

The second one is made of I^2C slave address byte with R/W bit at high level and all the successive data bytes read at successive addresses starting from the initial address given by the first sequence.

Figure 2. I^2C Write Operation

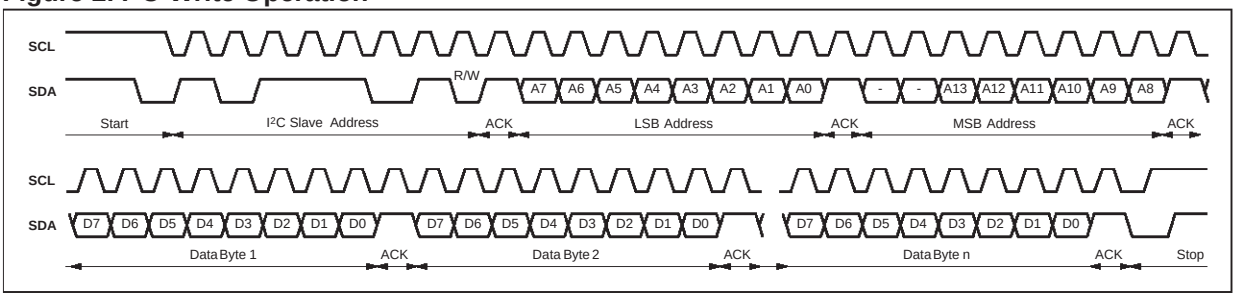
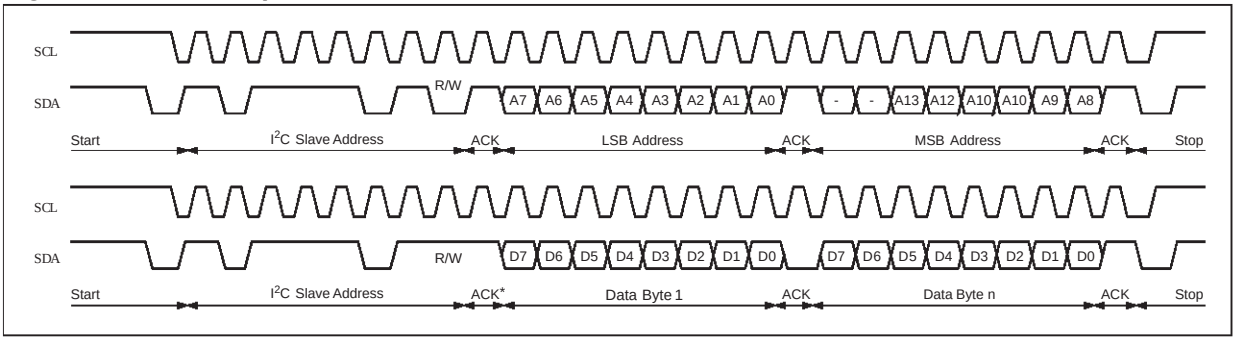


Figure 3. I^2C Read Operation



7.3 - ADDRESSING SPACE

7.3.1 - General Mapping

STV9432TAP registers, RAM and ROM are mapped in a 32Kbytes addressing space.
The mapping is the following:

0000 03FF	1024 bytes RAM	Descriptors and character codes
0400 07FF	Empty Space	
0800 3FFF	Character Generator ROM	
4000 403F	Internal Registers	
4040 7FFF	Empty Space	

Important Notice: All 16 bits datas are mapped LSB byte at lower address and MSB byte at higher address.

- Example: H1 12 bits register: @4000: 8 LSB bits - @4001: 4 MSB bits.
- Descriptors must also be written to RAM LSB byte first.

7.3.2 - I^2C Registers Mapping

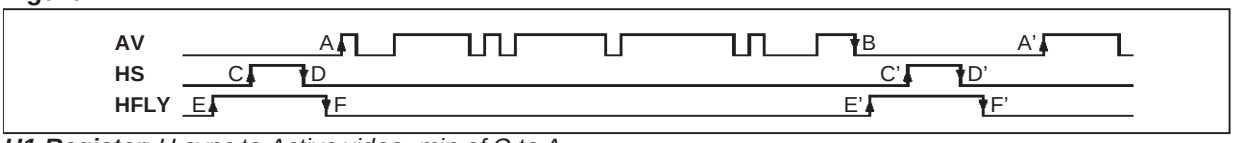
4000	H1 LSB	4024	Color 4
4001	H1 MSB	4025	Color 5
4002	H2 LSB	4026	Color 6
4003	H2 MSB	4027	Color 7
4004	H3 LSB	4028	Color 8
4005	H3 MSB	4029	Color 9
4006	H4 LSB	402A	Color 10
4007	H4 MSB	402B	Color 11
4008	H5 LSB	402C	Color 12
4009	H5 MSB	402D	Color 13
400A	H6 LSB	402E	Color 14
400B	H6 MSB	402F	Color 15
400C	V1 LSB	4030	Line Duration
400D	V1 MSB	4031	Top Margin
400E	V2 LSB	4032	Horizontal Delay
400F	V2 MSB	4033	Character Height
4010	V3 LSB	4034	Display Control
4011	V3 MSB	4035	Locking Time Constant
4012	RCI	4036	Capture Time Constant
4013	GCI	4037	Initial Pixel Period
4014	BCI	4038	PWM1
4015	SBN	4039	PWM2
4016	TIMG	403A	PWM3
4017-401F	Reserved	403B	PWM4
4020	Color 0	403C	PWM5
4021	Color 1	403D-403E	Reserved
4022	Color 2	403F	RST
4023	Color 3	4040-7FFF	Reserved

8 - TIMING ANALYZER

8.1 - VIDEO HORIZONTAL TIMINGS

All horizontal timing measurements use a 106.7MHz clock. This clock is made from the internal oscillator: $f_{HTIM} = 40f_{OSC} : 3$. These twelve bits read-only registers read time measurements, given in t_{HTIM} units. They hold the value of the last measurement that was initiated by I^2C command (see TIMG Register).

Figure 4.



***H1 Register**: H sync to Active video, min of C to A*

4000	H1.7	H1.6	H1.5	H1.4	H1.3	H1.2	H1.1	H1.0
4001	-	-	-	-	H1.11	H1.10	H1.9	H1.8

***H2 Register**: Active video to H sync, min of B to C'*

4002	H2.7	H2.6	H2.5	H2.4	H2.3	H2.2	H2.1	H2.0
4003	-	-	-	-	H2.11	H2.10	H2.9	H2.8

***H3 Register**: Line period, C to C'*

4004	H3.7	H3.6	H3.5	H3.4	H3.3	H3.2	H3.1	H3.0
4005	-	-	-	-	H3.11	H3.10	H3.9	H3.8

***H4 Register**: H Fly to H sync, E to C*

4006	H4.7	H4.6	H4.5	H4.4	H4.3	H4.2	H4.1	H4.0
4007	-	-	-	-	H4.11	H4.10	H4.9	H4.8

***H5 Register**: H sync to H Fly, C to E'*

4008	H5.7	H5.6	H5.5	H5.4	H5.3	H5.2	H5.1	H5.0
4009	-	-	-	-	H5.11	H5.10	H5.9	H5.8

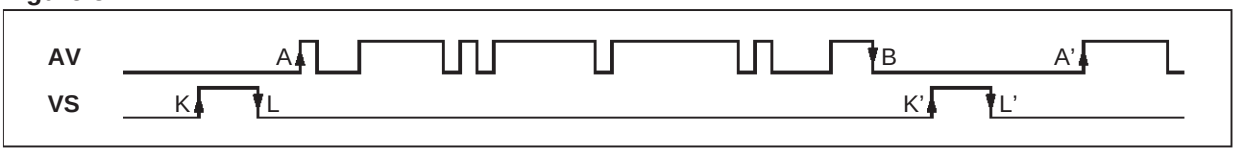
***H6 Register**: H fly pulse, E to F*

400A	H6.7	H6.6	H6.5	H6.4	H6.3	H6.2	H6.1	H6.0
400B	-	-	-	-	H6.11	H6.10	H6.9	H6.8

8.2 - VIDEO VERTICAL TIMINGS

These twelve bits read-only registers read time measurements, given in number of scan lines. They hold the value of the last measurement that was initiated by I^2C command (see TIMG Register).

Figure 5.



V1 Register: *V sync to Active video, min. of K to A*

400C	V1.7	V1.6	V1.5	V1.4	V1.3	V1.2	V1.1	V1.0
400D	-	-	-	-	V1.11	V1.10	V1.9	V1.8

V2 Register*: Active video to V sync, min. of B to K'*

400E	V2.7	V2.6	V2.5	V2.4	V2.3	V2.2	V2.1	V2.0
400F	-	-	-	-	V2.11	V2.10	V2.9	V2.8

V3 Register*: Number of lines per frame, K to K'* *'*

4010	V3.7	V3.6	V3.5	V3.4	V3.3	V3.2	V3.1	V3.0
4011	-	-	-	-	V3.11	V3.10	V3.9	V3.8

8.3 - TIMING ANALYSIS TRIGGER

The Timing Analysis is performed according to the setting of SBN and TIMG registers:

8.3.1 - SBN Register

This 8 bits register holds the "sampling bloc" number.

The sampling bloc is a set of 4 consecutive scan lines, the first of which is used for sampling the video timings or Beam currents.

The reset value of this register is 0.

4015	SBN7	SBN6	SBN5	SBN4	SBN3	SBN2	SBN1	SBN0

8.3.2 - TIMG Register

4016	STM	NFR1	NFR0	ADCDLY3	ADCDLY2	ADCDLY1	ADCDLY0	SELECT

This 8 bits register holds the following parameters:

STM	:	Start Measurement Bit. This bit has to be forced to 1 by I^2C to start the measurement sequence, depending on the measurement selection bit. When measurement is completed the IC will reset this bit to 0.
NFR [1:0]	:	NFR number of measurement frames, 1 to 4 frames
ADCDLY[3:0]	:	Cut-off Beam current ADC sampling delay time: 0 to 15 x t_{OSC}, by t_{OSC} steps
SELECT	:	Selection of Beam current measurement (0) or Timing measurement (1)

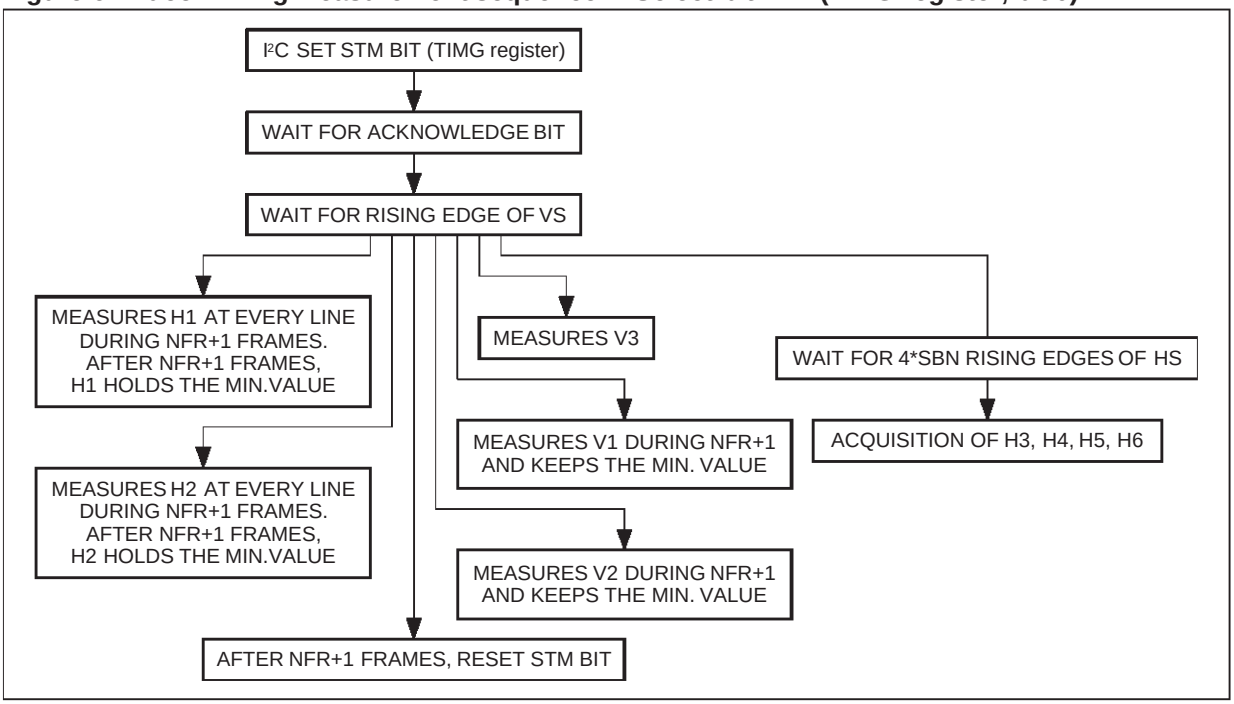
To initiate a Timing Analysis cycle:

- program the Sampling Bloc Number in the SBN Register,
- program the TIMG Register, with: "SELECT" bit =1, "NFR" bits specify the number of measurement frames (H1, H2, V1, V2), "STM" bit = 1 (Start Measurement).

As soon as the measurement cycle is finished, the "STM" bit is automatically reset by the device.

After a Timing Analysis cycle, reading a zero in STM bit of TIMG register means that the measurement is completed and the mcu may read the results in Hi and Vi registers.

Figure 6. Video Timing Measurement sequence - “Select bit = 1” (TIMG register, bit 0)



9 - BEAM CURRENTS MEASUREMENT

9.1 - BEAM CURRENT MEASUREMENT REGISTERS

The Beam Current Measurement circuitry uses three A to D converters, sampled at f_{OSC} frequency.

These three 8 bits registers read the values of the last Beam currents measurement, initiated by I^2C command (see TIMG register).

***RCI Register**: Red Beam Current Input*

4012	RCI7	RCI6	RCI5	RCII4	RCI3	RCI2	RCI1	RCI0

***GCI Register**: Green Beam Current Input*

4013	GCI7	GCI6	GCI5	GCI4	GCI3	GCI2	GCI1	GCI0

BCI Register: Blue Beam Current Input

4014	BCI7	BCI6	BCI5	BCI4	BCI3	BCI2	BCI1	BCI0

9.2 - BEAM CURRENT MEASUREMENT TRIGGER

The Beam Currents Measurement is performed according to the setting of SBN and TIMG registers :

9.2.1 - SBN Register

This 8 bits register holds the ”sampling bloc” number. The sampling bloc is a set of 4 consecutive scan lines, the first of which is used for sampling the video timings or Beam currents. The reset value of this register is 0.

4015	SBN7	SBN6	SBN5	SBN4	SBN3	SBN2	SBN1	SBN0

9.2.2 - TIMG Register

4016	STM	NFR1	NFR0	ADCDLY3	ADCDLY2	ADCDLY1	0	SELECT

This 8 bits register holds the following parameters:

STM : Start Measurement Bit. This bit has to be forced to 1 by I^2C to start the measurement sequence, depending on the measurement selection bit. When measurement is completed the IC will reset this bit to 0.

NFR [1:0] : NFR number of measurement frames, 1 to 4 frames

ADCDLY [3:0] : Cut-off Beam current ADC sampling delay time: 0 to 15 x t_{OSC}, by t_{OSC} steps

SELECT : Selection of Beam current measurement (0) or Timing measurement (1)

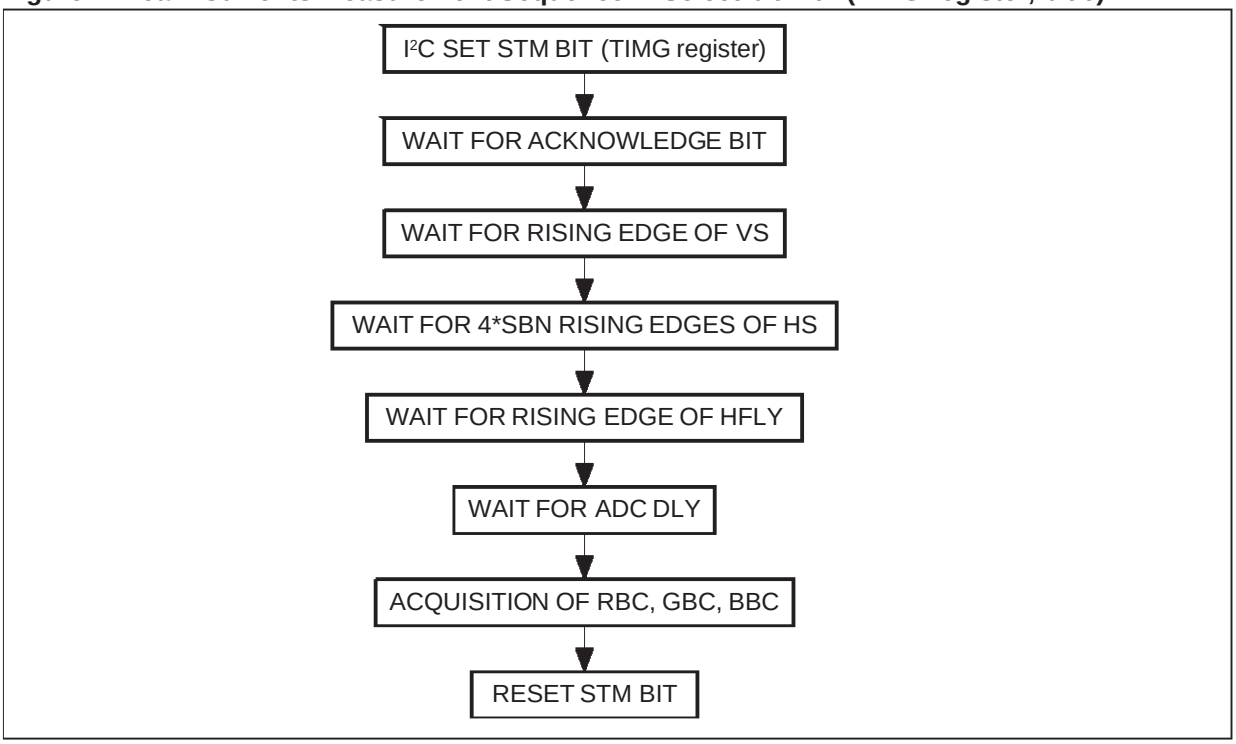
When measurement is completed the IC will reset this bit to 0. The reset value of this register is 0.

To initiate a Beam Currents Measurement cycle:

- program the Sampling Bloc Number in the SBN Register,
- program the TIMG Register, with: ”SELECT” bit = 0, ”ADCDLY” bits specify the sampling time during HFly, ”STM” bit = 1 (Start Measurement).

As soon as the measurement cycle is finished, the ”STM” bit is automatically reset by the device. After a Beam Currents Measurement cycle, reading a zero in STM bit of TIMG register means that the measurement is completed and the MCU may read the results in RCI, GCI, and BCI registers.

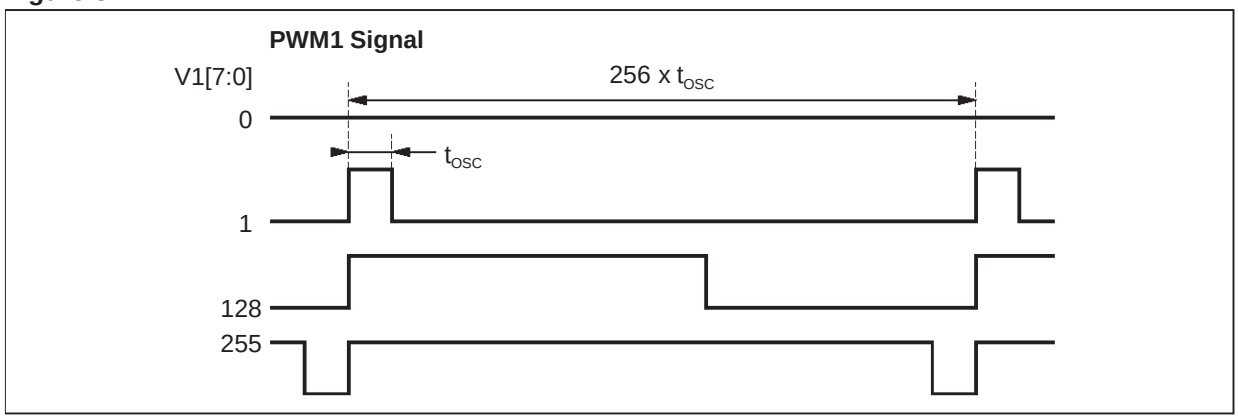
Figure 7. Beam Currents Measurement Sequence - “Select bit = 0” (TIMG register, bit 0)



10 - DIGITAL TO ANALOG PWM OUTPUTS

The five to A outputs PWM1 toc5 of the STV9432TAP are pulse width modulator type converter outputs. The frequency of the output signal is f_{OSC}: 256 and the duty cycle is: Value [7:0]: 256. After an external low pass filter, the voltage value of the output is: Value [7:0] x V_{DD} : 256.

Figure 8.



10.1 - PWM REGISTERS

Pulse Width Modulator 1

4038	V17	V16	V15	V14	V13	V12	V11	V10

V1[7:0] : Digital value of the 1st PWM D to A converter (Pin 13)

Pulse Width Modulator 2

4039	V27	V26	V25	V24	V23	V22	V21	V20

V2[7:0] : Digital value of the 2nd PWM D to A converter (Pin 14)

Pulse Width Modulator 3

403A	V37	V36	V35	V34	V33	V32	V31	V30

V3[7:0] : Digital value of the 3rd PWM D to A converter (Pin 15)

Pulse Width Modulator 4

403B	V47	V46	V45	V44	V43	V42	V41	V40

V4[7:0] : Digital value of the 4th PWM D to A converter (Pin 16)

Pulse Width Modulator 5

403C	V57	V56	V55	V54	V53	V52	V51	V50

V5[7:0] : Digital value of the 5th PWM D to A converter (Pin 17)

Note: Power-on reset default value of PWM register is OOH.

11 - SOFTWARE RESET REGISTER

403F	-	-	-	-	-	-	-	RST

To perform a software I^2C reset of the device, set the RST bit to ONE.

This bit will be automatically reset by the device.

Software Reset will put all Write registers at their default power-on value, and reset all internal logic blocks except the I^2C bus interface itself. It will not change the RAM contents.

12 - ON-SCREEN DISPLAY

The STV9432TAP on-screen display is able to display any line of characters (character strip) anywhere in the screen.

Character strings are programmed by the MCU in RAM via I^2C bus. Character shapes are coded in the internal ROM font. Character strips may be adjacent or separated by vertical spaces (Spacing strips)

Consequently, one display page is made of a list of Character strips and Spacing strips.

A Top Margin and a Left Margin are programmable in dedicated registers.

12.1 - RAM PROGRAMMING

12.1.1 - Two kinds of Data

Strip Descriptors and Character Codes

An OSD screen is made of a number of Character and Spacing strips.

There are two groups of Data that make one OSD screen:

- a Strip Descriptors list,
- Text strings - one per Character strip.

Each Strip is associated with a 2 bytes Strip Descriptor.

There are two kinds of Strip Descriptors:

- Character Strip Descriptors: they contain the Text string Ram address of the Character Strip,
- Spacing Strip Descriptors: they specify the vertical space height.

In the example shown in Figure 9, the OSD screen, is made of 9 strips.

In RAM, there is:

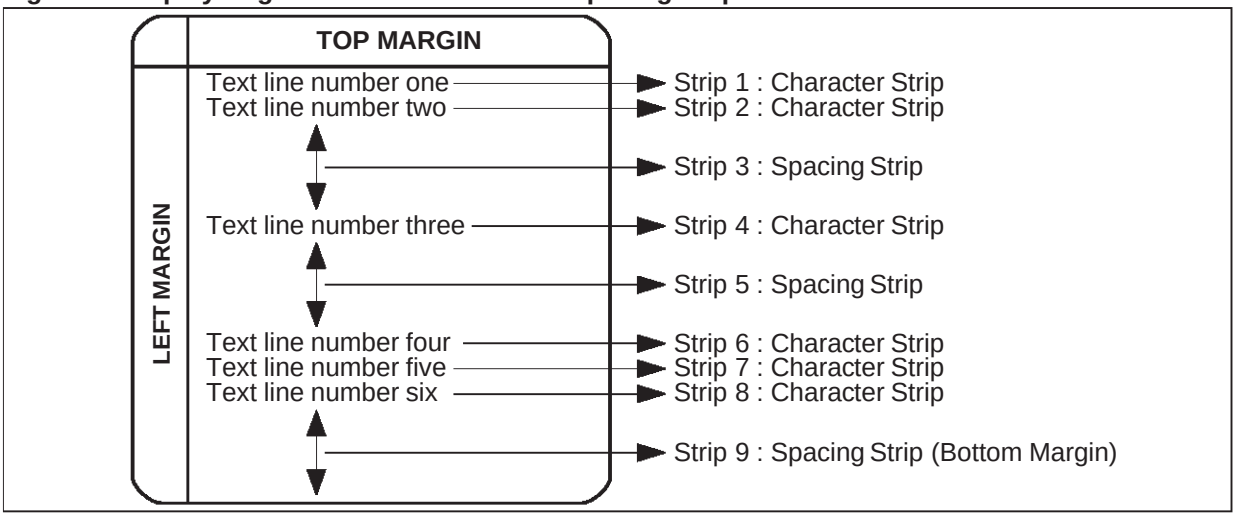
- one list of 9 Strip descriptors (size = 9 x 2 bytes = 18 bytes),
- 6 Text strings, each of them is made of the character codes of the line of text.

Text strings can be programmed anywhere in RAM. The Descriptor list can be located at 16 different addresses in RAM, this address is defined in the Display Control Register.

It is consequently possible to store up to 16 different pages in RAM.

The current Displayed page is specified in the Display Control Register. It refers to a given Page Descriptor list.

Figure 9. Display Page: list of Character and Spacing strips



12.1.2 - Descriptors

Spacing

MSB	0	L/C	-	-	-	-	-	-
LSB	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

L/C : LINE or CHARACTER spacing:
= 0, spacing descriptor defined as character height (SL[7:0] = 1 to 255 character).
= 1, spacing descriptor defined as scan line height (SL[7:0] = 1 to 255 scan lines).

SL[7:0] : Number of selected height (character or scan lines according L/C).

Character

MSB	1	DE	CLU3	CLU2	CLU1	CLU0	C9	C8
LSB	C7	C6	C5	C4	C3	C2	C1	C0

DE : Display enable:
= 0, R = G = B = 0 and FBLK = FBK bit of display control register on the whole strip,
= 1, display of the characters.

CLU[3:0] : Active color selection at the begining of the strip.

C[9:1] : Address of the first character code of the strip.

C0 : Address 0 must be 0.

12.1.3 - Code Format

There are basically 3 kinds of code:

- the control codes from 0 to 15 (00H to 0FH),
- the ROM monochrome character codes from 16 to 255 (10H to FFH),
- the two bytes multicolor character codes from 08F0 to 08FF (Hex).

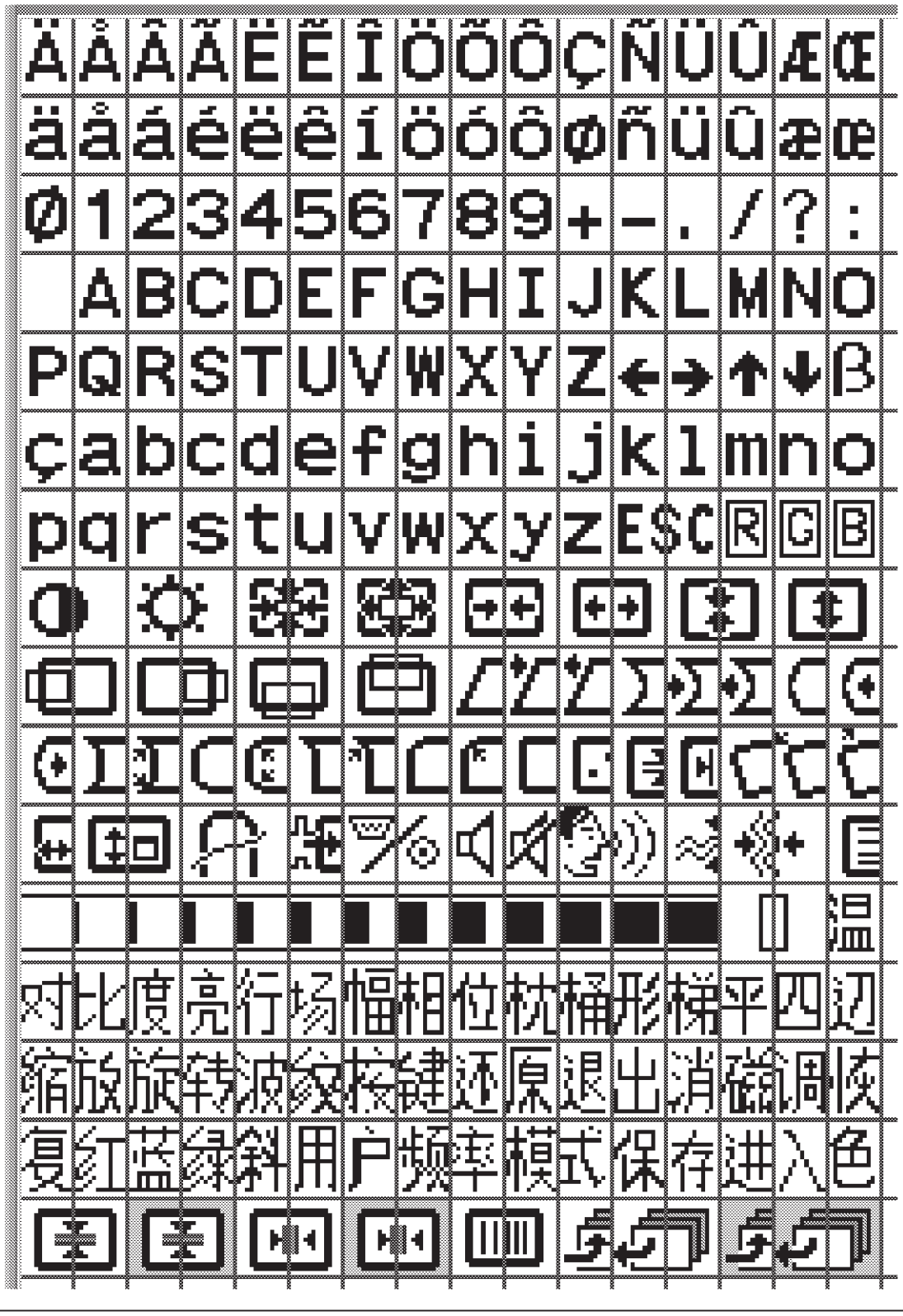
For code definitions see Table 1.

Table 1 Character and Command Codes

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	col 0	**240 Monochrome Characters**														
1	col 1															
2	col 2															
3	col 3															
4	col 4															
5	col 5															
6	col 6															
7	col 7															
8	multicol															
9	nop															
A	vflip															
B	hflip															
C	dflip															
D	call															
E	rtn															
F	eof															

Single byte codes 00 to 0f are command codes. Single byte codes 10 to ff are monochrome character codes. Double byte codes 08F0 to 08FF are multicolor character codes.

Figure 10. Character Font for the STV9432TAP



Control Codes

Control codes must be followed by a displayable code, except for RTN & EOL. They must not be used twice consecutively without a displayable code between them.

The control code CALL is preceded by an address byte. The control codes are not displayed except if mentioned.

Codes 0 to 7 (0h to 7h):

COL0 to COL7 codes select 1 byte among 8 within the CLUT in RAM. The block selection is fixed by CLU3 bit of the active character descriptor (see Table 1 and Table 2).

Code 8 (08h):

Multicolor character precode, must be followed by a multicolor character number from F0h to FFh.

Code 9 (09h):

NOP: no operation is performed, can be used to spare a location in RAM for an active control code.

Codes 10 to 12 (0Ah to 0Ch):

FLIPS:
HFLIP(0Bh) Horizontal Flip code flips horizontaly the following displayable code.

VFLIP(0Ah) Vertical Flip code flips verticaly the following displayable code.

DFLIP(0Ch) Horizontal & Vertical Flip code flips horizontaly and verticaly the following displayable code.

Code 13 (0Dh):

CALL, this control code switch the display of the next character to the code address given by the next byte as following:

CALL CODE (odd @) MSB	0	0	0	0	1	1	0	1
ADDRESS BYTE (even @) LSB	A8	A7	A6	A5	A4	A3	A2	A1

A[9:1] : Address of the next code to be used (A0 = 0 only even addresses), in low half part of RAM.

Notes:
CALL and RTN code must be used simultaneously.
CALL and RTN codes are displayed as a SPACE character.
CALL and RTN codes must be placed at odd addresses. They may be preceed by a NOP in order to place them at the right position.

Code 14 (0Eh):

RTN: return to the CALL + 1 code location (see Note).

Code 15 (0Fh):

EOL, end of line terminates the display of the current row.

ROM Character Codes

Codes 16 to 255 (10h to FFh):

ROM monochrome character codes. The characters shapes are 12x18 pixel matrix described in Figure 11.

Codes 256 to 272 (F0h to FFh):

ROM multicolor character codes. They must be preceded by the multicolor pre-code 08h. The characters shapes are 12x18 pixel matrix described in Figure 11.

12.1.4 - OSD Look-up Table

Color look-up table [CLUT] is read/write RAM table. Mapping address is described above in the section ROM Character Codes.

The CLUT is splitted in 2 blocks of 8 bytes. Each byte contains foreground and background informations as described below:

TRA	BR	BG	BB	FL	FR	FG	FB

TRA : Transparent background
FL : Flashing foreground
BR, BG, BB : Background color
FR, FG, FB : Foreground color

Each block may store a different set of colors. One block of colors may be used for the normal items of the menu while the second block, with brighter colors, may be used for selected items of the menu.

The block selection is done by programming bit CLU3 of CLU[3:0] of the character descriptor (see Table 2). It remains selected all the row long.

Bit CLU2, CLU1 and CLU0 of CLU[3:0] of the character descriptor select the active color at the beginning of the row.

The active color can be changed along the row, using 8 control codes COL0 to COL7.

Each control code (COL0 to COL7) activate a dedicated color byte in the CLUT as described in Table 2.

Table 2 CLUT Block Selection

CLU3	CLU[2:0]	Code Name	Command Code (hex)	Ram @(hex)	Reset Value (hex)
0	0	Col 0	00	@4020	07
	1	Col 1	01	@4021	16
	2	Col 2	02	@4022	25
	3	Col 3	03	@4023	34
	4	Col 4	04	@4024	43
	5	Col 5	05	@4025	52
	6	Col 6	06	@4026	61
	7	Col 7	07	@4027	70
1	0	Col 0	00	@4028	70
	1	Col 1	01	@4029	61
	2	Col 2	02	@402A	52
	3	Col 3	03	@402B	43
	4	Col 4	04	@402C	34
	5	Col 5	05	@402D	25
	6	Col 6	06	@402E	16
	7	Col 7	07	@402F	07

12.2 - OSD CONTROL REGISTERS

Line Duration *(reset value: 20H)*

4030	VSP	HSP	LD6	LD5	LD4	LD3	LD2	LD1

VSP : V-SYNC active edge selection
= 0, falling egde,
= 1, rising edge.

HSP : HFLY active edge selection
= 0, rising egde,
= 1, falling edge.

LD[6:1] : LINE DURATION
LD0 = 0
LD1 = 2 periods of character
One character period is 12 pixels long.

Top Margin *(reset value: 30H)*

4031	M9	M8	M7	M6	M5	M4	M3	M2

M[9:2] : TOP MARGIN height from the VSYNC reference edge.
M0 = 0, M1 = 0
M2 = 4 scan lines

Note: The top margin is displayed before the first strip of descriptor list. It can be black if FBK of DISPLAY CONTROL register is set or transparent if FBK is clear.

Horizontal Delay (reset value: 20H)

4032	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

DD[7:0] : HORIZONTAL DISPLAY DELAY from the HSYNC reference edge to the 1st pixel position of the character strips.
Unit = 6 pixel periods. Minimum value is 08H. First pixel position = [DD[7:0] - 6] x 6 + 54 with DD[7:0] = 0,2,4,6 delay is 54 pixel and with DD[7:0] = 1,3,5 delay is 60 pixel

Character Height (reset value: 24H)

4033	-	-	CH5	CH4	CH3	CH2	CH1	CH0

CH[5:0] : HEIGHT of the character strips in scan lines. For each scan line, the number of the slice which is displayed is given by:

SLICE-NUMBER =

$$\text{round}\left(\frac{\text{SCAN-LINE-NUMBER x 18}}{\text{CH[5:0]}}\right)$$

SCAN-LINE-NUMBER = Number of the current scan line of the strip.

Display Control (reset Value: 00H)

4034	OSD	FBK	FL1	FL0	P9	P8	P7	P6

OSD : ON/OFF (if 0, R, G, B and FBLK outputs are 0).

FBK : Fast blanking control:
= 1, forces FBLK pin at "1" outside and inside the OSD area.
This leads to blank video RGB and to only display OSD RGB.
= 0, FBLK pin is driven according character code for normal display of OSD data.

FL[1:0] : Flashing mode :

- 00: No flashing. The character attribute is ignored,
- 01: Flashing at f_F (50% duty cycle),
- 10: Flashing at 2 f_F
- 11: Flashing at 4 f_F

Note: f_F is 128 time vertical frequency.

P[9:6] : Address of the 1st descriptor of the current displayed pages.
P[13:10] and P[5:0] = 0; up to 16 different pages can be stored in the RAM.

Locking Condition Time Constant *(reset value: 01H)*

4035	FR	AS2	AS1	AS0	LUK	BS2	BS1	BS0

FR : Free Running; if = 1 PLL is disabled and the pixel frequency keeps its last value.

AS[2:0] : Phase constant during locking conditions.

BS[2:0] : Frequency constant during locking conditions.

LUK : Lock unlock status bit
0 = unlocked PLL
1 = Locked PLL

Capture Process Time Constant *(reset value: 24H)*

4036	LEN	AF2	AF1	AF0	-	BF2	BF1	BF0

LEN : Lock enable
0 = R,G,B, FBLK are always enabled,
1 = R,G,B,, FBLK are enabled only when PLL is locked.

AF[2:0] : Phase constant during the capture process.

BF[2:0] : Frequency constant during the capture process.

Initial Pixel Period *(reset value: 06H)*

4037	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0

PP[7:0] : Value to initialize the pixel period of the PLL.

12.3 - OSD TIMINGS

The number of pixel periods is given by the LINE DURATION register and is equal to:

[LD[6:1] x 2 + 1] x 12.

(LD[6:1]: value of the LINE DURATION register).

This value allows to define the horizontal size of the characters.

The horizontal left margin is given by the HORIZONTAL DELAY register and is equal to:

(DD[7:0] -6) x 6 + 54

(DD[7:0]: value of the DISPLAY DELAY register).

This value allows to define the horizontal position of the characters on the screen. Due to internal logic, minimum horizontal delay is fixed at 4.5 characters (54 pixel) when DD is even and lower or equal to 6, and it is fixed at 5 characters (60 pixel) when DD is odd and lower or equal to 7.

12.4 - PLL

The PLL function of the STV9432TAP provides the internal pixel clock locked on the horizontal synchro signal and used by the display processor to generate the R, G, B and fast blanking signals. It is made of 2 PLLs. The first one analog (see Figure 11) provides a high frequency that is 40 times the internal oscillator frequency, or 320MHz. This high frequency clock is used by the Display controller.

The 320MHz frequency is then divided by three. The resulting 106.7MHz clock is used by the Video timings analysis block.

The second PLL, full digital (see Figure 12), provides a pixel frequency locked on the horizontal synchro signal. The ratio between the frequencies of these 2 signals is:

M = 12 x (LD[6:1] x 2 + 1) where LD[6:1] is the value of the LINE DURATION register.

Figure 11. Analog PLL

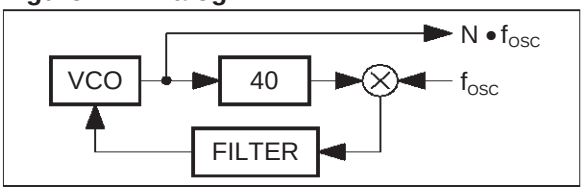
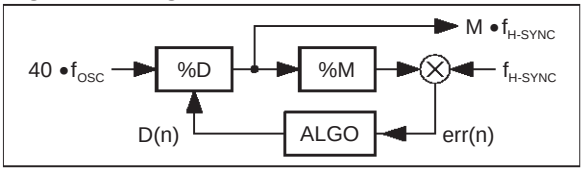


Figure 12. Digital PLL



12.4.1 - Programming of the PLL Registers

Initial Pixel Period (@4037)

This register allows to increase the speed of the convergence of the PLL when the horizontal frequency changes (new graphic standard). The relationship between PP[7:0], LD[6:1], f_{HSYNC} and f_{OSC} is:

$$PP[7:0] = \text{round}\left(\frac{40 \cdot f_{OSC}}{6 \cdot (2 \cdot LD + 1) \cdot f_{HSYNC}}\right)$$

Locking Condition Time Constant (@ 4035)

This register provides the AS[2:0] and BS[2:0] constants used by the algo part of the PLL (see Figure 11). These two constants as well as the phase error err(n) give the new value D(n) of the high frequency signal division. AS[2:0] and BS[2:0] fix the pixel clock frequency. These two constants are used only in locking condition, if the phase error is inferior to a fixed value during at least 4 scan lines. If the phase error becomes greater than this fixed value, the PLL is not in locking condition but in capture process. In this case, the algo part of the PLL used the other constants, AF[2:0] and BF[2:0], given by the next register.

Capture Process Time Constant (@ 4036)

The choice between these two time constants (locking condition or capture process) allows to decrease the capture process time by changing the time response of the PLL.

12.4.2 - How to choose the time constant value

The time response of the PLL is given by its characteristic equation which is:

$(x - 1)^2 + (\alpha + \beta) \cdot (x - 1) + \beta = 0$

Where:

$\alpha = 3 \cdot LD[6:1] \cdot 2^{A-11}$ and $\beta = 3 \cdot LD[6:1] \cdot 2^{B-19}$

(LD[6:1] = value of the LINE DURATION register,

A = value of the 1st time constant, AF or AS and

B = value of the 2^d time constant, BF or BS).

As you can see, the solution depends only on the LINE DURATION and the TIME CONSTANTS given by the I^2C registers.

If $(\alpha + \beta)^2 - 4\beta \geq 0$ and $2\alpha - \beta < 4$, the PLL is stable and its response is like that presented in Figure 14.

If $(\alpha + \beta)^2 - 4\beta \leq 0$, the response of the PLL is like that presented in Figure 15. In this case the PLL is stable if $\tau > 0.7$ damping coefficient). Table 3 gives some good values for A and B constants for different values of the LINE DURATION.

Figure 13. Time Response of the PLL/ Characteristic equation solutions (with real solutions)

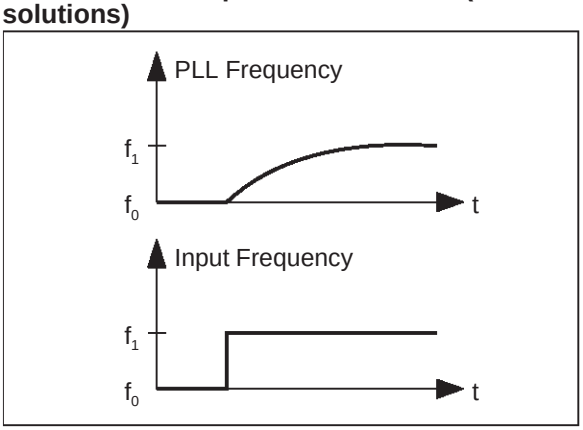


Figure 14. Time Response of the PLL/ Characteristic equation solutions (with complex solutions)

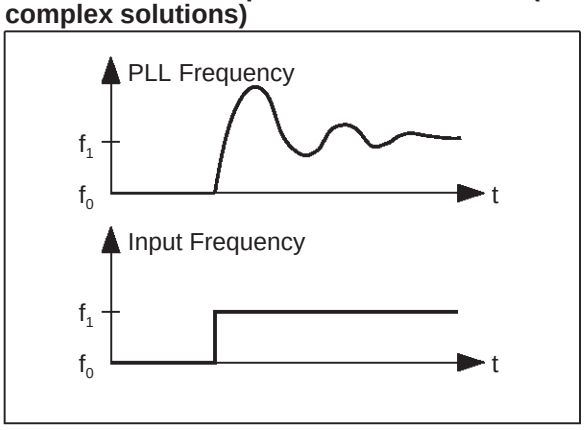


Table 3 Valid Time Constants Examples

B \ A	0	1	2	3	4	5	6
0	YYYY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
1	YYYY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
2	NYYY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
3	NNNY	YYYY	YYYY	YYYN	YNNN	NNNN	NNNN
4	NNNN	NYYY(1)	YYYY	YYYN	YNNN	NNNN	NNNN
5	NNNN	NNNY	YYYY	YYYN	YNNN	NNNN	NNNN
6	NNNN	NNNN	NYYY	YYYN	YNNN	NNNN	NNNN
7	NNNN	NNNN	NNNY	YYYN	YNNN	NNNN	NNNN

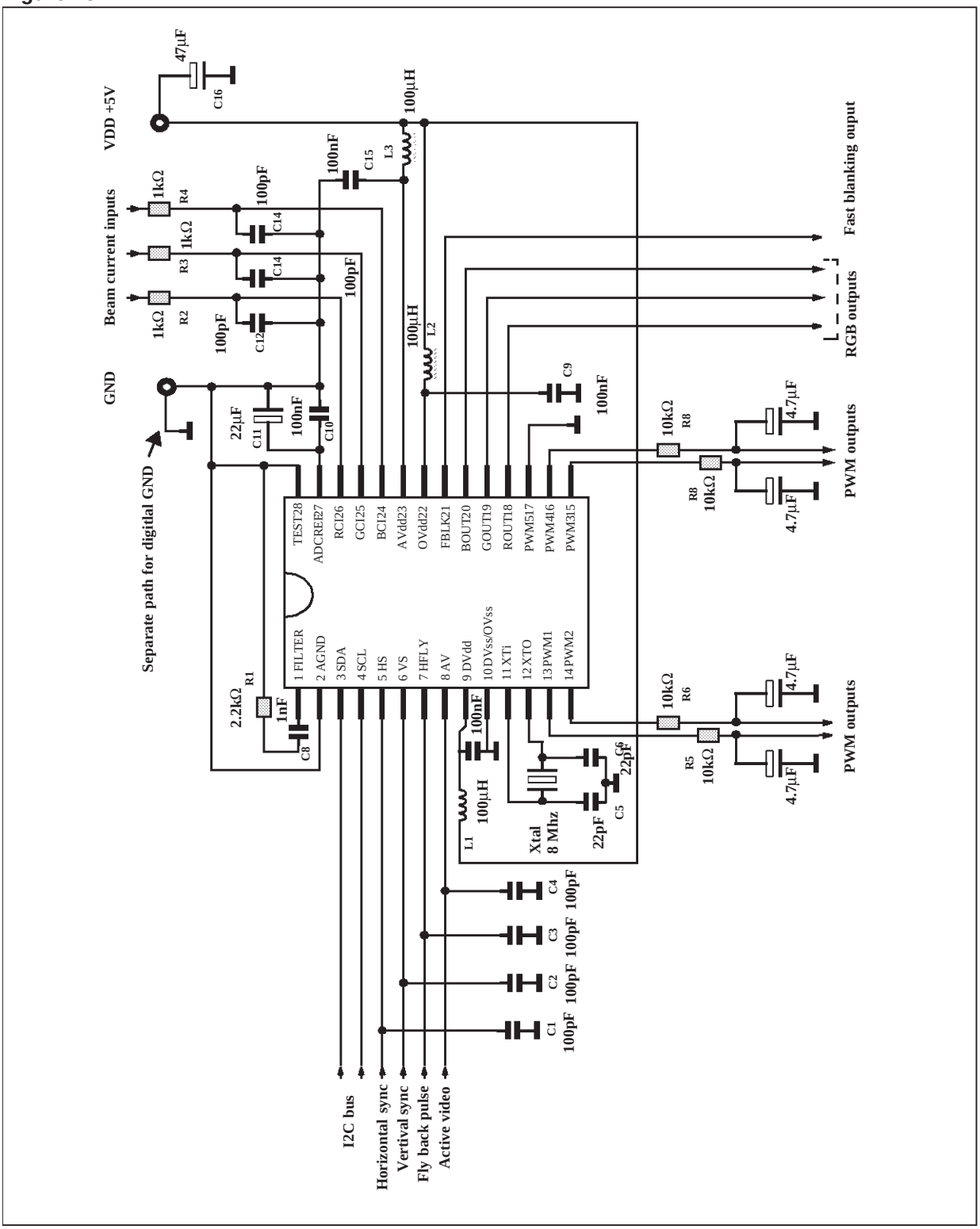
Note : Case of A[2:0] = 1 (001) and B[2:0] = 4 (100):

LD[6:1]	8	16	24	32
Valid Time Constants	N	Y	Y	Y

Table meaning: N = No possible capture - No stability, Y = PLL can lock.

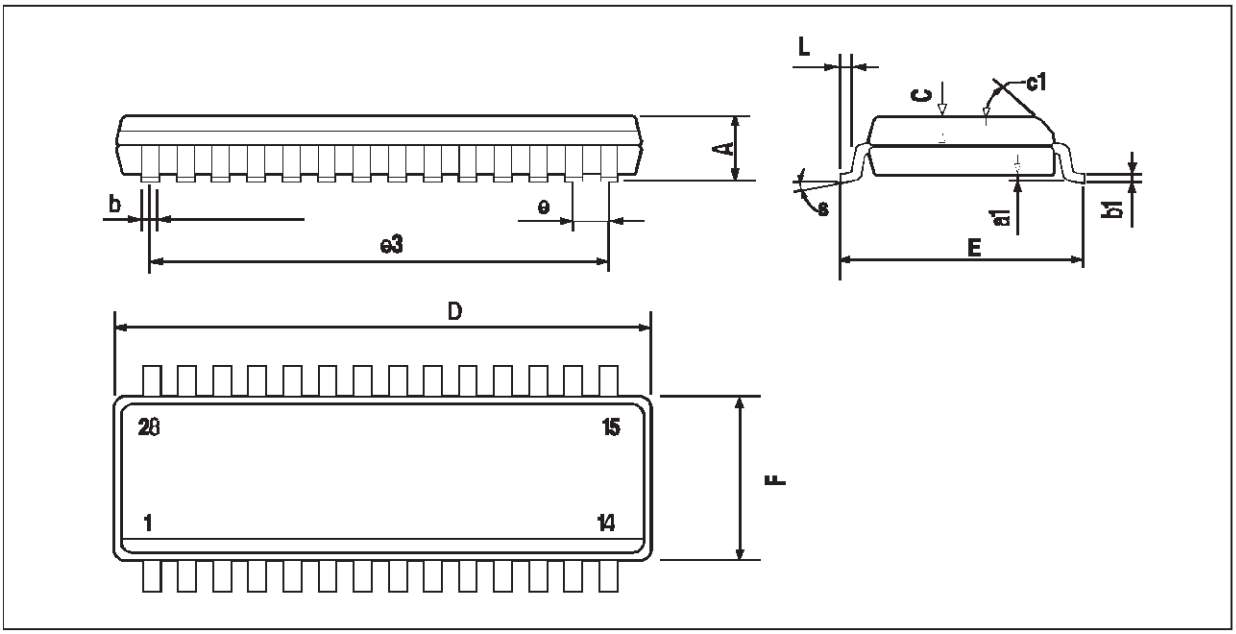
13 - APPLICATION DIAGRAM

Figure 15.



PACKAGE MECHANICAL DATA

28 PINS - PLASTIC MICROPACKAGE (SO)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		
L	0.4		1.27	0.016		0.299
S	8° (Max.)					0.050