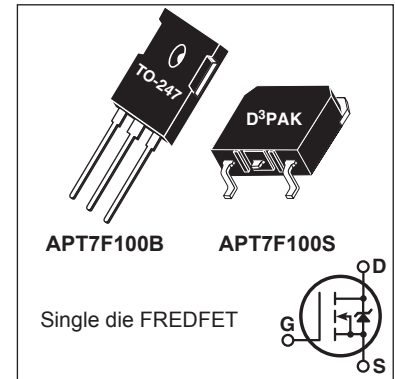


N-Channel FREDFET

POWER MOS 8® is a high speed, high voltage N-channel switch-mode power MOSFET. This 'FREDFET' version has a drain-source (body) diode that has been optimized for high reliability in ZVS phase shifted bridge and other circuits through reduced t_{rr} , soft recovery, and high recovery dv/dt capability. Low gate charge, high gain, and a greatly reduced ratio of C_{rss}/C_{iss} result in excellent noise immunity and low switching loss. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control di/dt during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency.



FEATURES

- Fast switching with low EMI
- Low t_{rr} for high reliability
- Ultra low C_{rss} for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant 

TYPICAL APPLICATIONS

- ZVS phase shifted and other full bridge
- Half bridge
- PFC and other boost converter
- Buck converter
- Single and two switch forward
- Flyback

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	7	A
	Continuous Drain Current @ $T_C = 100^\circ\text{C}$	5	
I_{DM}	Pulsed Drain Current ^①	27	
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ^②	415	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	4	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$			290	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.43	$^\circ\text{C/W}$
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.15		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	$^\circ\text{C}$
T_L	Soldering Temperature for 10 Seconds (1.6mm from case)			300	
W_T	Package Weight		0.22		oz
			6.2		g
Torque	Mounting Torque (TO-247 Package), 6-32 or M3 screw			10	in-lbf
				1.1	N-m

Static Characteristics

$T_J = 25^{\circ}\text{C}$ unless otherwise specified

APT7F100B S

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	1000			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to $25^{\circ}\text{C}, I_D = 250\mu A$		1.15		V/ $^{\circ}\text{C}$
$R_{DS(on)}$	Drain-Source On Resistance ^③	$V_{GS} = 10V, I_D = 4A$		1.76	2.0	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 0.5mA$	2.5	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient			-10		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 1000V$ $V_{GS} = 0V$			250 1000	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 30V$			± 100	nA

Dynamic Characteristics

$T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	$V_{DS} = 50V, I_D = 4A$		7.5		S
C_{iss}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1MHz$		1800		pF
C_{rss}	Reverse Transfer Capacitance			25		
C_{oss}	Output Capacitance			158		
$C_{o(cr)}^{④}$	Effective Output Capacitance, Charge Related	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 670V$		65		
$C_{o(er)}^{⑤}$	Effective Output Capacitance, Energy Related			33		
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10V, I_D = 4A,$ $V_{DS} = 500V$		58		nC
Q_{gs}	Gate-Source Charge			10		
Q_{gd}	Gate-Drain Charge			27		
$t_{d(on)}$	Turn-On Delay Time	Resistive Switching $V_{DD} = 670V, I_D = 4A$ $R_G = 10\Omega^{⑥}, V_{GG} = 15V$		24		ns
t_r	Current Rise Time			26		
$t_{d(off)}$	Turn-Off Delay Time			77		
t_f	Current Fall Time			22		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			7	A
I_{SM}	Pulsed Source Current (Body Diode) ^①				27	
V_{SD}	Diode Forward Voltage	$I_{SD} = 4A, T_J = 25^{\circ}\text{C}, V_{GS} = 0V$			1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 4A^{③}$ $di_{SD}/dt = 100A/\mu s$ $V_{DD} = 100V$	$T_J = 25^{\circ}\text{C}$	133	152	ns
			$T_J = 125^{\circ}\text{C}$	209	251	
Q_{rr}	Reverse Recovery Charge		$T_J = 25^{\circ}\text{C}$	.56		μC
			$T_J = 125^{\circ}\text{C}$	1.2		
I_{rrm}	Reverse Recovery Current		$T_J = 25^{\circ}\text{C}$	7		A
			$T_J = 125^{\circ}\text{C}$	9		
dv/dt	Peak Recovery dv/dt	$I_{SD} \leq 4A, di/dt \leq 1000A/\mu s, V_{DD} = 500V,$ $T_J = 125^{\circ}\text{C}$			25	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at $T_J = 25^{\circ}\text{C}, L = 53mH, R_G = 25\Omega, I_{AS} = 4A$.

③ Pulse test: Pulse Width < 380 μs , duty cycle < 2%.

④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with $V_{DS} = 67\%$ of $V_{(BR)DSS}$. To calculate $C_{o(er)}$ for any value of V_{DS} less than $V_{(BR)DSS}$, use this equation: $C_{o(er)} = -3.43E-8/V_{DS}^2 + 1.44E-8/V_{DS} + 5.38E-11$.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

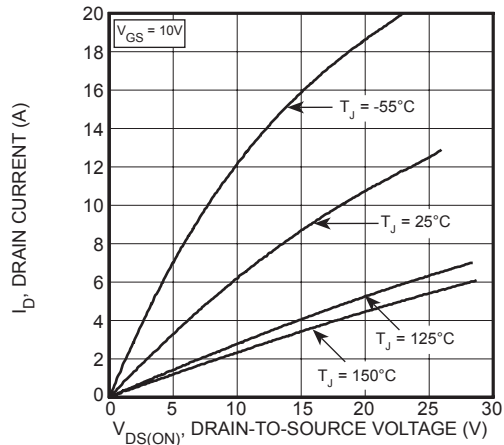


Figure 1, Output Characteristics

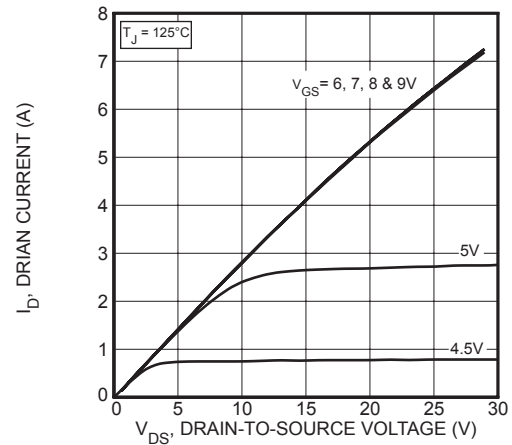


Figure 2, Output Characteristics

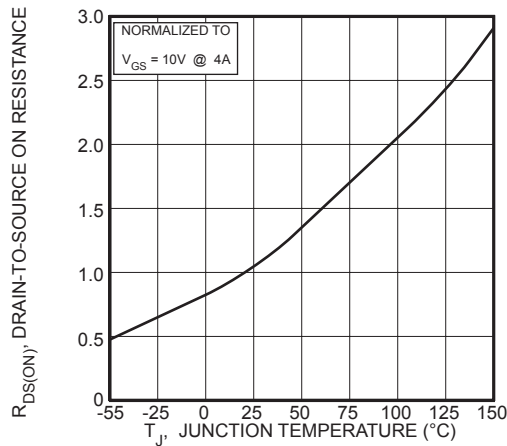
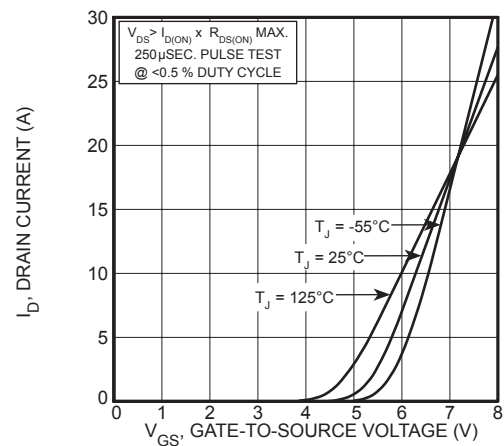
Figure 3, $R_{DS(ON)}$ vs Junction Temperature

Figure 4, Transfer Characteristics

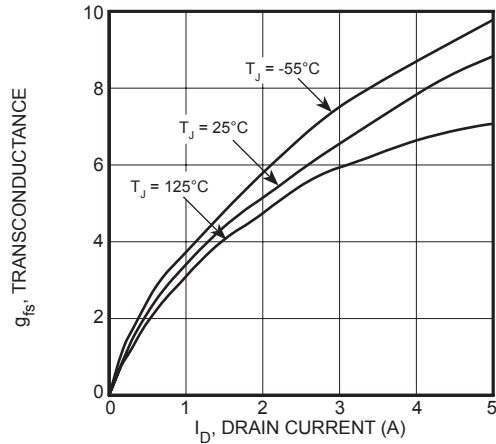


Figure 5, Gain vs Drain Current

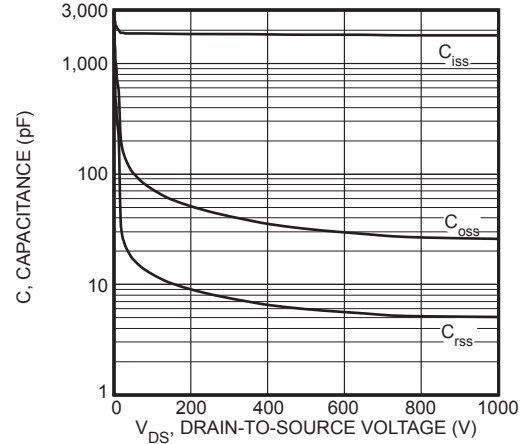


Figure 6, Capacitance vs Drain-to-Source Voltage

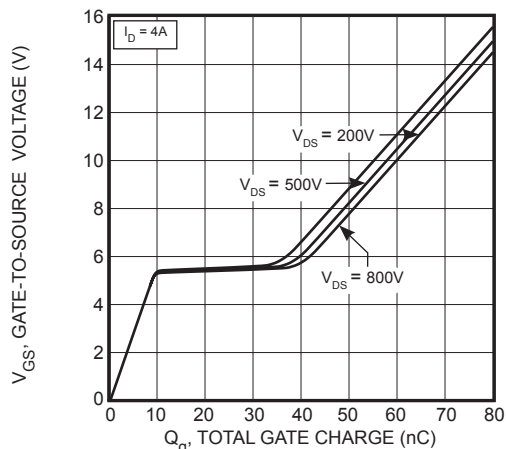


Figure 7, Gate Charge vs Gate-to-Source Voltage

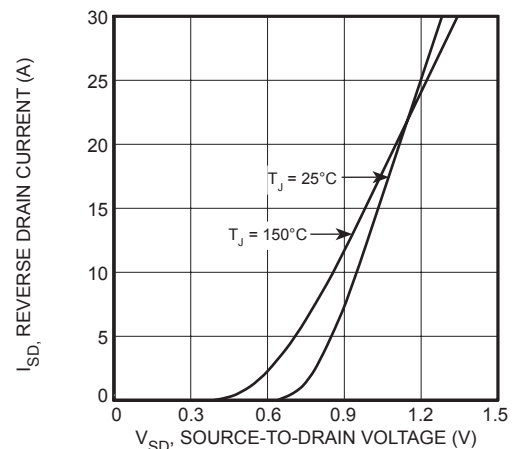


Figure 8, Reverse Drain Current vs Source-to-Drain Voltage

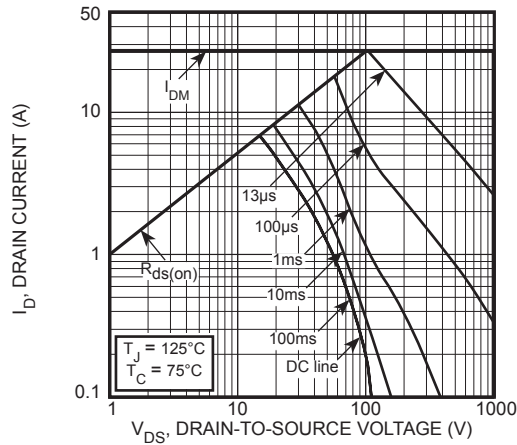


Figure 9, Forward Safe Operating Area

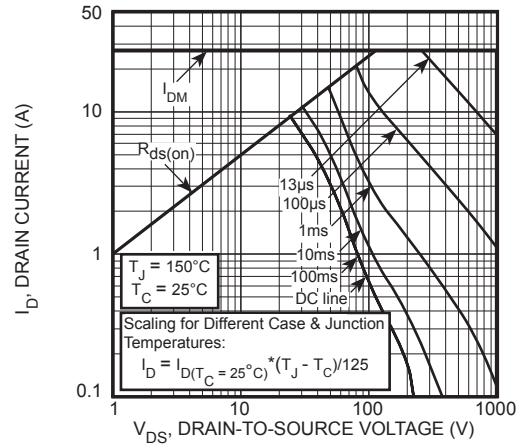


Figure 10, Maximum Forward Safe Operating Area

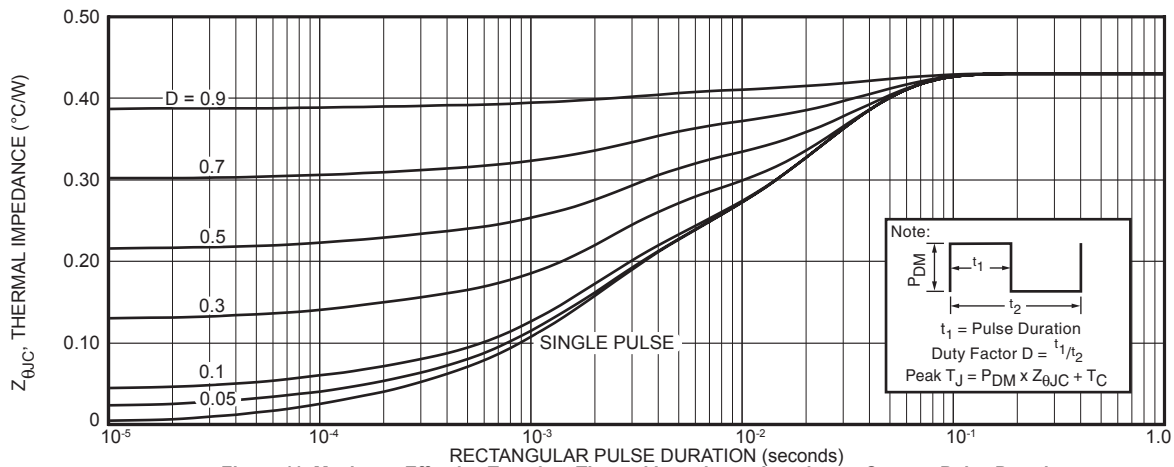
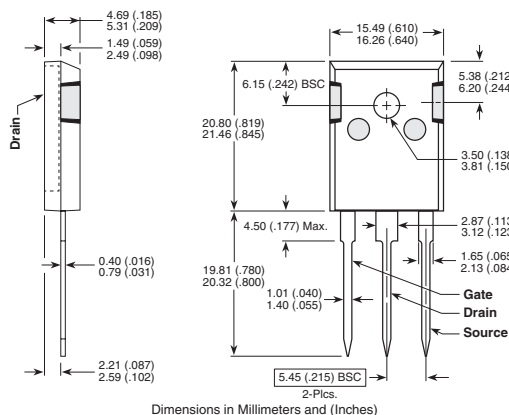


Figure 11, Maximum Effective Transient Thermal Impedance Junction-to-Case vs Pulse Duration

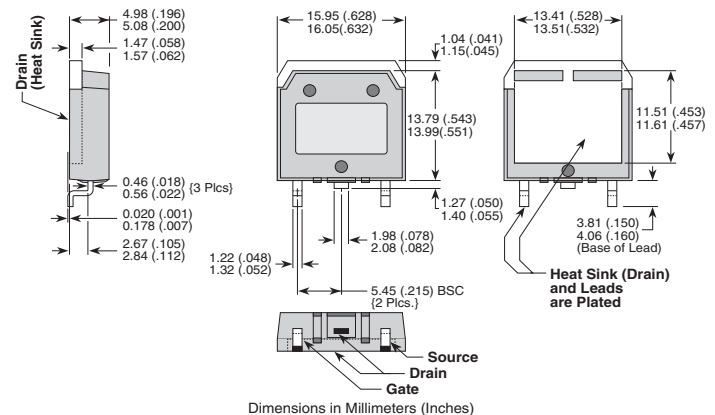
TO-247 (B) Package Outline



Dimensions in Millimeters and (Inches)

D³PAK Package Outline

e1 100% Sn Plated



Dimensions in Millimeters (Inches)

Microsemi's products are covered by one or more of U.S. patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 6,939,743, 7,352,045 5,283,201 5,801,417 5,648,283 7,196,634 6,664,594 7,157,886 6,939,743 7,342,262 and foreign patents. US and Foreign patents pending. All Rights Reserved.