



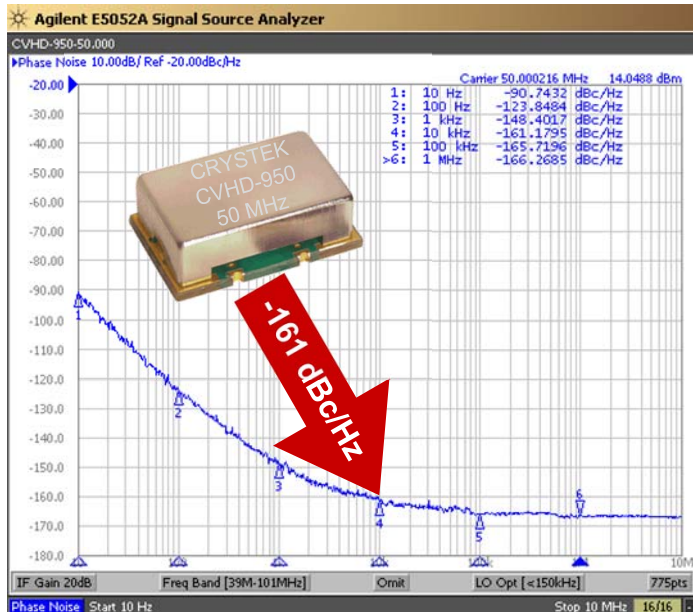
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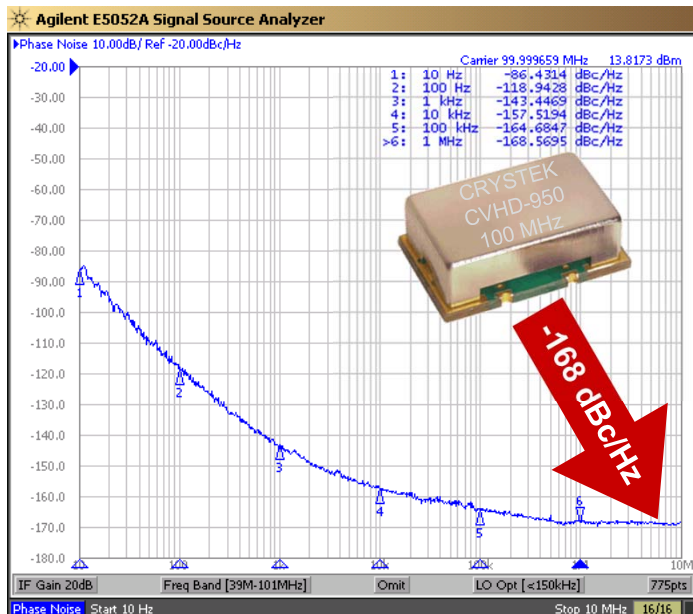
# CVHD-950 VCXO Ultra-Low Phase Noise Oscillators

**CVHD-950 Model**  
**9×14 mm SMD, 3.3V, CMOS**

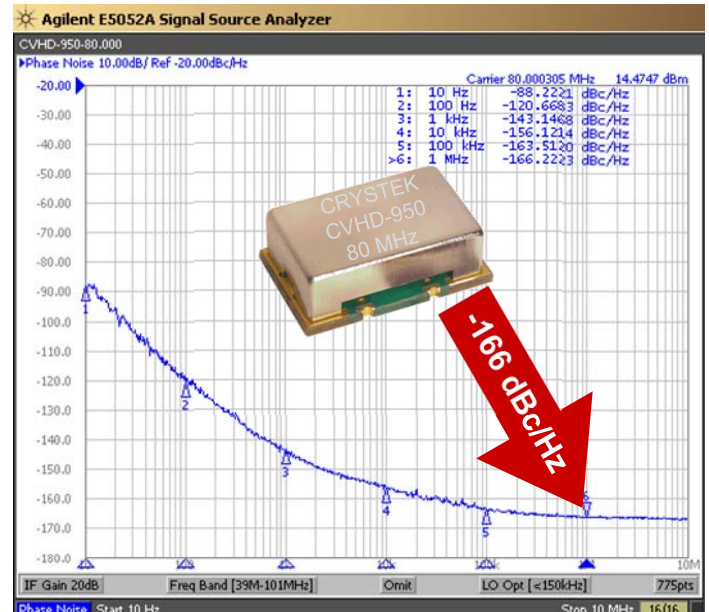
**50 MHz HCMOS 3.3V**



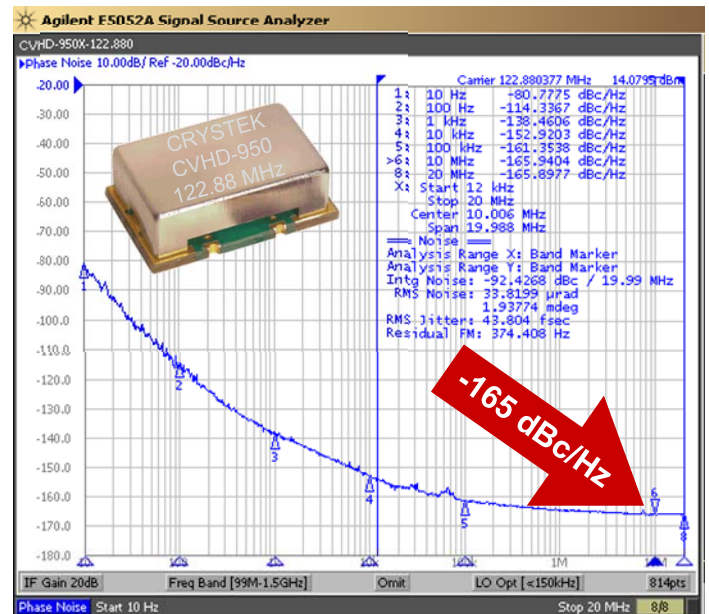
**100 MHz HCMOS 3.3V**



**80 MHz HCMOS 3.3V**



**122.880 MHz HCMOS 3.3V**



**Model CVHD-950 is a 40 MHz to 130 MHz CMOS Voltage Controlled Crystal Oscillator. High Q crystal and 3<sup>rd</sup> overtone technology provides Ultra-Low Phase Noise and Low-Jitter performance with a CMOS output. Features include -168 dBc/Hz phase noise floor with 3.3Vdc input voltage, -40°C to +85°C operating temperature, and 9×14 mm SMT package. The oscillator has no sub-harmonics.**

**Applications include High Definition TV, Avionics  
Low Phase Signal Sources, and Test and Measurement.**

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# CVHD-950 VCXO

## Ultra-Low Phase Noise Oscillators

**CVHD-950 Model**  
**9×14 mm SMD, 3.3V, CMOS**

|                               |                                                                               |
|-------------------------------|-------------------------------------------------------------------------------|
| Frequency Range:              | 40 MHz to 130 MHz                                                             |
| Temperature Range:            | 0°C to +70°C (standard)                                                       |
| (Option M)                    | -20°C to +70°C                                                                |
| (Option X)                    | -40°C to +85°C                                                                |
| Storage:                      | -45°C to 90°C                                                                 |
| Input Voltage:                | 3.3V ±0.3V                                                                    |
| Supply Pushing:               | 1.2ppm/V Typical                                                              |
| Input Current:                | 15mA Typical, 25mA Max                                                        |
| Output:                       | CMOS                                                                          |
| Symmetry:                     | 45/55% Max @ 50%Vdd                                                           |
| Rise/Fall Time:               | 3nsec Max @ 20% to 80% Vdd                                                    |
| Logic:                        | "0" = 10% Vdd Max<br>"1" = 90% Vdd Min                                        |
| Load:                         | 15pF                                                                          |
| Output Current:               | ±24mA Max                                                                     |
| Input:                        |                                                                               |
| Modulation Bandwidth:         | >10kHz @ -3dB                                                                 |
| Input Impedance:              | 51 kΩ                                                                         |
| Control Voltage:              | 1.65V ±1.65V                                                                  |
| Tuning Sensitivity:           | +25ppm/V Typical                                                              |
| Frequency Pulling:            | ±20ppm APR Min<br>(Inclusive of frequency stability, calibration, and aging.) |
| Linearity:                    | ±5% Max                                                                       |
| Phase Jitter (12kHz~20MHz):   | 40 fsec Typical @100MHz                                                       |
| Typical Phase Noise (100MHz): |                                                                               |
| 1kHz                          | -140 dBc/Hz                                                                   |
| 10kHz                         | -155 dBc/Hz                                                                   |
| 100kHz                        | -164 dBc/Hz                                                                   |
| 1MHz                          | -166 dBc/Hz                                                                   |
| Phase Noise Floor:            | -166 dBc/Hz Typical, -162 dBc/Hz Max                                          |
| Sub-harmonics:                | None                                                                          |
| Aging:                        | <3ppm 1 <sup>st</sup> year, <1ppm thereafter                                  |



Part Number Example: CVHD-950X-100.000 = 3.3V, 45/55, -40°C to +85°C (±20ppmAPR), 100 MHz

| Absolute Maximum Ratings |        |      |
|--------------------------|--------|------|
| Parameter                | Rating | Unit |
| Input Supply Voltage     | +6.0   | V    |
| Input Control Voltage    | +10.0  | V    |

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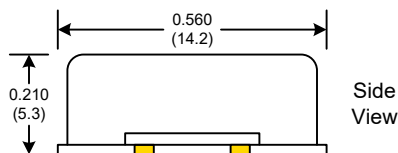
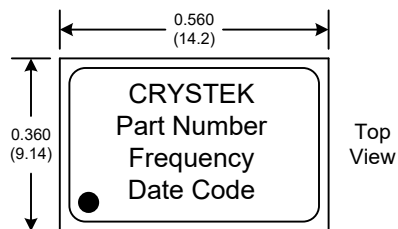
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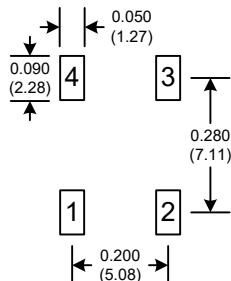
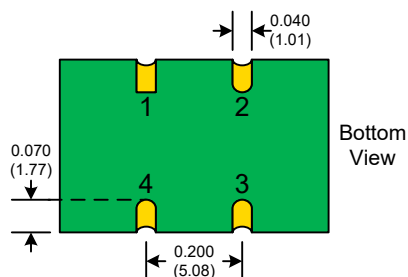
# CVHD-950 VCXO

## Ultra-Low Phase Noise Oscillators

**CVHD-950 Model**  
9×14 mm SMD, 3.3V, CMOS



### SUGGESTED PAD LAYOUT



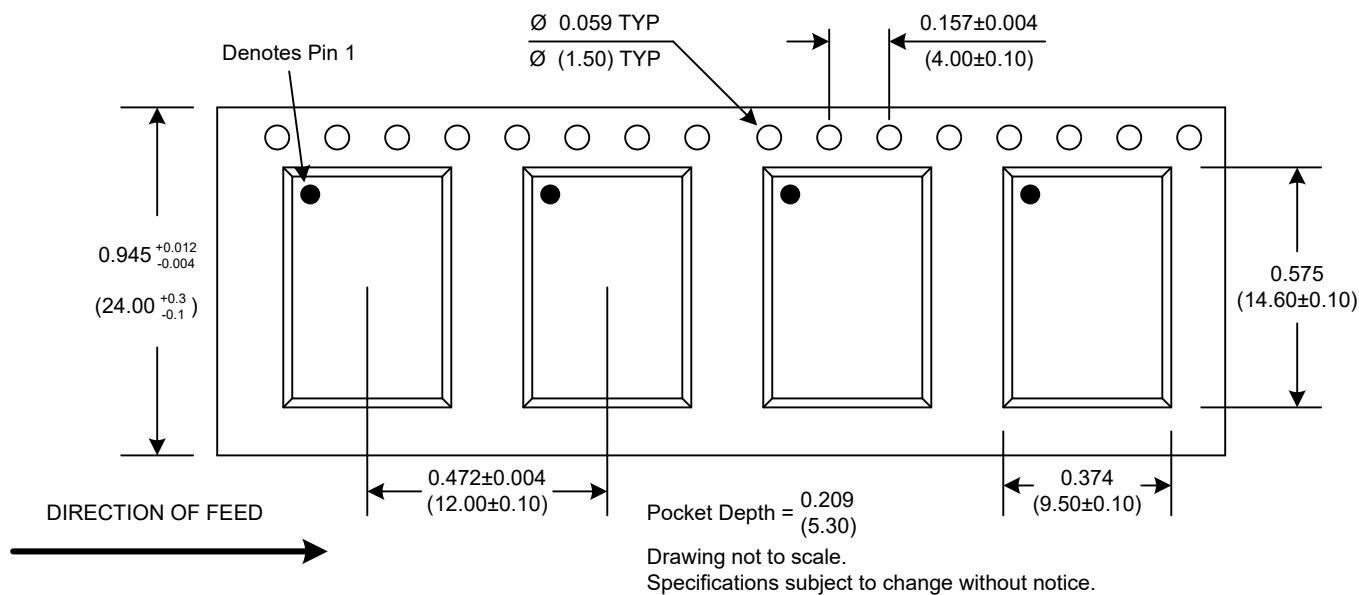
**RECOMMENDED REFLOW SOLDERING PROFILE**  
900034 (See App Note listed on website)

<http://www.crystek.com/specification/reflow/900034.pdf>

| Pad | Connection   |
|-----|--------------|
| 1   | Volt Control |
| 2   | GND          |
| 3   | OUT          |
| 4   | Vdd          |

**PAD FINISH:** Immersion Gold (ENIG); 5 micro inches maximum

### TAPE AND REEL



#### Mechanical:

Shock: MIL-STD-883, Method 2002, Condition B  
Solderability: MIL-STD-883, Method 2003  
Vibration: MIL-STD-883, Method 2007, Condition A  
Solvent Resistance: MIL-STD-202, Method 215  
Resistance to Soldering Heat: MIL-STD-202, Method 210, Condition I or J

#### Environmental:

Thermal Shock: MIL-STD-883, Method 1011, Condition A  
Moisture Resistance: MIL-STD-883, Method 1004

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