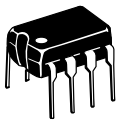
CAT24WC66

64-Kb I²C Serial EEPROM with Partial Array Write Protection

ON Semiconductor®

http://onsemi.com



PDIP–8
L SUFFIX
CASE 646AA

SOIC–8
W or X SUFFIX
CASE 751BD

Description

The CAT24WC66 is a 64−Kb Serial CMOS EEPROM internally organized as 8192 words of 8 bits each. ON Semiconductor's advanced CMOS technology substantially reduces device power requirements. The CAT24WC66 features a 32−byte page write buffer. The device operates via the I²C bus serial interface and is available in 8−pin PDIP or 8−pin SOIC packages.

Features

- 400 kHz I²C Bus
- 1.8 V to 5.5 V Supply Voltage Range
- Cascadable for up to Eight Devices
- 32−byte Page Write Buffer
- Self−timed Write Cycle with Auto−clear
- Schmitt Trigger Inputs for Noise Protection
- Write Protection
  – Top 1/4 Array Protected when WP at V_{IH}
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Automotive Temperature Ranges
- This Device is Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

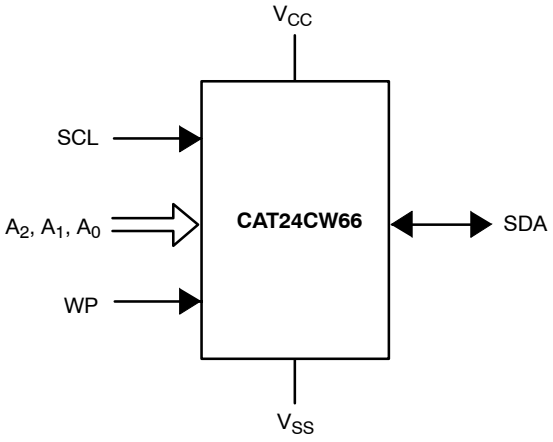
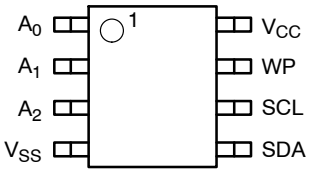
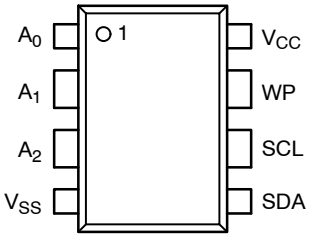


Figure 1. Functional Symbol

PIN CONFIGURATIONS



DIP Package (L)



SOIC Package (W, X)

PIN FUNCTION

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	–55 to +125	°C
Storage Temperature	–65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	–2.0 to V_{CC} + 2.0	V
V_{CC} with Respect to Ground	–2.0 to 7.0	V
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Lead Soldering Temperature (10 secs)	300	°C
Output Short Circuit Current (Note 2)	100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The minimum DC input voltage is –0.5 V. During transitions, inputs may undershoot to –2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.
2. Output shorted for no more than one second. No more than one output shorted at a time.

Table 2. REABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
NEND (Note 3)	Endurance	MIL–STD–883, Test Method 1033	1,000,000		Cycles / Byte
TDR (Note 3)	Data Retention	MIL–STD–883, Test Method 1008	100		Years
VZAP (Note 3)	ESD Susceptibility	MIL–STD–883, Test Method 3015	2000		Volts
ILTH (Notes 3, 4)	Latch–up	JEDEC Standard 17	100		mA

3. This parameter is tested initially and after a design or process change that affects the parameter.
4. Latch–up protection is provided for stresses up to 100 mA on address and data pins from –1 V to V_{CC} + 1 V.

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.8 V to 5.5 V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	f_{SCL} = 100 kHz			3	mA
I_{SB} (Note 5)	Standby Current (V_{CC} = 5 V)	V_{IN} = GND or V_{CC}			1	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			10	μA
V_{IL}	Input Low Voltage		–1		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage (V_{CC} = +3.0 V)	I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Voltage(V_{CC} = +1.8 V)	I_{OL} = 1.5 mA			0.5	V

5. Maximum standby current (ISB) = 10 μA for the Automotive and Extended Automotive temperature range.

Table 4. CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{I/O}$ (Note 3)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0 V			8	pF
C_{IN} (Note 3)	Input Capacitance (A0, A1, A2, SCL, WP)	V_{IN} = 0 V			6	pF

Table 5. A.C. CHARACTERISTICS (V_{CC} = 1.8 V to 5.5 V, unless otherwise specified. Output Load is 1TTL Gate and 100 pF.)

Symbol	Parameter	1.8 V – 2.5 V		4.5 V – 5.5 V		Units
		Min	Max	Min	Max	
MEMORY READ & WRITE CYCLE LIMITS						
FSCL	Clock Frequency		100		400	kHz
T_I (Note 6)	Noise Suppression Time Constant at SCL, SDA Inputs		200		200	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		1	μs
t_{BUF} (Note 6)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		μs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		μs
t_{LOW}	Clock Low Period	4.7		1.2		μs
t_{HIGH}	Clock High Period	4		0.6		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	50		50		ns
t_R (Note 6)	SDA and SCL Rise Time		1		0.3	μs
t_F (Note 6)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		μs
t_{DH}	Data Out Hold Time	100		100		ns

6. This parameter is tested initially and after a design or process change that affects the parameter.

Table 6. POWER−UP TIMING (Notes 6, 7)

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power−Up to Read Operation			1	ms
t_{PUW}	Power−Up to Write Operation			1	ms

7. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 7. WRITE CYCLE LIMITS

Symbol	Parameter	Min	Typ	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Functional Description

The CAT24WC66 supports the I^2C Bus data transmission protocol. This Inter−Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24WC66 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

Pin Description

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs

These pins are hardwired or left unconnected (for hardware compatibility with CAT24WC16). When hardwired, up to eight CAT24WC66 devices may be addressed on a single bus system (refer to Device Addressing). When the pins are left unconnected, the default values are zeros.

WP: Write Protect

This input, when tied to GND, allows write operations to the entire memory. When this pin is tied to V_{CC}, the top 1/4 array of memory is write protected. When left floating, memory is unprotected.

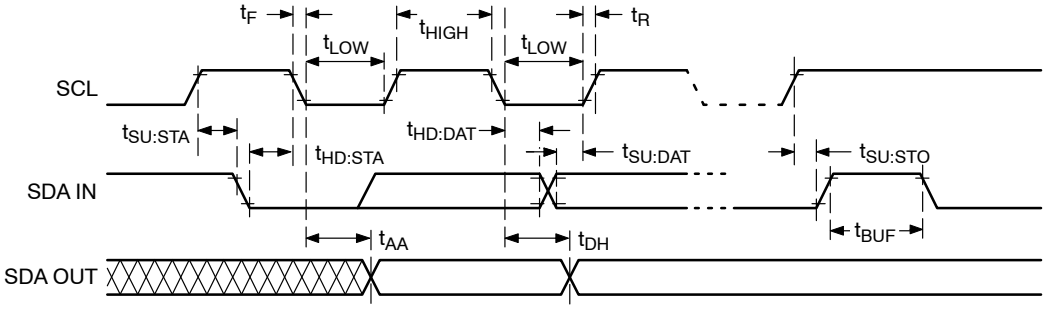


Figure 2. Bus Timing

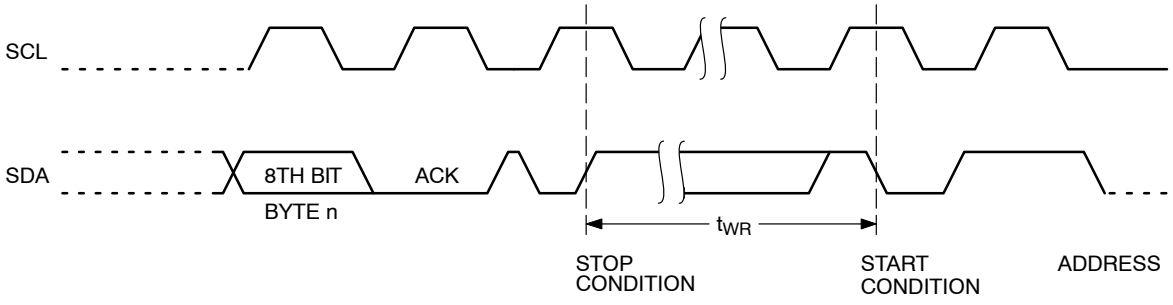


Figure 3. Write Cycle Timing

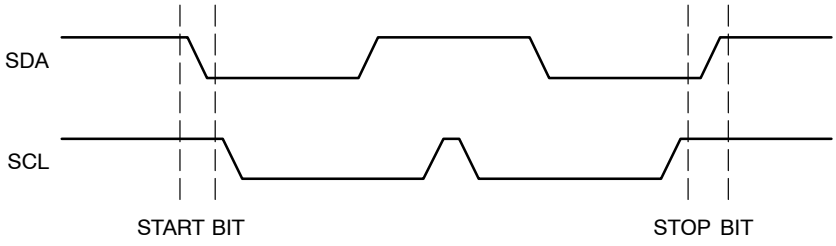


Figure 4. Start/Stop Timing

I²C Bus Protocol

The features of the I²C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24WC66 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

The bus Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8−bit slave address are fixed as 1010 (Figure 6). The next three bits (A2, A1, A0) are the device address bits; up to eight 64K devices may to be connected to the same bus. These bits must compare to the hardwired input pins, A2, A1 and A0. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24WC66 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24WC66 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24WC66 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8−bit byte.

When the CAT24WC66 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24WC66 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a stop condition to return the CAT24WC66 to the standby power mode and place the device in a known state.

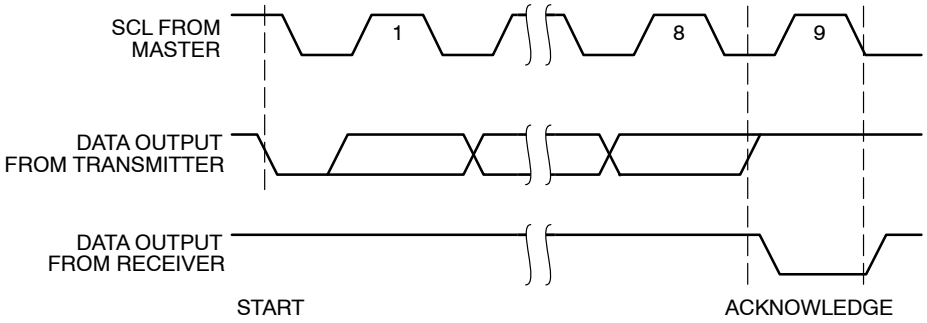


Figure 5. Acknowledge Timing

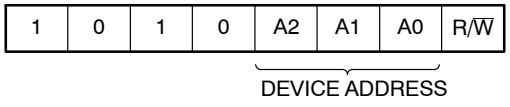


Figure 6. Slave Address Bits

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends two 8−bit address words that are to be written into the address pointers of the CAT24WC66. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24WC66 acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to nonvolatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24WC66 writes up to 32 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 31 additional bytes. After each byte has been transmitted, CAT24WC66 will respond with an acknowledge, and internally increment the five low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 32 bytes before sending the STOP condition, the address counter ‘wraps around’, and previously transmitted data will be overwritten.

When all 32 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT24WC66 in a single write cycle.

Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host’s write operation, CAT24WC66 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If CAT24WC66 is still busy with the write operation, no ACK will be returned. If CAT24WC66 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection

The Write Protection feature allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to VCC, the top 1/4 of the memory array (locations 1800H to 1FFF) is protected and becomes read only. The CAT24WC66 will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device’s failure to send an acknowledge after the first byte of data is received.

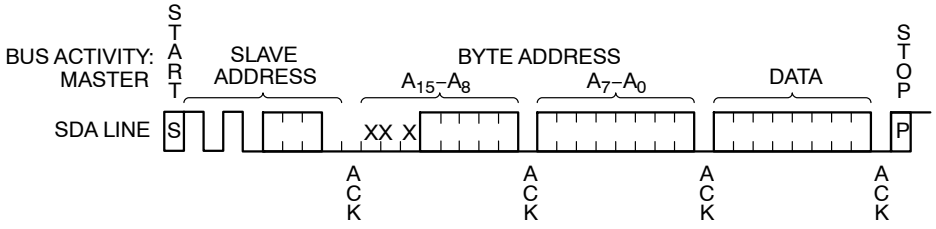


Figure 7. Byte Write Timing

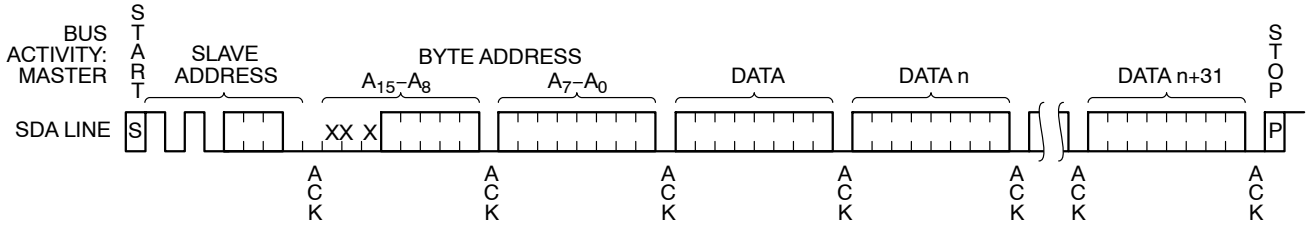


Figure 8. Page Write Timing

READ OPERATIONS

The READ operation for the CAT24WC66 is initiated in the same manner as the write operation with one exception, that R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/ Random READ and Sequential READ.

Immediate/Current Address Read

The CAT24WC66’s address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from

address N+1. If N=E (where E=8191), then the counter will ‘wrap around’ to address 0 and continue to clock out data. After the CAT24WC66 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8 bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a ‘dummy’ write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After CAT24WC66 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT24WC66 then responds with its acknowledge and sends the 8−bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24WC66 sends the initial 8−bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24WC66 will continue to output an 8−bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from CAT24WC66 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24WC66 address bits so that the entire memory array can be read during one operation. If more than E (where E=8191) bytes are read out, the counter will ‘wrap around’ and continue to clock out data bytes.

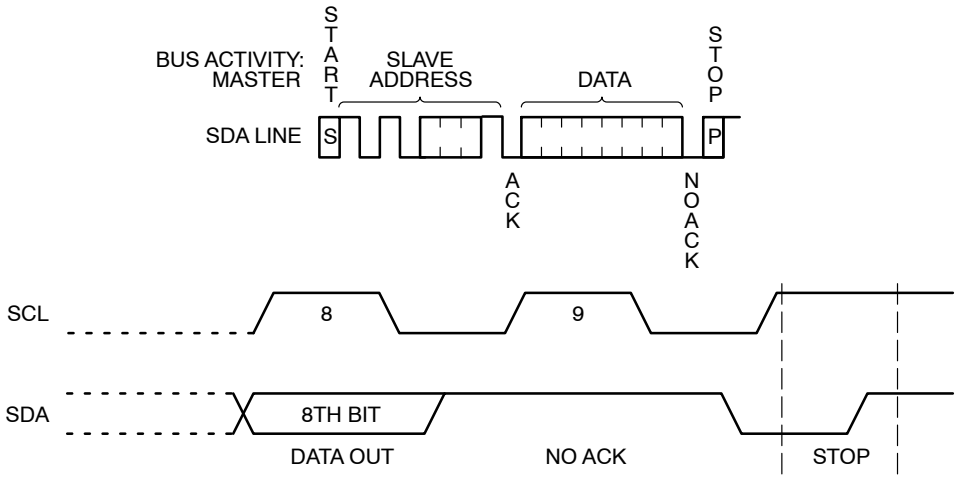


Figure 9. Immediate Address Read Timing

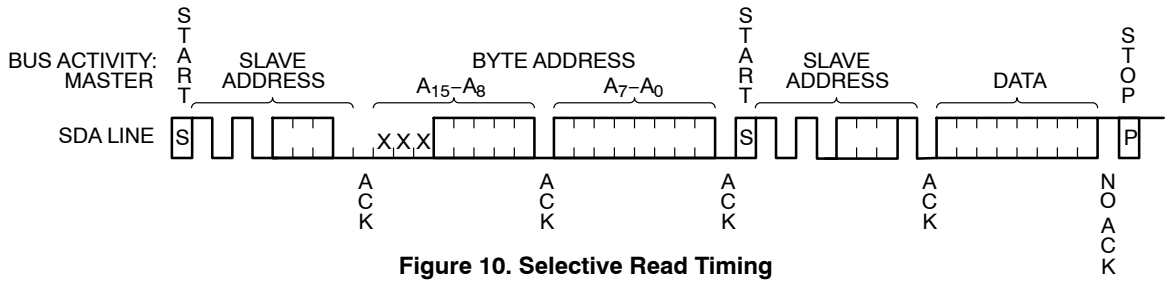


Figure 10. Selective Read Timing

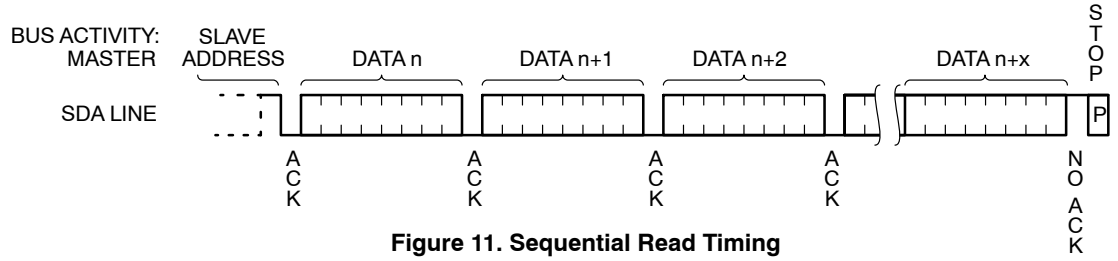
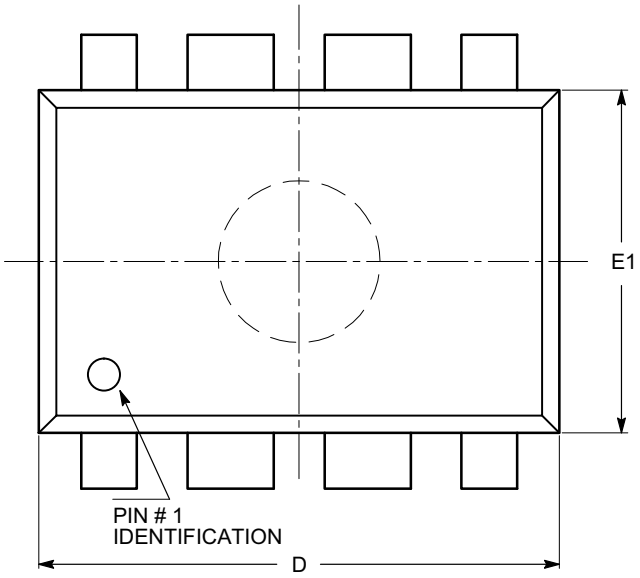


Figure 11. Sequential Read Timing

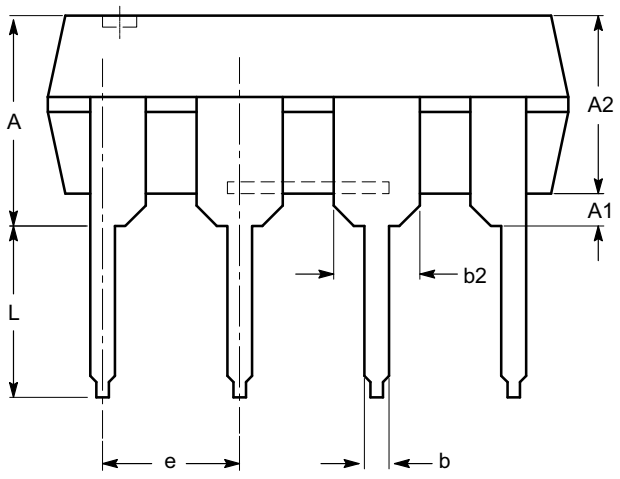
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

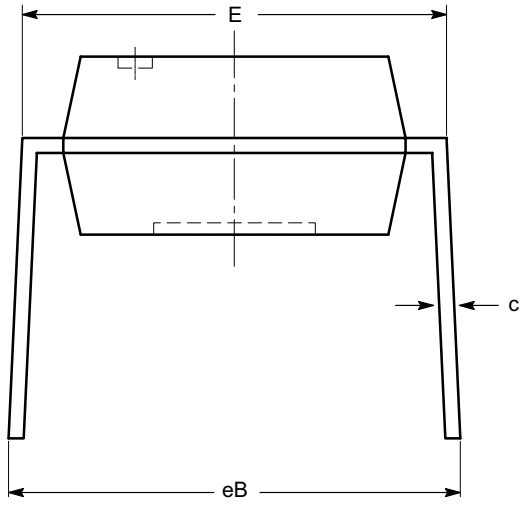


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

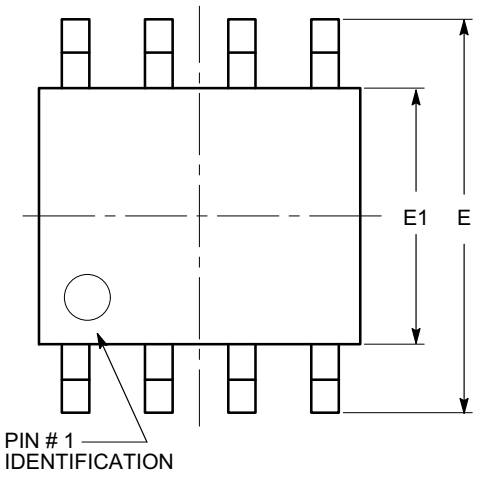


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

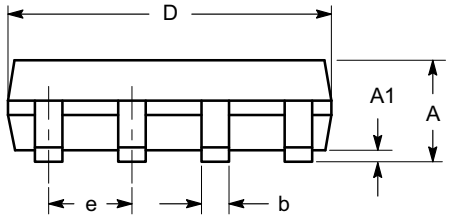
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

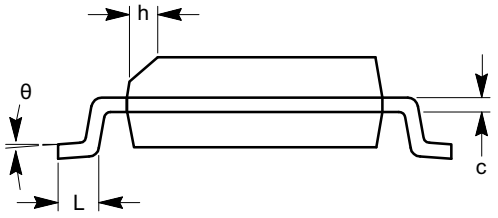


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

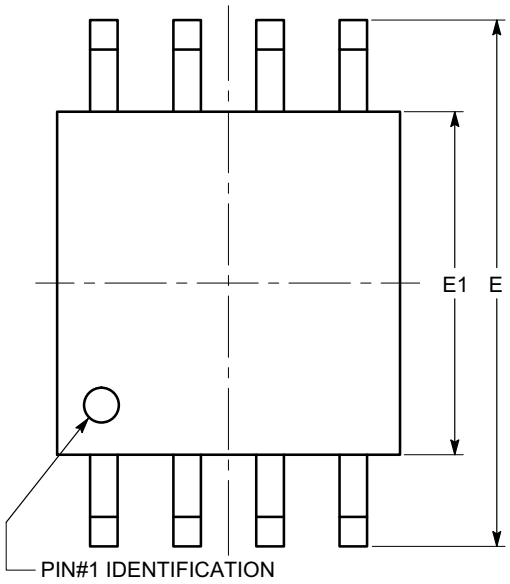


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

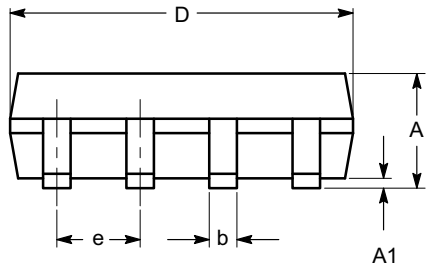
PACKAGE DIMENSIONS

SOIC−8, 208 mils
CASE 751BE−01
ISSUE O

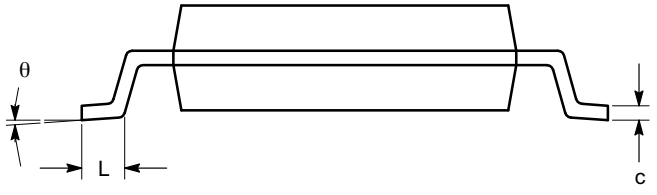


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			2.03
A1	0.05		0.25
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e		1.27 BSC	
L	0.51		0.76
θ	0º		8º



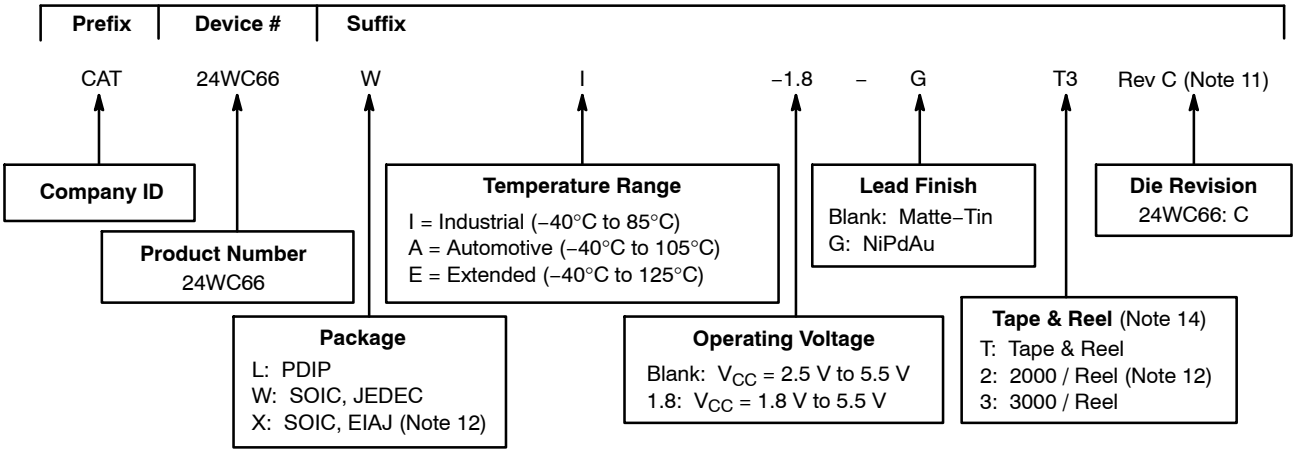
SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with EIAJ EDR-7320.

Example of Ordering Information



8. All packages are RoHS-compliant (Lead-free, Halogen-free).
9. The standard lead finish is NiPdAu.
10. The device used in the above example is a CAT24W66WI−1.8−GT3 (SOIC, Industrial Temperature, 1.8 to 5.5 V Operating Voltage, NiPdAu, Tape & Reel).
11. Product die revision letter is marked on top of the package as a suffix to the production date code (e.g. AYWWC). For additional information, please contact your ON Semiconductor sales office.
12. For SOIC, EIAJ (X) package the standard lead finish is Matte-Tin. This package is available in 2000 pcs/reel, i.e. CAT24WC66XI-T2.
13. For additional package and temperature options, please contact your nearest ON Semiconductor sales office.
14. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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