TAOS TEXAS ADVANCED OPTOELECTRONIC SOLUTIONS

PC404A Evaluation Module
User's Guide

1. Introduction

The PC404A facilitates evaluation of the TAOS analog linear sensor arrays (TSL201, TSL202, TSL208, TSL1401, TSL1402, TSL1406, TSL1410, or TSL1301) by providing the necessary timing and clock signals to support the on-board imaging device. The designer is then free to investigate the properties and performance of the device without having to design and construct support circuitry. A single 5 volt regulated power supply (and light) are the only inputs required. An oscilloscope is required for observation and analysis of the output signals.

2. Functional Description

The linear sensor array support circuitry of the PC404A consists of an oscillator, a counter/divider and logic to provide the imager with the required clock and integration pulse signals for operation. The oscillator is built around a TLC555 timer. The oscillator output is inverted and fed into divider U10 to provide lower frequency options. The clock frequency may

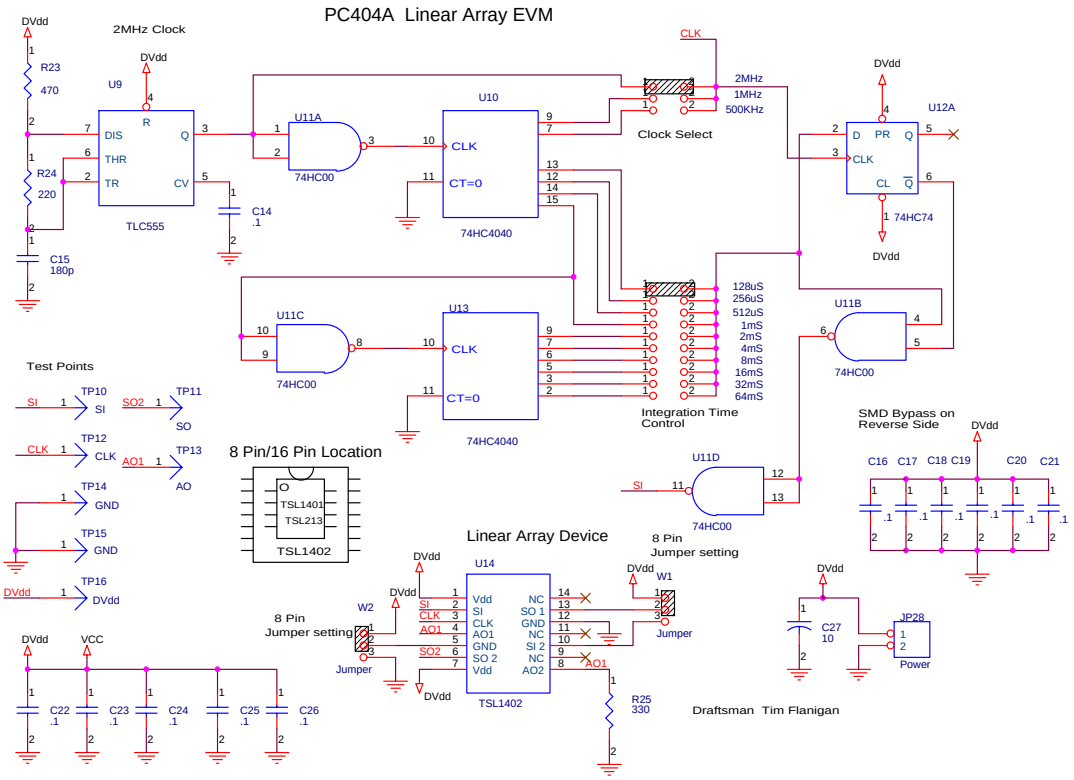

Figure 1 - PC404A Schematic Diagram

be selected from 2 MHz, 1 MHz and 500 kHz by moving the clock select jumper to the desired position (see Figure 1). U10, U11, and U12 generate the serial input (SI) pulse with the proper relationship to the clock (see Figure 2). The sensor integration time, defined by the time between SI clock pulses, may be selected from 128uS to 64mS by placing the jumper at the appropriate location.

The analog output (AO) pin of the linear array is routed to the AO test terminal on the right side of the board, as are SI, clock (CLK), and serial out (SO) signals. The SO signal is generated by the linear array device (applies to TSL202, TSL208, TSL1402, TSL1406, and TSL1410 only). A supply terminal (DVdd) and 2 GND terminals are provided for applying +5 volts and common ground. Power may be applied through terminal block JP28 if desired.

The analog output voltage is directly proportional to the light intensity and the integration time up to the devices saturation level (3.5V typ). The proportionality constant is the responsivity of the device given in ($V*cm^2/uW*sec$). Responsivity is wavelength dependent. For the linear arrays the responsivity will peak at about 770nm.

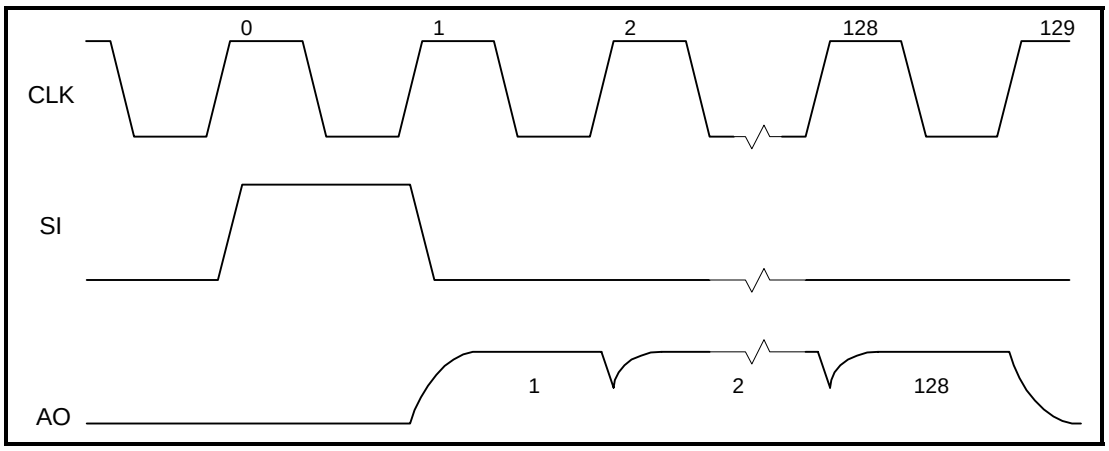

Figure 2 - System Timing (AO output for TSL1401 shown)

3. Operation

To operate the PC404A, apply 5VDC to the board using a regulated lab power supply. Connect an oscilloscope probe to the Ao terminal and the scope ground to one of the GND terminals. For best results, connect another probe to the SI terminal and use that signal to trigger the oscilloscope.

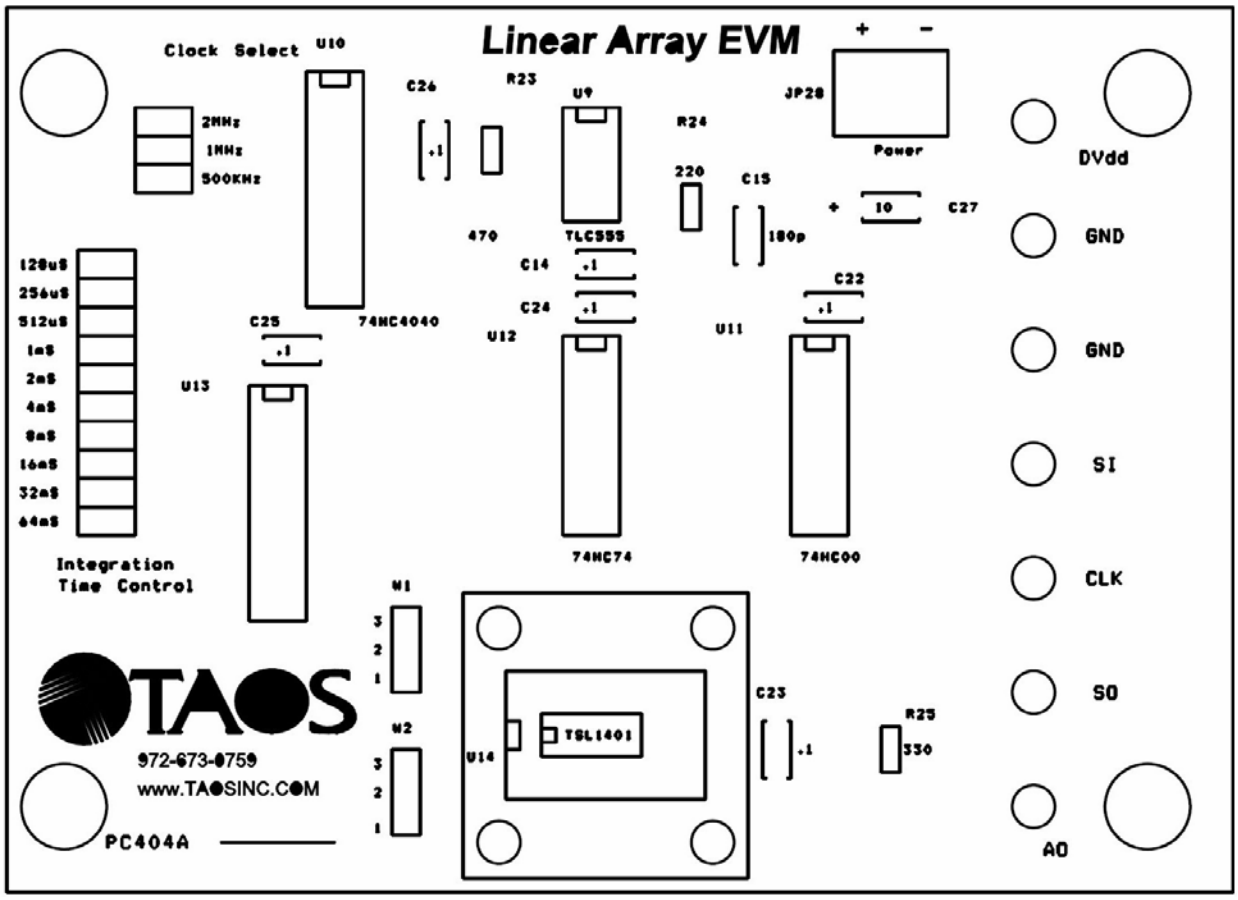

Figure 3 - PC404A Silkscreen (top side)

Table 1 - W1 and W2 Jumper Configuration

DEVICE	JUMPER W1	JUMPER W2
TSL1301 / 1401R / 201R	Open	1-2
TSL1402R / TSL202R	2-3	2-3
TSL1406R / TSL1410R / TSL1412R	2-3	2-3
TSL208	Open	Open
TSL210R	Open	Open
TSL2014	Open	Open