

HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

Check for Samples: [SN65LVDS386/388A/390](#), [SN65LVDT386/388A/390](#), [SN75LVDS386/388A/390](#), [SN75LVDT386/388A/390](#)

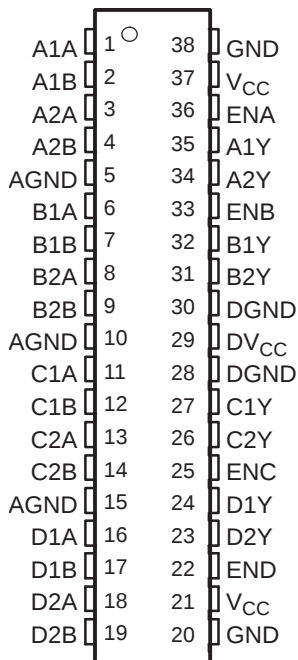
FEATURES

- **Four- ('390), Eight- ('388A), or Sixteen- ('386) Line Receivers Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard**
- **Integrated 110-Ω Line Termination Resistors on LVDT Products**
- **Designed for Signaling Rates**
Signaling Rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)
**Up To
200 Mbps (See Table 1)**
- **SN65 Version's Bus-Terminal ESD Exceeds 15 kV**
- **Operates From a Single 3.3-V Supply**
- **Typical Propagation Delay Time of 2.6 ns**
- **Output Skew 100 ps (Typ) Part-To-Part Skew Is Less Than 1 ns**
- **LVTTTL Levels Are 5-V Tolerant**
- **Open-Circuit Fail Safe**
- **Flow-Through Pinout**
- **Packaged in Thin Shrink Small-Outline Package With 20-mil Terminal Pitch**

DESCRIPTION

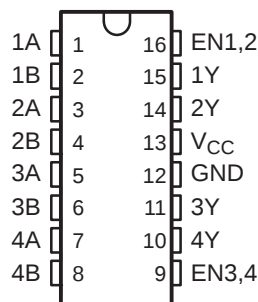
This family of four-, eight-, or sixteen-, differential line receivers (with optional integrated termination) implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3-V supply rail. Any of the eight or sixteen differential receivers provides a valid logical output state with a ± 100 -mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes. Additionally, the high-speed switching of LVDS signals almost always requires the use of a line impedance matching resistor at the receiving end of the cable or transmission media. The LVDT products eliminate this external resistor by integrating it with the receiver.

'LVDS388A, 'LVDT388A
DBT PACKAGE
(TOP VIEW)



See application section for V_{CC} and GND description.

'LVDS390, 'LVDT390
D OR PW PACKAGE
(TOP VIEW)



'LVDS386, 'LVDT386
DGG PACKAGE
(TOP VIEW)

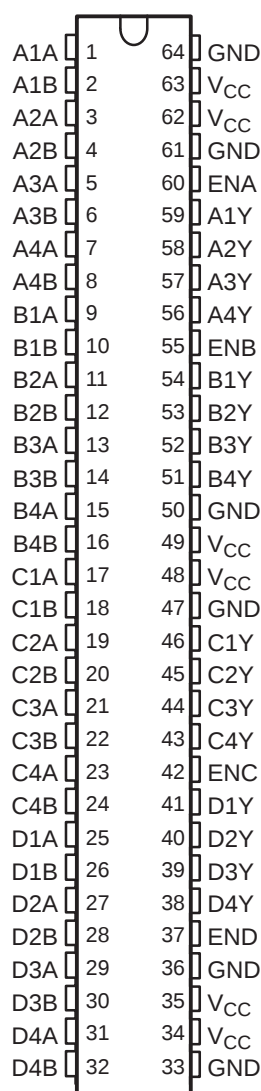


Table 1. Maximum Recommended Operating Speeds

PART NUMBER	ALL BUFFERS ACTIVE
SN65LVDS386, SN75LVDS386	250 Mbps
SN65LVDS388A, SN75LVDS388A	200 Mbps
SN65LVDS390, SN75LVDS390	200 Mbps



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The large number of receivers integrated into the same substrate along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of clock and data for synchronous parallel data transfers. When used with its companion, 8- or 16-channel driver, the SN65LVDS389 or SN65LVDS387, over 300 million data transfers per second in single-edge clocked systems are possible with little power. (Note: The ultimate rate and distance of data transfer depends on the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

AVAILABLE OPTIONS

PART NUMBER	TEMPERATURE RANGE	NUMBER OF RECEIVERS	BUS-PIN ESD	SYMBOLIZATION
SN65LVDS386DGG	–40°C to 85°C	16	15 kV	LVDS386
SN65LVDT386DGG	–40°C to 85°C	16	15 kV	LVDT386
SN75LVDS386DGG	0°C to 70°C	16	4 kV	75LVDS386
SN75LVDT386DGG	0°C to 70°C	16	4 kV	75LVDT386
SN65LVDS388ADBT	–40°C to 85°C	8	15 kV	LVDS388A
SN65LVDT388ADBT	–40°C to 85°C	8	15 kV	LVDT388A
SN75LVDS388ADBT	0°C to 70°C	8	4 kV	75LVDS388A
SN75LVDT388ADBT	0°C to 70°C	8	4 kV	75LVDT388A
SN65LVDS390D	–40°C to 85°C	4	15 kV	LVDS390
SN65LVDS390PW	–40°C to 85°C	4	15 kV	LVDS390
SN65LVDT390D	–40°C to 85°C	4	15 kV	LVDT390
SN65LVDT390PW	–40°C to 85°C	4	15 kV	LVDT390
SN75LVDS390D	0°C to 70°C	4	4 kV	75LVDS390
SN75LVDS390PW	0°C to 70°C	4	4 kV	DS390
SN75LVDT390D	0°C to 70°C	4	4 kV	75LVDT390
SN75LVDT390PW	0°C to 70°C	4	4 kV	DG390

LOGIC DIAGRAM (POSITIVE LOGIC)

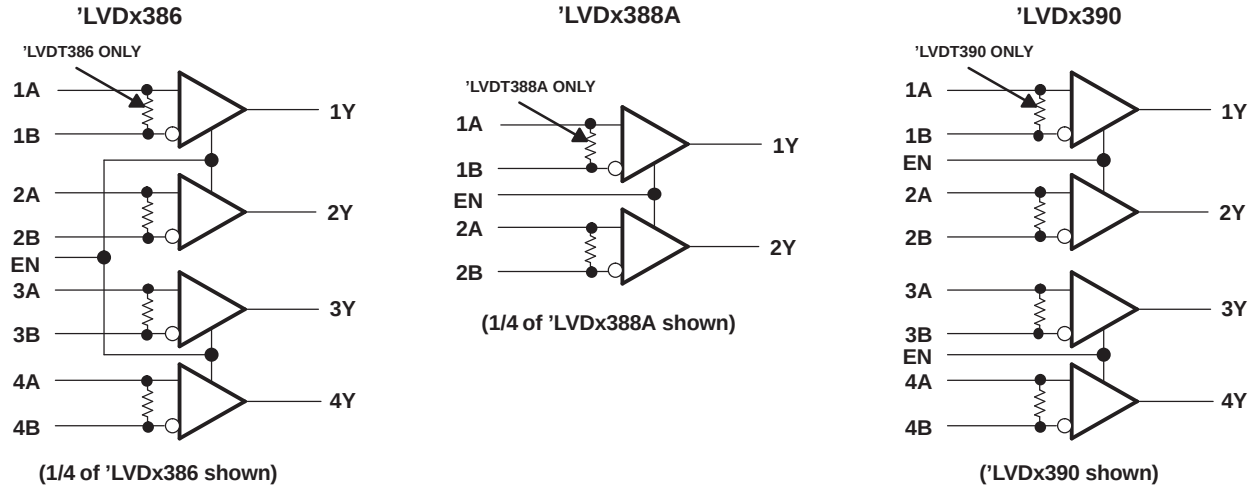
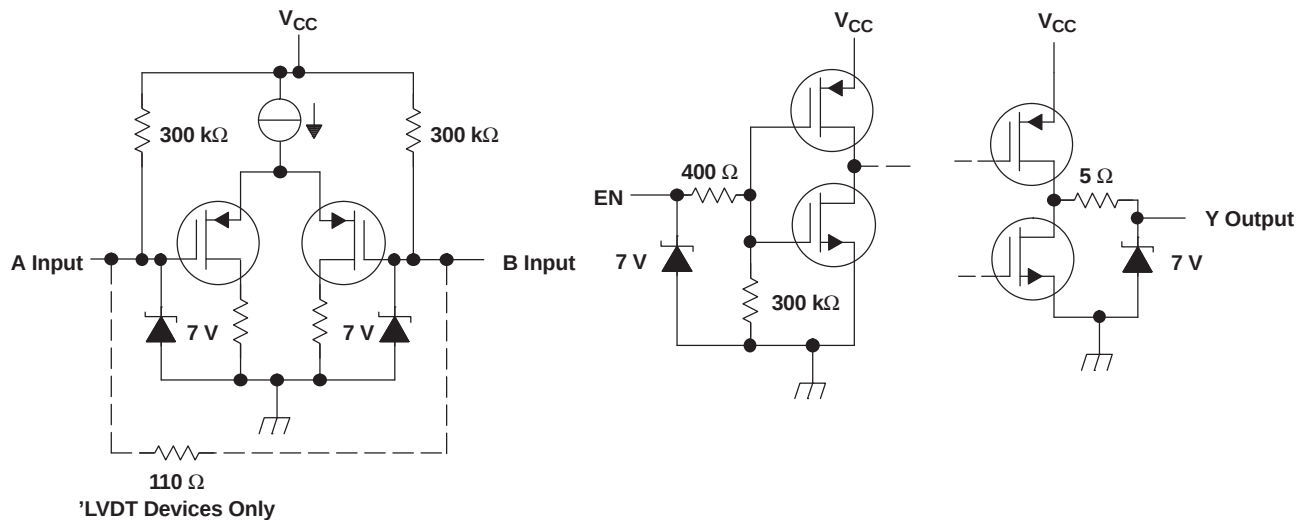


Table 2. FUNCTION TABLE

SNx5LVD386/388A/390 and SNx5LVDT386/388A/390		
DIFFERENTIAL INPUT ⁽¹⁾	ENABLES ⁽¹⁾	OUTPUT ⁽¹⁾
A-B	EN	Y
$V_{ID} \geq 100 \text{ mV}$	H	H
$-100 \text{ mV} < V_{ID} \leq 100 \text{ mV}$	H	?
$V_{ID} \leq -100 \text{ mV}$	H	L
X	L	Z
Open	H	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

			UNITS
V _{CC} ⁽²⁾	Supply voltage range		–0.5 V to 4 V
V _I	Voltage range:	Enables or Y	–0.5 V to 6 V
		A or B	–0.5 V to 4 V
I _O	Output current	Y	±12 mA
V _{ID}	Differential input voltage magnitude	SN65LVDT' or SN75LVDT' only	1 V
	Electrostatic discharge: see ⁽³⁾	SN65' (A, B, and GND)	Class 3, A:15 kV, B: 400 V
		SN75' (A, B, and GND)	Class 2, A:4 kV, B: 400 V
Continuous power dissipation			See Dissipation Rating Table
T _{stg}	Storage temperature range		–65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds			260°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DBT	1071 mW	8.5 mW/°C	688 mW	556 mW
DGG	2094 mW	16.7 mW/°C	1342 mW	1089 mW
PW	774 mW	6.2 mW/°C	496 mW	402 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3	3.3	3.6	V
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
I _O	Output current	Y	– 8		8	mA
V _{ID}	Magnitude of differential input voltage		0.1		0.6	V
V _{IC}	Common-mode input voltage, See Figure 4		$\frac{ V_{ID} }{2}$	$2.4 - \frac{ V_{ID} }{2}$		V
				V _{CC} – 0.8		
T _A	Operating free-air temperature	SN75'	0		70	°C
		SN65'	–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 3			100	mV
V _{IT–}	Negative-going differential input voltage threshold		–100			mV
V _{OH}	High-level output voltage	I _{OH} = –8 mA	2.4	3		V
V _{OL}	Low-level output voltage	I _{OL} = 8 mA		0.2	0.4	V
I _{CC}	Supply current	'LVDx386		50	70	mA
		'LVDx388A		22	40	
		'LVDx390		8	18	
		'LVDx386			3	
		'LVDx388A			3	
		'LVDx390			1.5	
I _I	Input current (A or B inputs)	'LVDS	V _I = 0 V	–13	–20	μA
			V _I = 2.4 V	–1.2	–3	
		'LVDT	V _I = 0 V, other input open		–40	
			V _I = 2.4 V, other input open	–2.4		
I _{ID}	Differential input current I _{IA} – I _{IB}	'LVDS	V _{IA} = 0 V, V _{IB} = 0.1 V, V _{IA} = 2.4 V, V _{IB} = 2.3 V		±2	μA
I _{ID}	Differential input current (I _{IA} – I _{IB})	'LVDT	V _{IA} = 0.2 V, V _{IB} = 0 V, V _{IA} = 2.4 V, V _{IB} = 2.2 V	1.5	2.2	mA
I _{I(OFF)}	Power-off input current (A or B inputs)	'LVDS	V _{CC} = 0 V, V _I = 2.4 V	12	±20	μA
I _{I(OFF)}	Power-off input current (A or B inputs)	'LVDT	V _{CC} = 0 V, V _I = 2.4 V		±40	μA
I _{IH}	High-level input current (enables)		V _{IH} = 2 V		10	μA
I _{IL}	Low-level input current (enables)		V _{IL} = 0.8 V		10	μA
I _{OZ}	High-impedance output current		V _O = 0 V		±1	μA
			V _O = 3.6 V		10	
C _{IN}	Input capacitance, A or B input to GND		V _{ID} = 0.4 sin 2.5E09 t V	5		pF
Z _(t)	Termination impedance		V _{ID} = 0.4 sin 2.5E09 t V	88	132	Ω

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	See Figure 2	1	2.6	4	ns
t_{PHL} Propagation delay time, high-to-low-level output		1	2.5	4	ns
t_r Output signal rise time		500	800	1200	ps
t_f Output signal fall time		500	800	1200	ps
$t_{sk(p)}$ Pulse skew ($ t_{PHL} - t_{PLH} $)			150	600	ps
$t_{sk(o)}$ Output skew ⁽²⁾			100	400	ps
$t_{sk(pp)}$ Part-to-part skew ⁽³⁾				1	ns
t_{PZH} Propagation delay time, high-impedance-to-high-level output	See Figure 3		7	15	ns
t_{PZL} Propagation delay time, high-impedance-to-low-level output			7	15	ns
t_{PHZ} Propagation delay time, high-level-to-high-impedance output			7	15	ns
t_{PLZ} Propagation delay time, low-level-to-high-impedance output			7	15	ns

- (1) All typical values are at 25°C and with a 3.3-V supply.
- (2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
- (3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of any two devices characterized in this data sheet when both devices operate with the same supply voltage, at the same temperature, and have the same test circuits.

PARAMETER MEASUREMENT INFORMATION

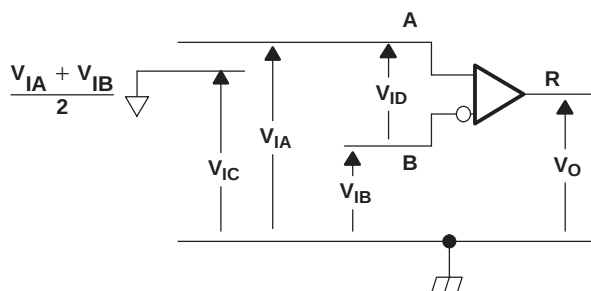
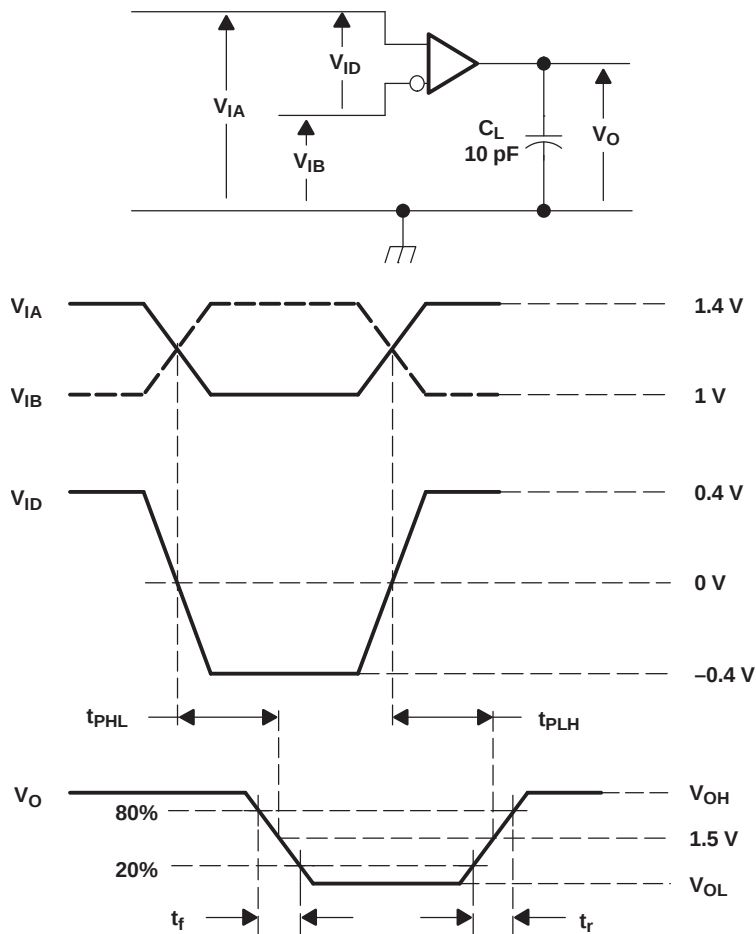


Figure 1. Voltage Definitions

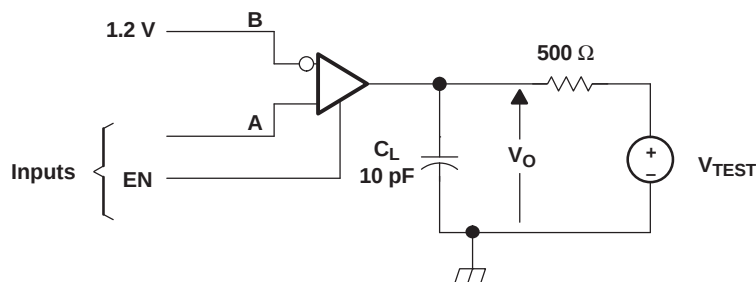
Table 3. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON- MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 50 Mpps, pulse width = $10 \pm 0.2 \text{ ns}$. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 2. Timing Test Circuit and Wave Forms



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

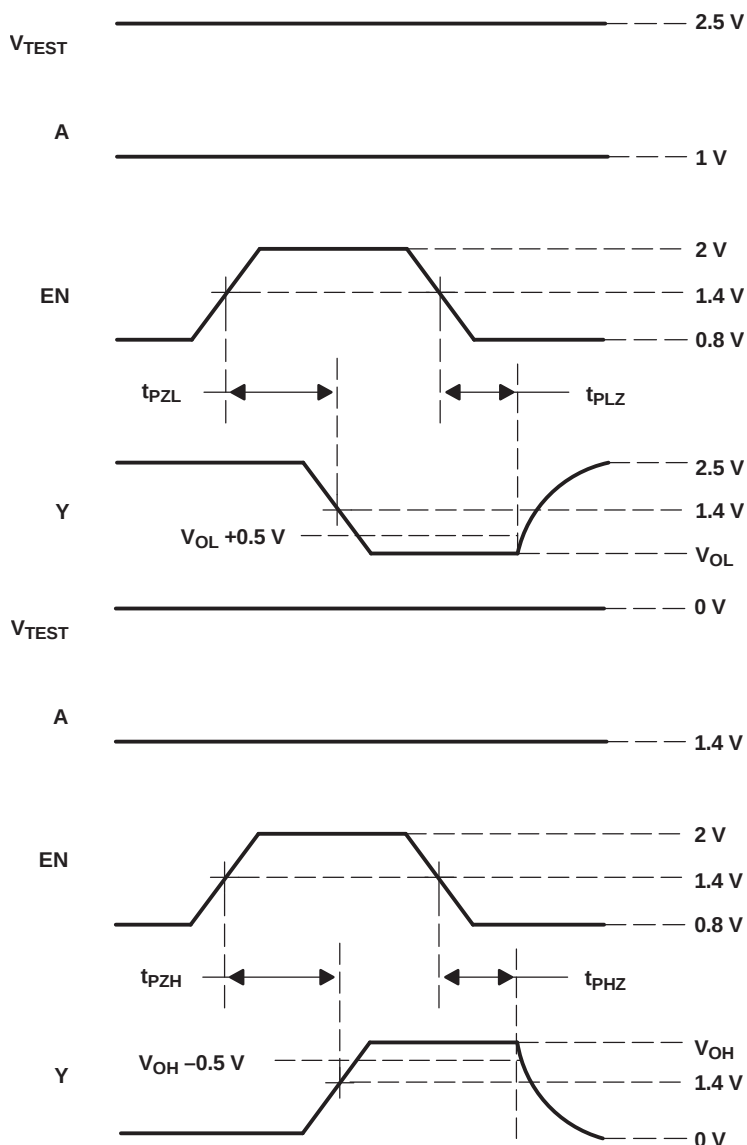


Figure 3. Enable/Disable Time Test Circuit and Wave Forms

TYPICAL CHARACTERISTICS

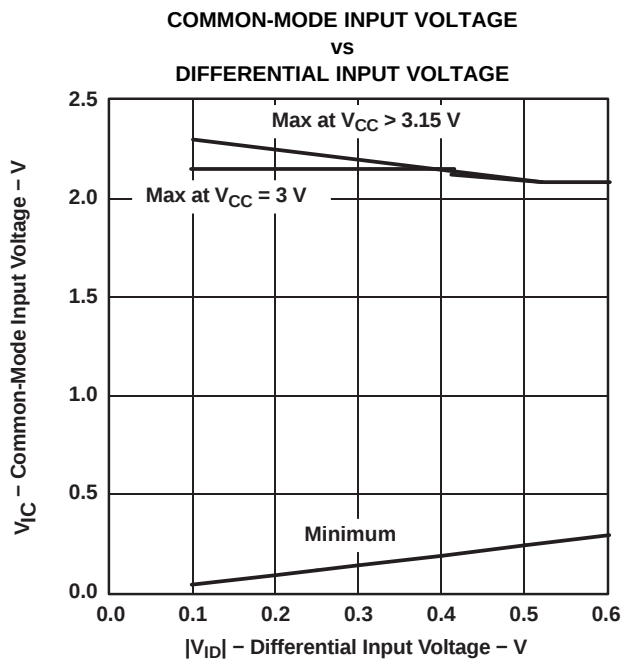


Figure 4.

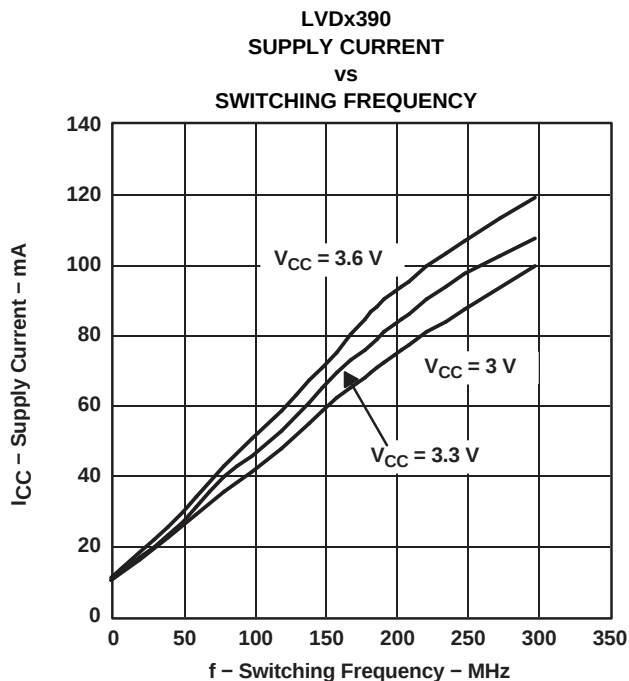


Figure 5.

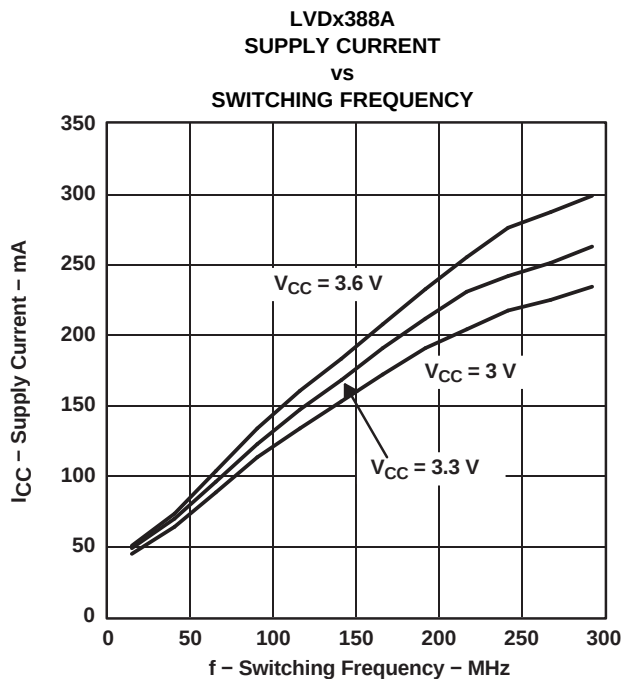


Figure 6.

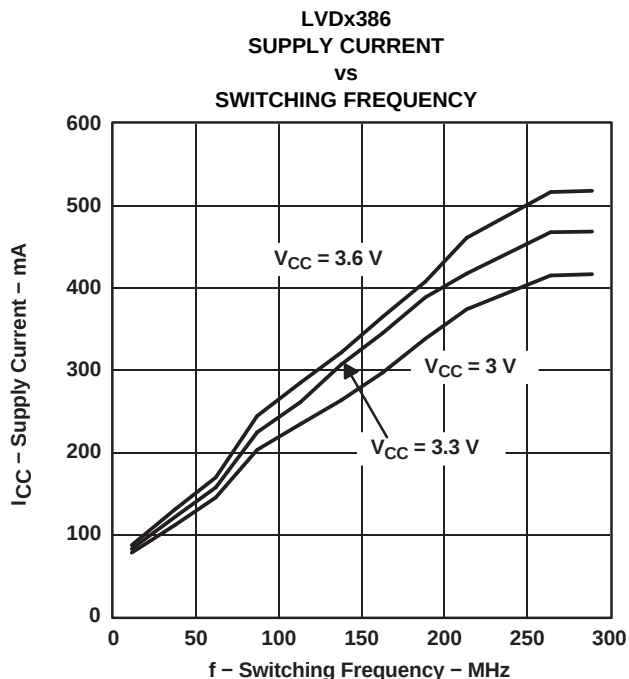


Figure 7.

TYPICAL CHARACTERISTICS (continued)

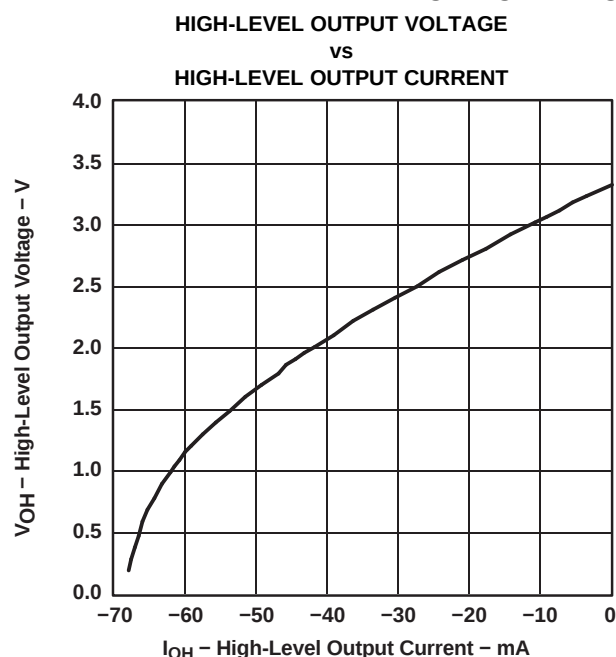


Figure 8.

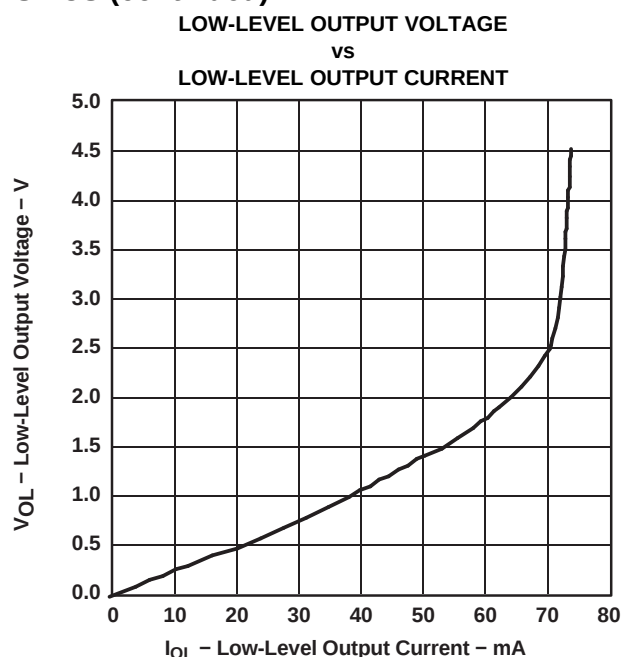


Figure 9.

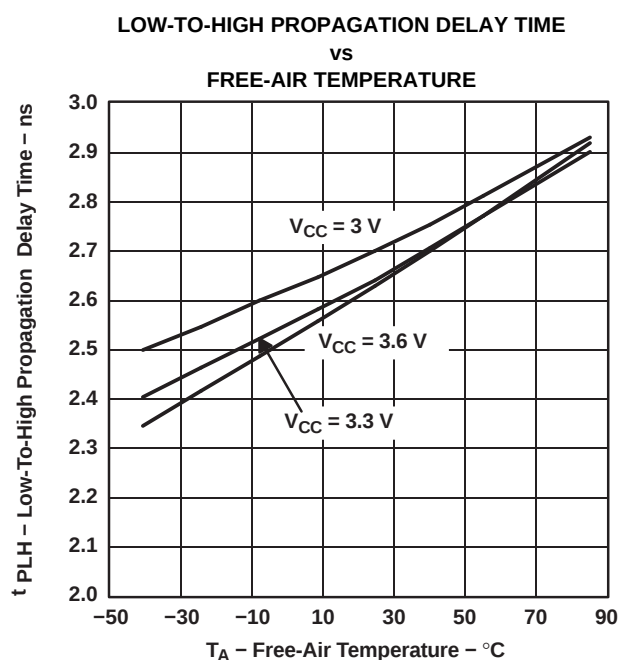


Figure 10.

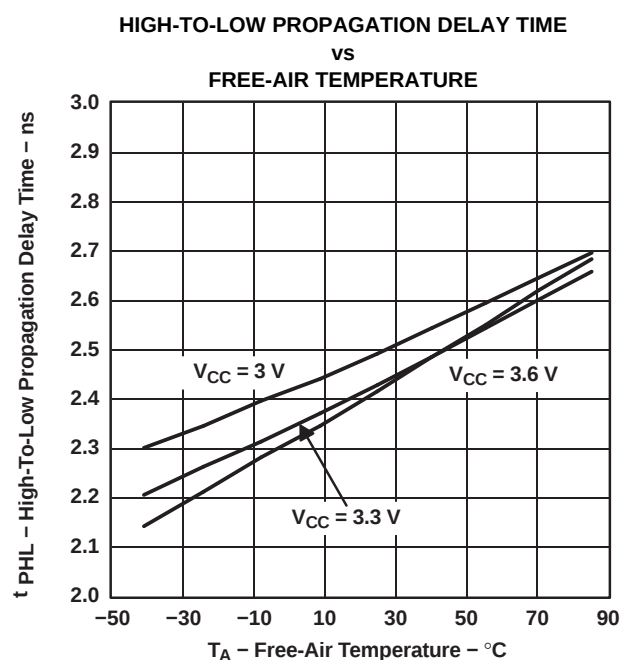


Figure 11.

APPLICATION INFORMATION

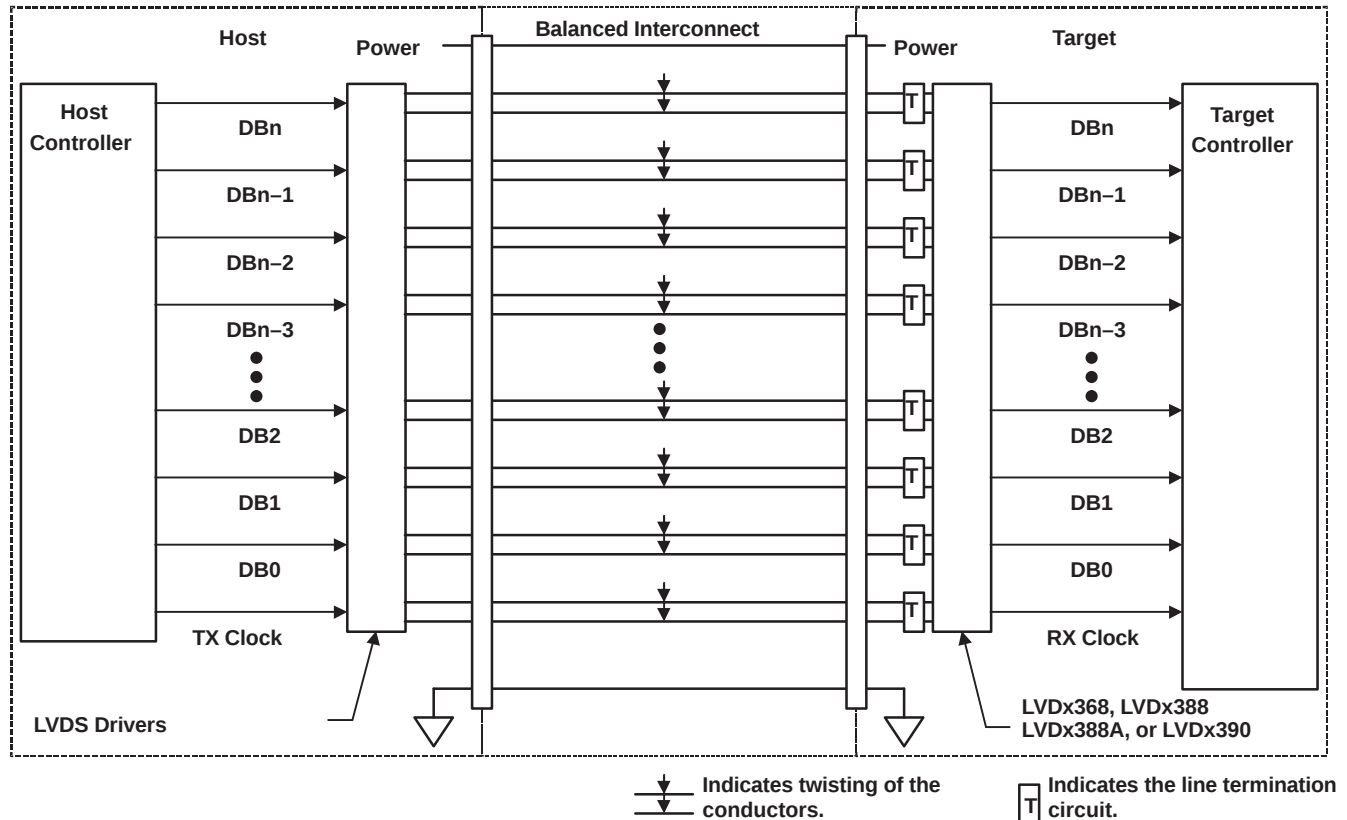


Figure 12. Typical Application Schematic

ANALOG AND DIGITAL GROUNDS/POWER SUPPLIES

Although it is not necessary to separate out the analog/digital supplies and grounds on the SN65LVDS/T388A and SN75LVDS/T388A, the pinout provides the user that option. To help minimize or perhaps eliminate switching noise being coupled between the two supplies, the user could lay out separate supply and ground planes for the designated pinout.

Most applications probably have all grounds connected together and all power supplies connected together. This configuration was used while characterizing and setting the data-sheet parameters.

FAIL SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and 100 mV , and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through $300\text{-k}\Omega$ resistors, as shown in Figure 13. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level, regardless of the differential input voltage.

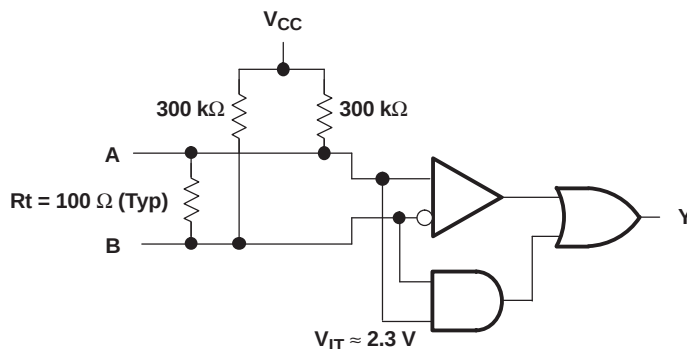


Figure 13. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, R_t , does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

EQUIPMENT

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS6604 Digital Storage Scope
- Agilent ParBERT E4832A

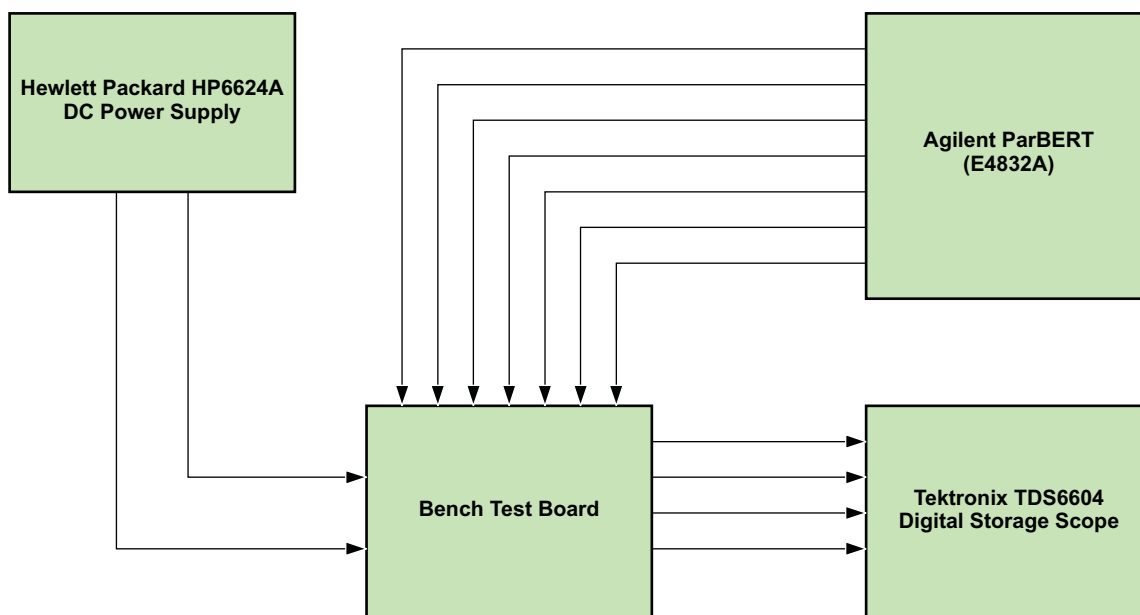


Figure 14. Equipment Setup

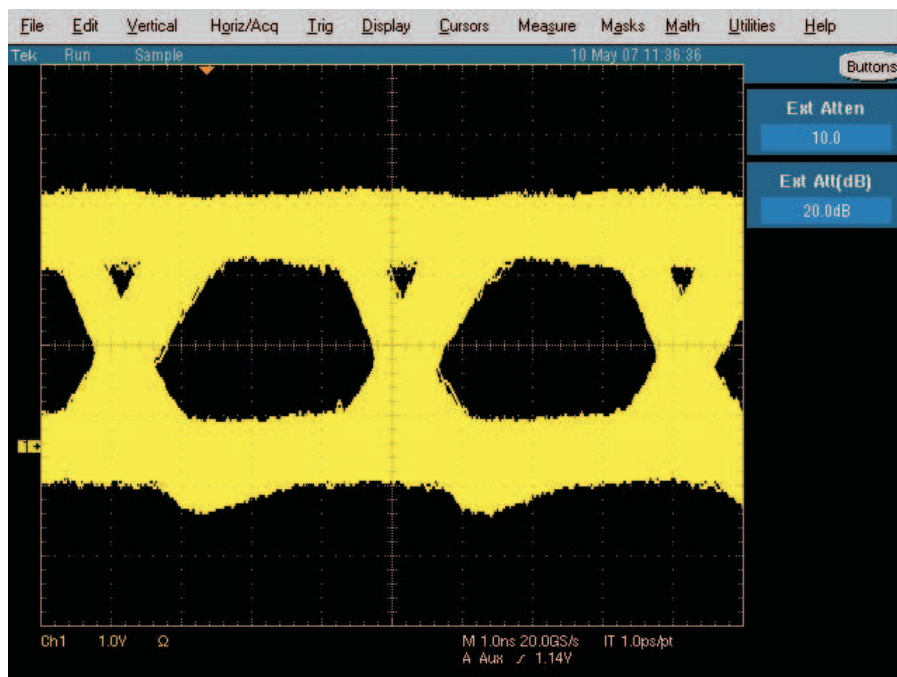


Figure 15. Typical Eye Pattern SN65LVDS386 all 16 Rx Switching at 250Mbps:
($T_A = 25^\circ\text{C}$; $V_{CC} = 3.6\text{V}$; PRBS = $2^{23}-1$) (Ch1 = xyY)
(where x represents the Rx group: A, B, C, or D, y represents the Rx: 1, 2, 3, or 4)

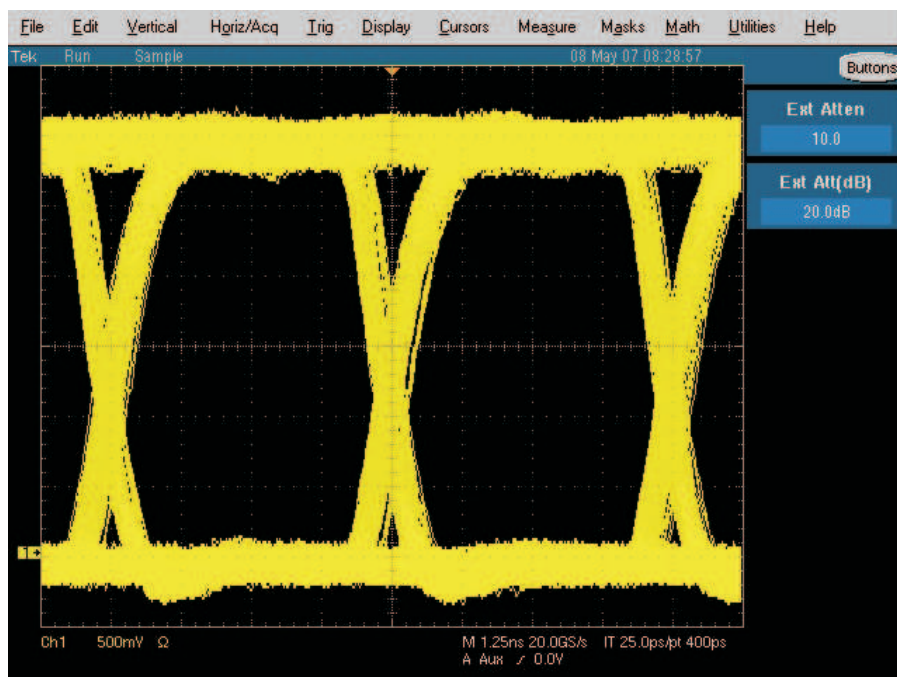


Figure 16. Typical Eye Pattern SN65LVDS388A all 8 Rx Switching at 200Mbps:
($T_A = 25^\circ\text{C}$; $V_{CC} = 3.6\text{V}$; PRBS = $2^{23}-1$) (Ch1 = xyY)
(where x represents the Rx group: A, B, C, or D, y represents the Rx: 1 or 2)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS386DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS386	Samples
SN65LVDS386DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS386	Samples
SN65LVDS386DGGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS386	Samples
SN65LVDS386DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS386	Samples
SN65LVDS388ADBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS388A	Samples
SN65LVDS388ADBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS388A	Samples
SN65LVDS388ADBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS388A	Samples
SN65LVDS388ADBTRG4	ACTIVE	TSSOP	DBT	38		TBD	Call TI	Call TI	-40 to 85		Samples
SN65LVDS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDS390PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS390	Samples
SN65LVDT386DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT386	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDT386DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT386	Samples
SN65LVDT386DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT386	Samples
SN65LVDT386DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT386	Samples
SN65LVDT388ADBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT388A	Samples
SN65LVDT388ADBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT388A	Samples
SN65LVDT388ADBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT388A	Samples
SN65LVDT388ADBTRG4	ACTIVE	TSSOP	DBT	38		TBD	Call TI	Call TI	-40 to 85		Samples
SN65LVDT390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT390	Samples
SN65LVDT390DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT390	Samples
SN65LVDT390PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT390	Samples
SN65LVDT390PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT390	Samples
SN65LVDT390PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT390	Samples
SN65LVDT390PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT390	Samples
SN75LVDS386DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS386	Samples
SN75LVDS386DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS386	Samples
SN75LVDS386DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS386	Samples
SN75LVDS388ADBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDS388A	Samples
SN75LVDS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS390	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVDS390DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS390	Samples
SN75LVDS390DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDS390	Samples
SN75LVDS390PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS390	Samples
SN75LVDS390PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS390	Samples
SN75LVDS390PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS390	Samples
SN75LVDS390PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DS390	Samples
SN75LVDT386DGG	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT386	Samples
SN75LVDT386DGGG4	ACTIVE	TSSOP	DGG	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT386	Samples
SN75LVDT386DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT386	Samples
SN75LVDT388ADBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT388A	Samples
SN75LVDT388ADBTG4	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT388A	Samples
SN75LVDT388ADBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT388A	Samples
SN75LVDT388ADBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75LVDT388A	Samples
SN75LVDT390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDT390	Samples
SN75LVDT390DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75LVDT390	Samples
SN75LVDT390PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DG390	Samples
SN75LVDT390PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DG390	Samples
SN75LVDT390PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DG390	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVDT390PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	DG390	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS386DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDS388ADBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN65LVDS390DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS390PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDT386DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN65LVDT388ADBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN65LVDT390PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75LVDS390DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75LVDS390PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN75LVDT386DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1
SN75LVDT388ADBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN75LVDT390DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75LVDT390PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS386DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN65LVDS388ADBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
SN65LVDS390DR	SOIC	D	16	2500	367.0	367.0	38.0
SN65LVDS390PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65LVDT386DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN65LVDT388ADBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
SN65LVDT390PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN75LVDS390DR	SOIC	D	16	2500	367.0	367.0	38.0
SN75LVDS390PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN75LVDT386DGGR	TSSOP	DGG	64	2000	367.0	367.0	45.0
SN75LVDT388ADBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0
SN75LVDT390DR	SOIC	D	16	2500	367.0	367.0	38.0
SN75LVDT390PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

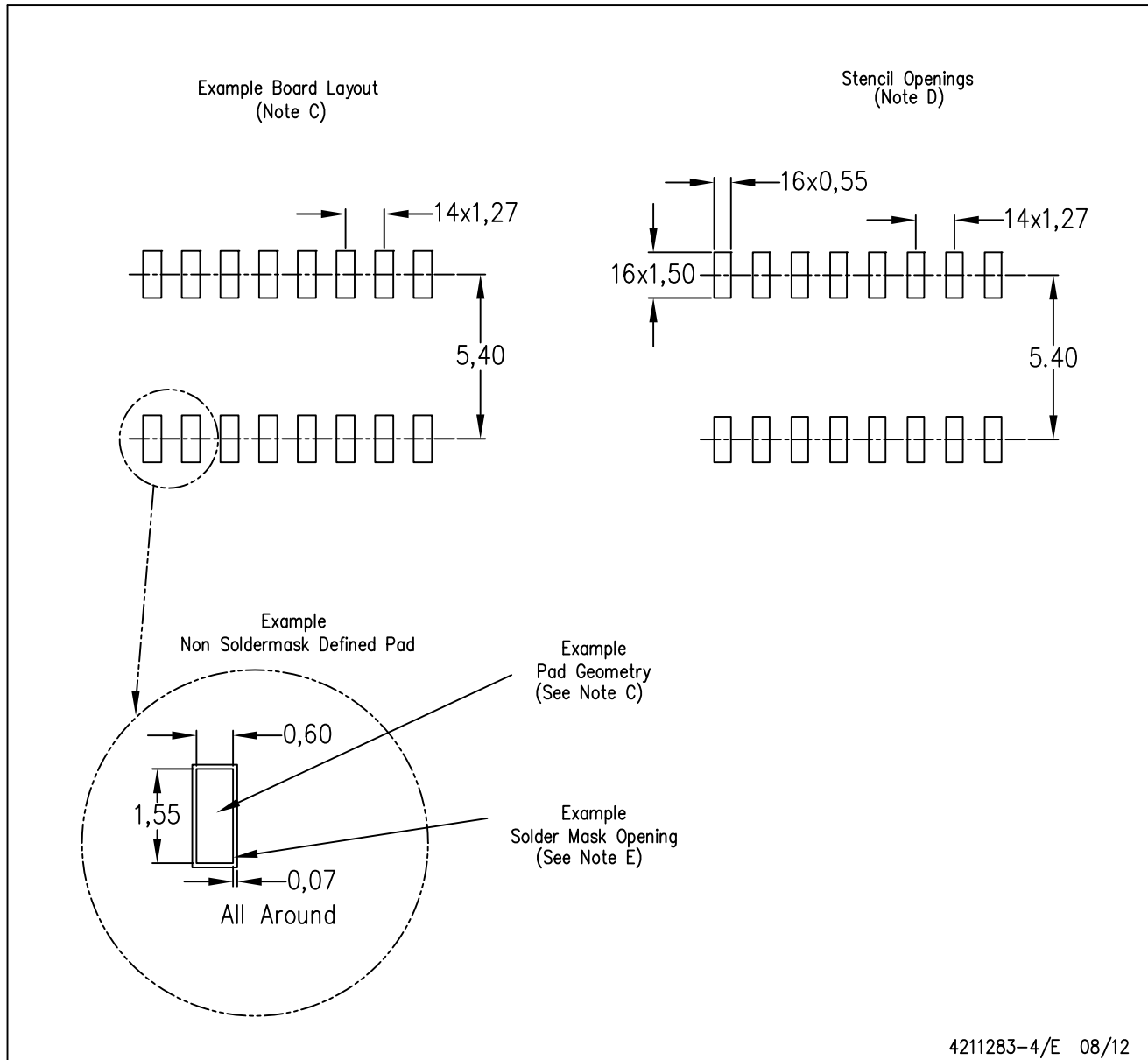


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

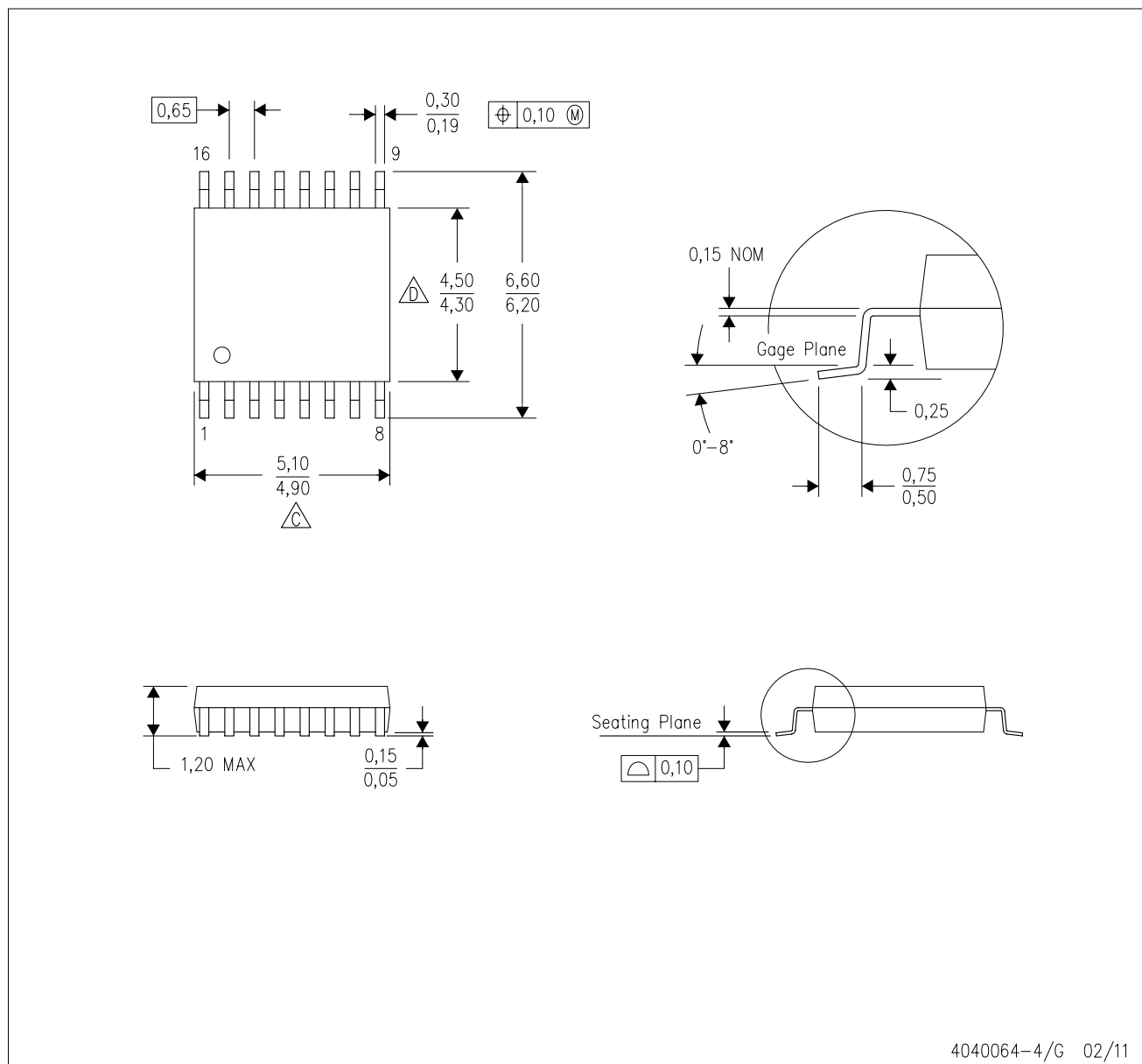
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

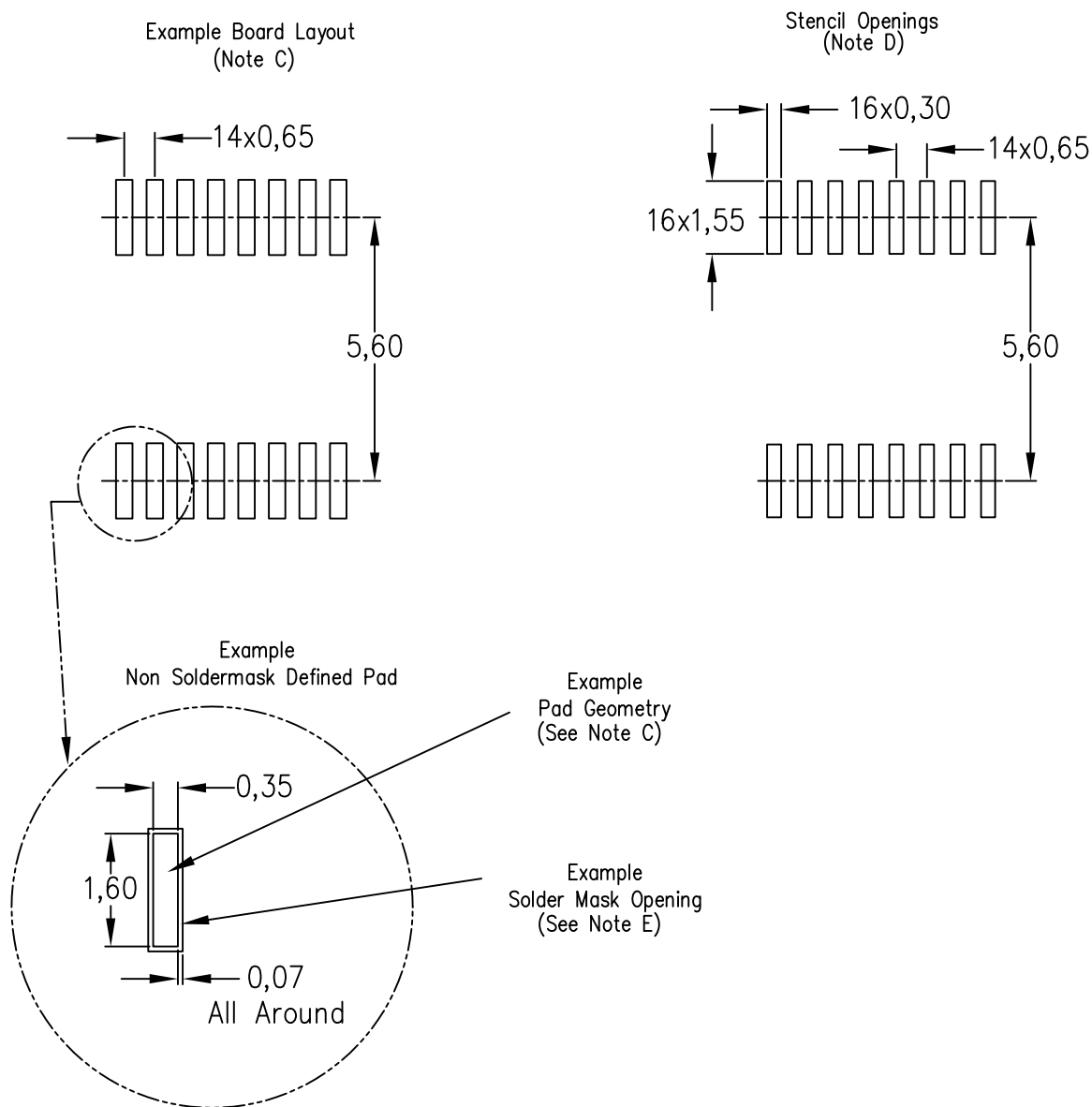


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

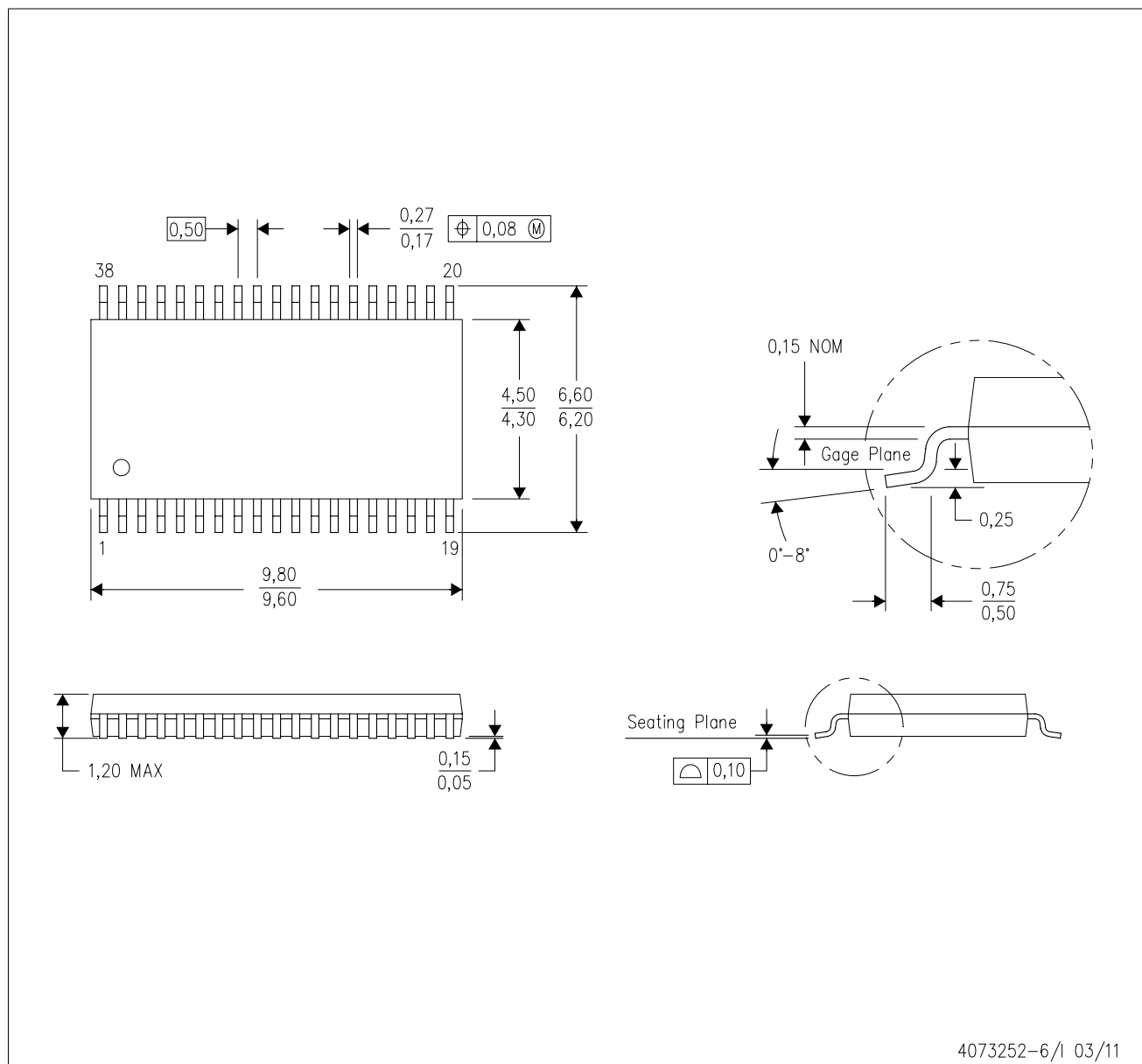


4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBT (R-PDSO-G38)

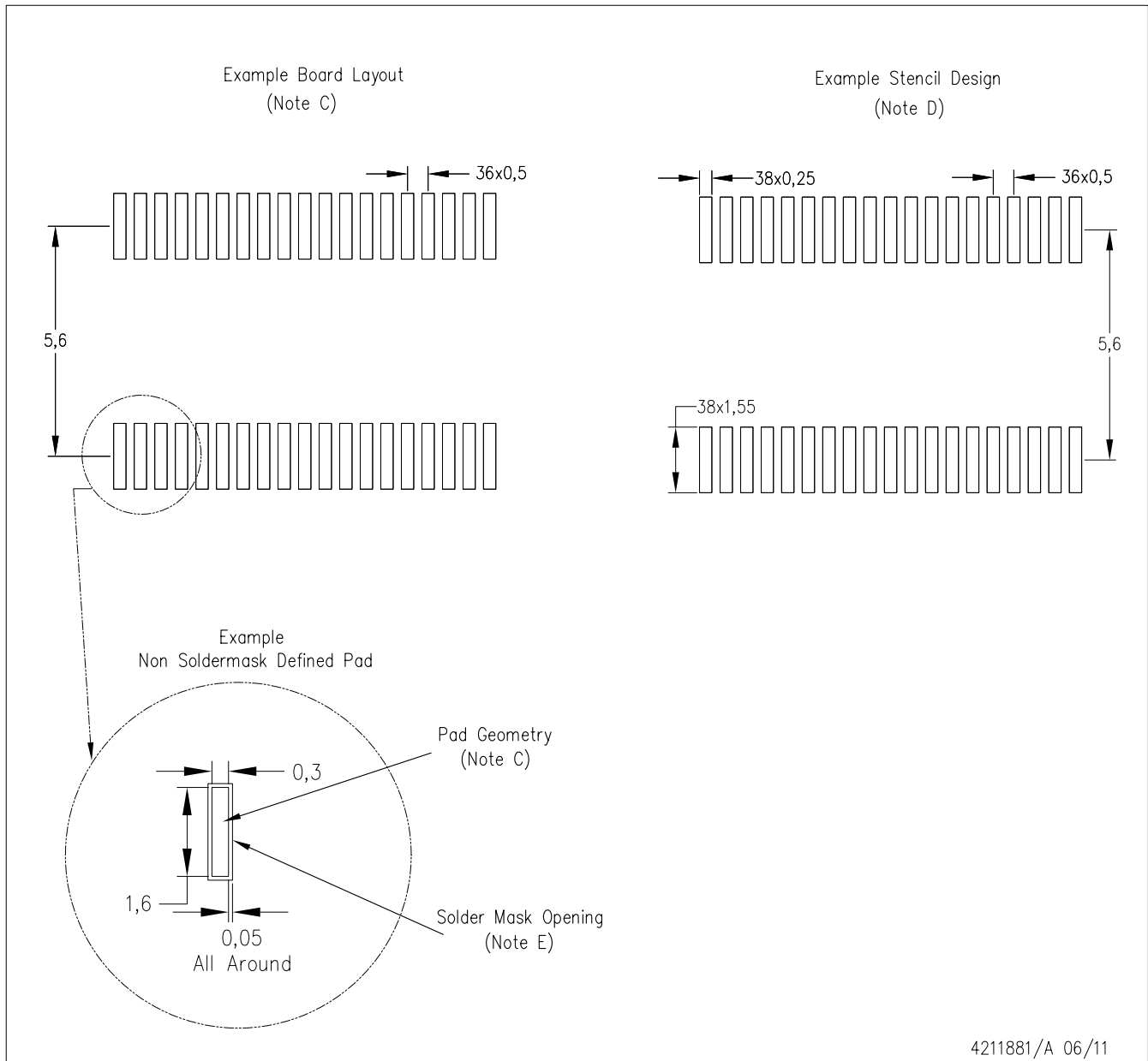
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-153.

DBT (R-PDSO-G38)

PLASTIC SMALL OUTLINE

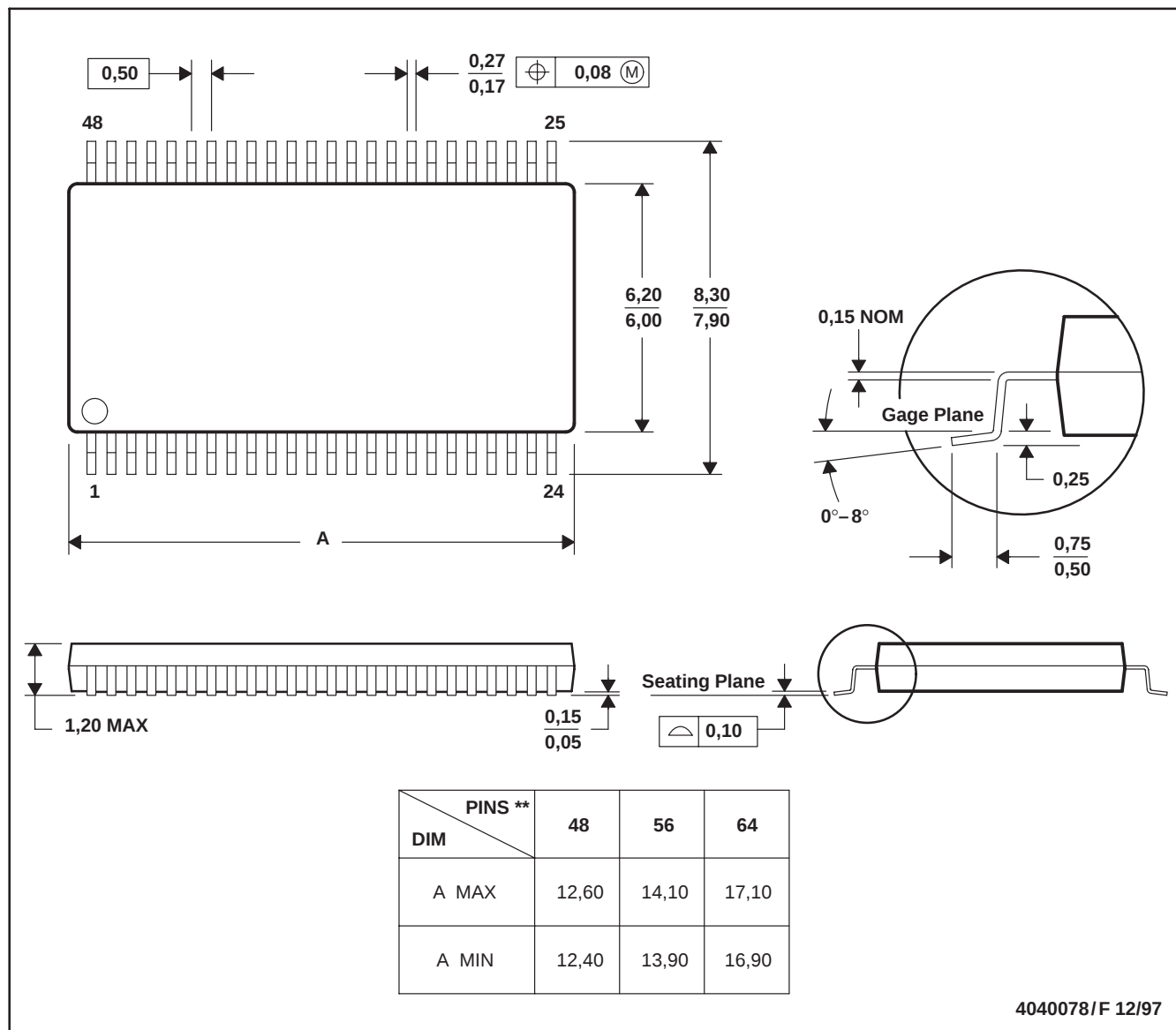


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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