

## MAX5389

## Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

### General Description

The MAX5389 dual, 256-tap, volatile, low-voltage linear taper digital potentiometer offers three end-to-end resistance values of 10k $\Omega$ , 50k $\Omega$ , and 100k $\Omega$ . Operating from a single +2.6V to +5.5V power supply, the device provides a low 35ppm/ $^{\circ}$ C end-to-end temperature coefficient. The MAX5389 features an up/down interface.

The small package size, low supply operating voltage, low supply current, and automotive temperature range of the MAX5389 make the device uniquely suited for the portable consumer market and battery backup industrial applications.

The MAX5389 is specified over the automotive -40 $^{\circ}$ C to +125 $^{\circ}$ C temperature range and is available in a 14-pin TSSOP package.

### Applications

- Audio Mixing
- Mechanical Potentiometer Replacement
- Low-Drift Programmable Filters and Amplifiers
- Adjustable Voltage References/Linear Regulators
- Programmable Delays and Time Constants
- Low-Voltage Battery Applications

### Features

- Dual, 256-Tap Linear Taper Positions
- Single +2.6V to +5.5V Supply Operation
- Low (< 1 $\mu$ A) Quiescent Supply Current
- 10k $\Omega$ , 50k $\Omega$ , 100k $\Omega$  End-to-End Resistance Values
- Up/Down Interface
- Power-On Sets Wiper to Midscale
- -40 $^{\circ}$ C to +125 $^{\circ}$ C Operating Temperature Range

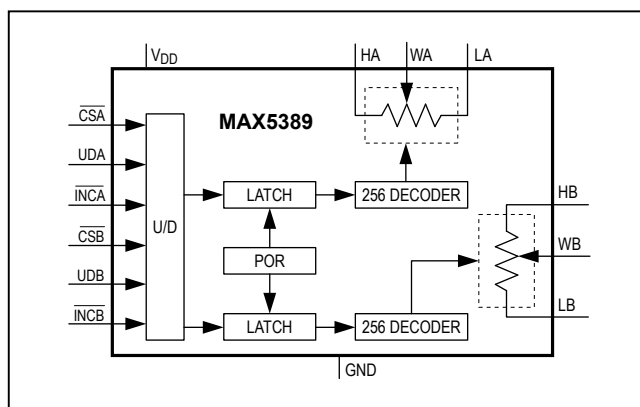
### Ordering Information

PART	PIN-PACKAGE	END-TO-END RESISTANCE (k $\Omega$ )
MAX5389LAUD+	14 TSSOP	10
MAX5389MAUD+	14 TSSOP	50
MAX5389NAUD+	14 TSSOP	100

**Note:** All devices are specified over the -40 $^{\circ}$ C to +125 $^{\circ}$ C operating temperature range

+Denotes a lead(Pb)-free/RoHS-compliant package.

### Functional Diagram



## Absolute Maximum Ratings

$V_{DD}$ to GND .....	-0.3V to +6V
$H_{-}$ , $W_{-}$ , $L_{-}$ to GND .....	-0.3V to the lower of ( $V_{DD} + 0.3V$ ) and +6V
All Other Pins to GND .....	-0.3V to +6V
Continuous Current into $H_{-}$ , $W_{-}$ , and $L_{-}$	
MAX5389L .....	$\pm 5mA$
MAX5389M .....	$\pm 2mA$
MAX5389N .....	$\pm 1mA$

Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
14-Pin TSSOP (derate 10mW/ $^{\circ}C$ above $+70^{\circ}C$ ) .....	796.8mW
Operating Temperature Range .....	$-40^{\circ}C$ to $+125^{\circ}C$
Junction Temperature .....	$+150^{\circ}C$
Storage Temperature Range .....	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (soldering, 10s) .....	$+300^{\circ}C$
Soldering Temperature (reflow) .....	$+260^{\circ}C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Electrical Characteristics

( $V_{DD} = +2.6V$  to  $+5.5V$ ,  $V_{H_{-}} = V_{DD}$ ,  $V_{L_{-}} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{DD} = +5V$ ,  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution	N			256			Taps
DC PERFORMANCE (Voltage-Divider Mode)							
Integral Nonlinearity	INL	(Note 2)		-0.5		+0.5	LSB
Differential Nonlinearity	DNL	(Note 2)		-0.5		+0.5	LSB
Dual Code Matching		Register A = register B		-0.5		+0.5	LSB
Ratiometric Resistor Tempco		(ΔV <sub>W</sub> /V <sub>W</sub> )/ ΔT, no load		+5			LSB
Full-Scale Error		Code = FFH	MAX5389L	-3	-2.5		LSB
			MAX5389M	-1	-0.5		
			MAX5389N	-0.5	-0.25		
Zero-Scale Error		Code = 00H	MAX5389L		+2.5	+3	LSB
			MAX5389M		+0.5	+1.0	
			MAX5389N		+0.25	+0.5	
DC PERFORMANCE (Variable-Resistor Mode) (Note 3)							
Integral Nonlinearity	R-INL	V <sub>DD</sub> > +2.6V	MAX5389L		±1.0	±2.5	LSB
			MAX5389M		±0.5	±1.0	
			MAX5389N		±0.25	±0.8	
		V <sub>DD</sub> > +4.75V	MAX5389L		±0.4	±1.5	
			MAX5389M		±0.3	±0.75	
			MAX5389N		±0.25	±0.5	
Differential Nonlinearity	R-DNL	V <sub>DD</sub> ≥ 2.6V		-0.5		+0.5	LSB
DC PERFORMANCE (Resistor Characteristics)							
Wiper Resistance (Note 4)	R <sub>WL</sub>	V <sub>DD</sub> > 2.6V		250		600	Ω
		V <sub>DD</sub> > 4.75V		150		200	
Terminal Capacitance	C <sub>H_</sub> , C <sub>L_</sub>	Measured to GND		10			pF
Wiper Capacitance	C <sub>W_</sub>	Measured to GND		50			pF
End-to-End Resistor Tempco	TC <sub>R</sub>	No load		35			ppm/°C
End-to-End Resistor Tolerance	ΔR <sub>HL</sub>	Wiper not connected		-25		+25	%

## Electrical Characteristics (continued)

( $V_{DD} = +2.6V$  to  $+5.5V$ ,  $V_{H\_} = V_{DD}$ ,  $V_{L\_} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{DD} = +5V$ ,  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC PERFORMANCE							
Crosstalk		(Note 5)		-90		dB	
-3dB Bandwidth	BW	Code = 80H, 10pF load, V <sub>DD</sub> = +2.6V	MAX5389L	600		kHz	
			MAX5389M	150			
			MAX5389N	75			
Total Harmonic Distortion Plus Noise	THD+N	Measured at W, V <sub>H_</sub> = 1V <sub>RMS</sub> at 1kHz		0.015		%	
Wiper Settling Time (Note 6)	t <sub>S</sub>	MAX5389L		300		ns	
		MAX5389M		1000			
		MAX5389N		2000			
POWER SUPPLIES							
Supply Voltage Range	V <sub>DD</sub>			2.6	5.5		V
Standby Current		Digital inputs = V <sub>DD</sub> or GND		1		μA	
DIGITAL INPUTS							
Minimum Input High Voltage	V <sub>IH</sub>			70		% x V <sub>DD</sub>	
Maximum Input Low Voltage	V <sub>IL</sub>			30		% x V <sub>DD</sub>	
Input Leakage Current				-1		+1	
Input Capacitance				5		pF	
TIMING CHARACTERISTICS (Note 7)							
Maximum INC_ Frequency	f <sub>MAX</sub>			10		MHz	
CS to INC_ Setup Time	t <sub>CI</sub>			25		ns	
CS to INC_ Hold Time	t <sub>IC</sub>			0		ns	
INC_ Low Period	t <sub>IL</sub>			25		ns	
INC_ High Period	t <sub>IH</sub>			25		ns	
UD_ to INC_ Setup Time	t <sub>DI</sub>			50		ns	
UD_ to INC_ Hold Time	t <sub>ID</sub>			0		ns	

**Note 1:** All devices are 100% production tested at  $T_A = +25^{\circ}C$ . Specifications over temperature limits are guaranteed by design and characterization.

**Note 2:** DNL and INL are measured with the potentiometer configured as a voltage-divider (Figure 1) with  $H\_ = V_{DD}$  and  $L\_ = GND$ . The wiper terminal is unloaded and measured with a high-input-impedance voltmeter.

**Note 3:** R-DNL and R-INL are measured with the potentiometer configured as a variable resistor (Figure 1). DNL and INL are measured with potentiometer configured as a variable resistor.  $H\_$  is unconnected and  $L\_ = GND$ . For  $V_{DD} = +5V$ , the wiper terminal is driven with a source current of 400 $\mu A$  for the 10k $\Omega$  configuration, 80 $\mu A$  for the 50k $\Omega$  configuration, and 40 $\mu A$  for the 100k $\Omega$  configuration. For  $V_{DD} = +2.6V$ , the wiper terminal is driven with a source current of 200 $\mu A$  for the 10k $\Omega$  configuration, 40 $\mu A$  for the 50k $\Omega$  configuration, and 20 $\mu A$  for the 100k $\Omega$  configuration.

**Note 4:** The wiper resistance is the worst value measured by injecting the currents given in Note 3 into  $W\_$  with  $L\_ = GND$ .  $R_W = V_W - V_H / I_W$ .

**Note 5:** Drive  $HA$  with a 1kHz, GND to  $V_{DD}$  amplitude, tone.  $LA = LB = GND$ . No load.  $WB$  is at midscale with a 10pF load. Measure  $WB$ .

**Note 6:** The wiper-settling time is the worst case 0 to 50% rise time, measured between tap 0 and tap 127.  $H\_ = V_{DD}$ ,  $L\_ = GND$ , and the wiper terminal is loaded with 10pF capacitance to ground.

**Note 7:** Digital timing is guaranteed by design and characterization, not production tested.

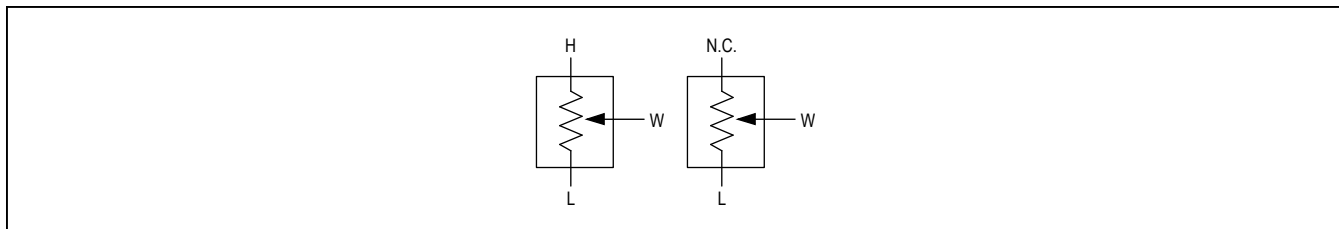
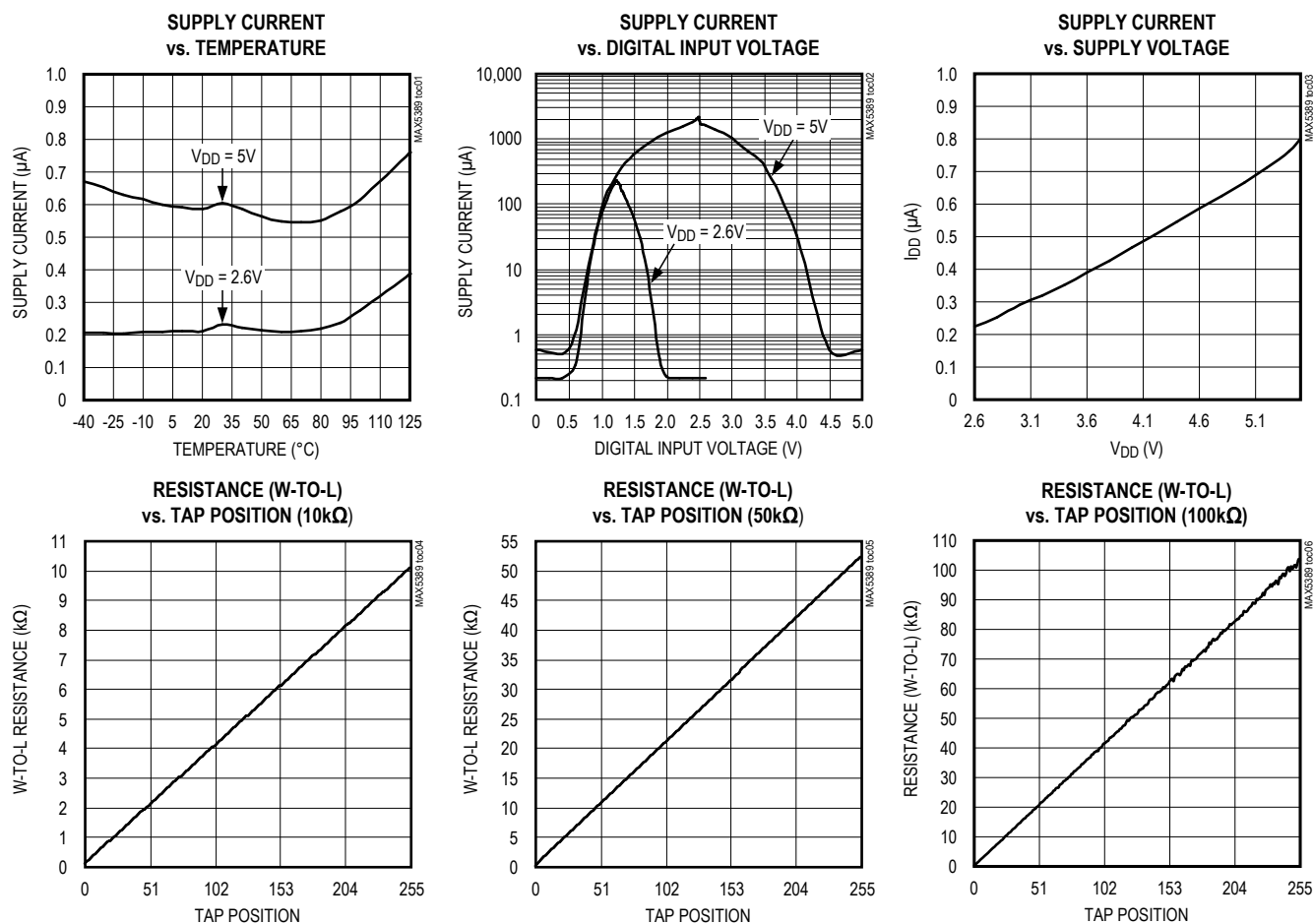


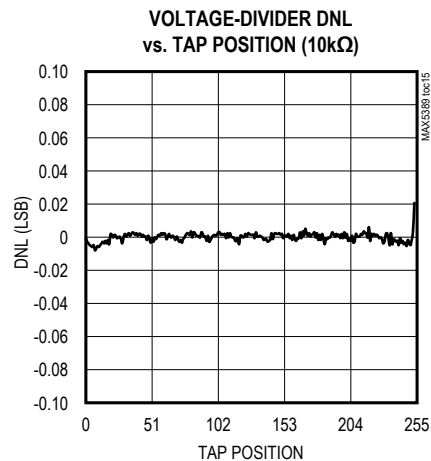
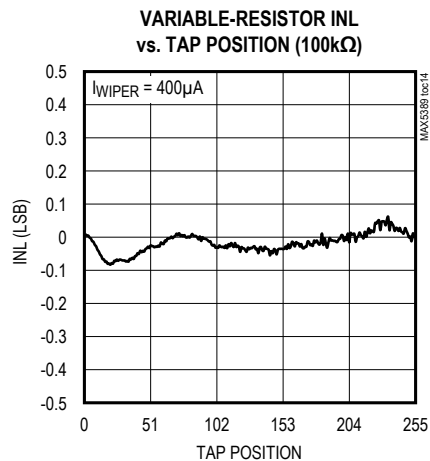
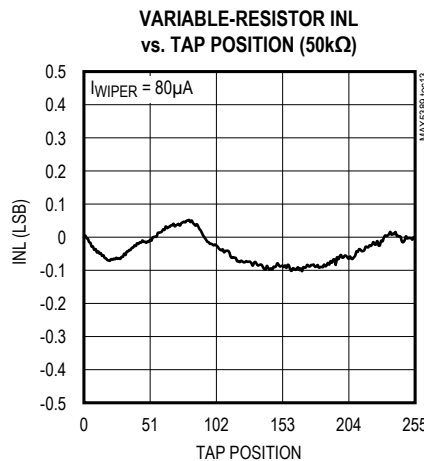
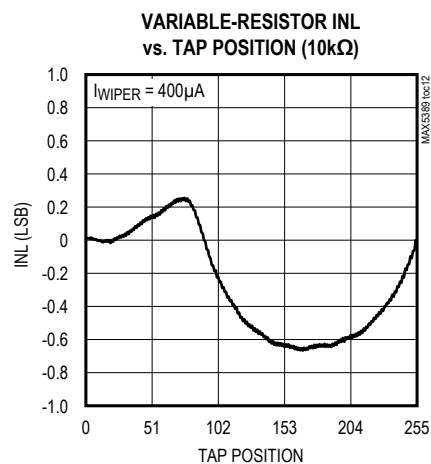
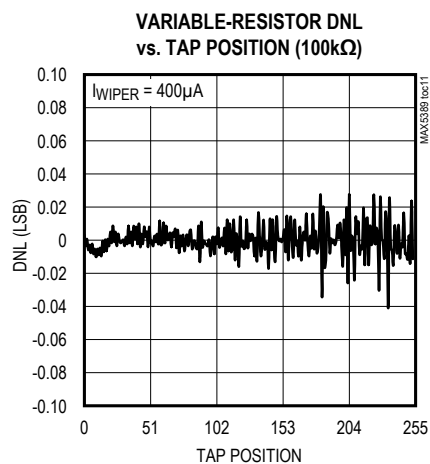
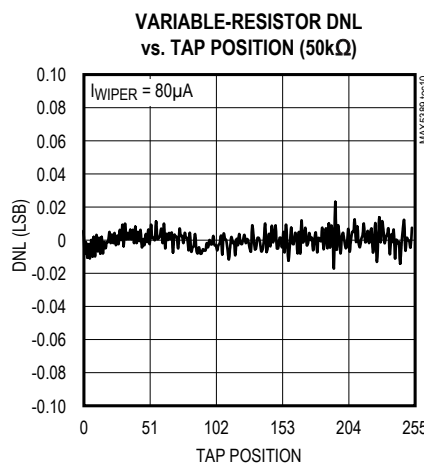
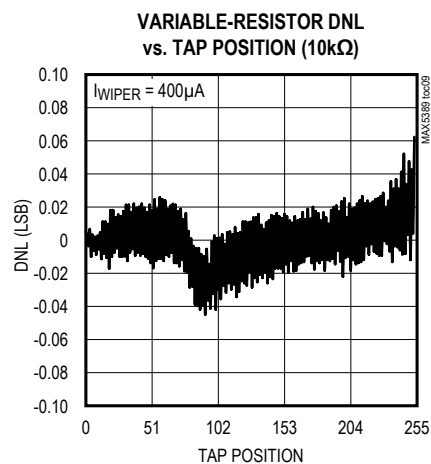
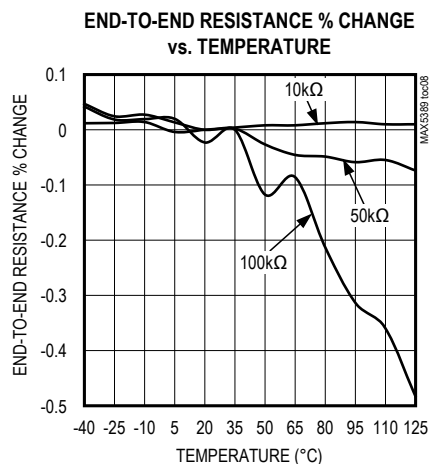
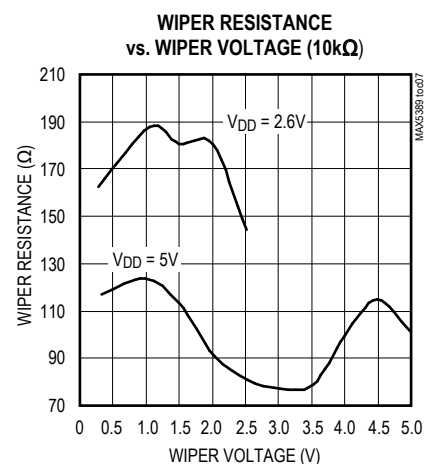
Figure 1. Voltage-Divider and Variable Resistor Configurations

## Typical Operating Characteristics

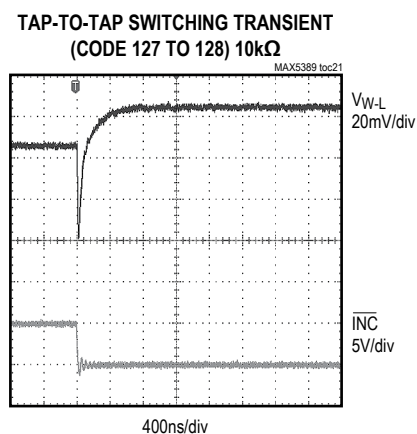
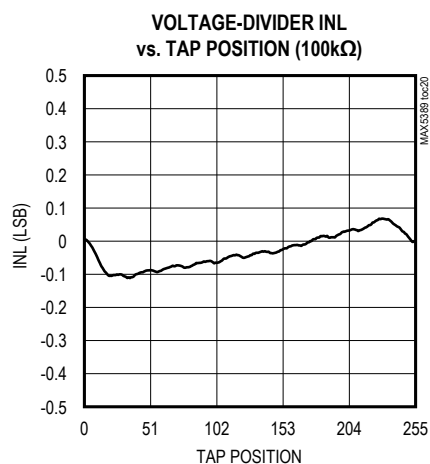
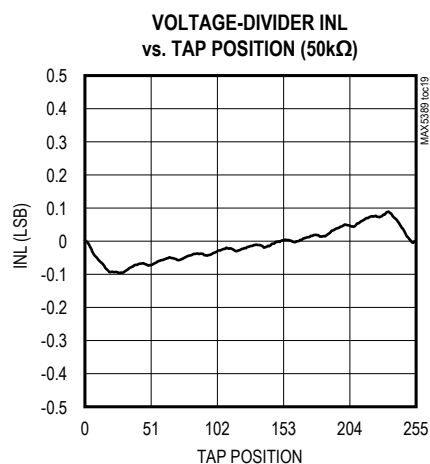
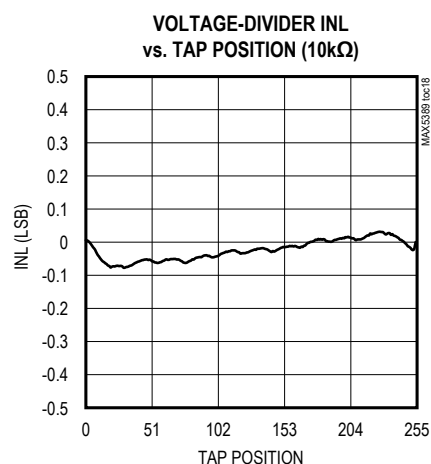
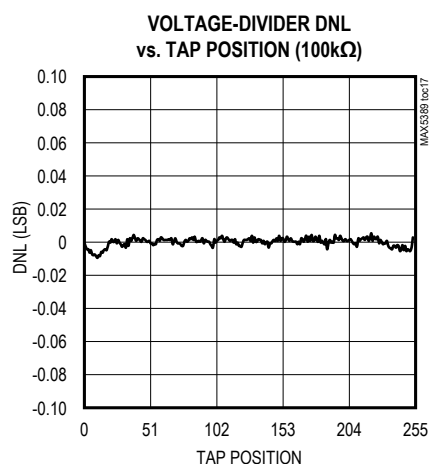
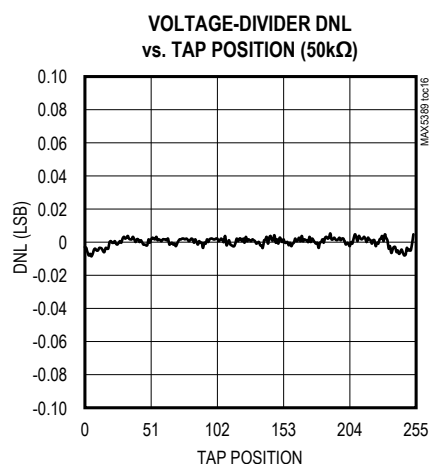
( $V_{DD} = +5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



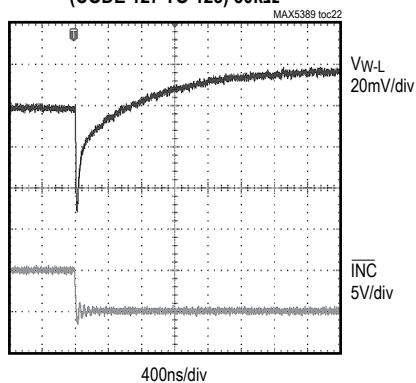
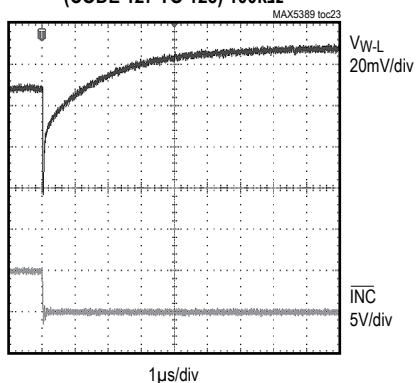
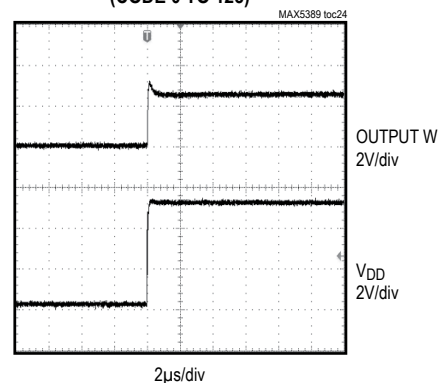
## Typical Operating Characteristics (continued)

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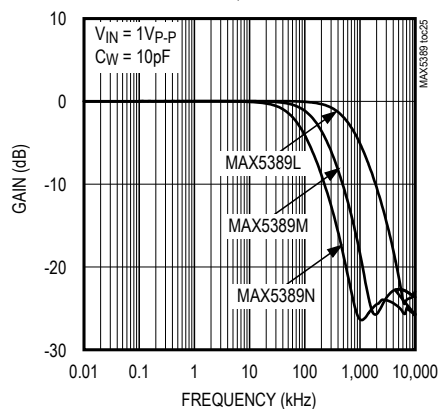
## Typical Operating Characteristics (continued)

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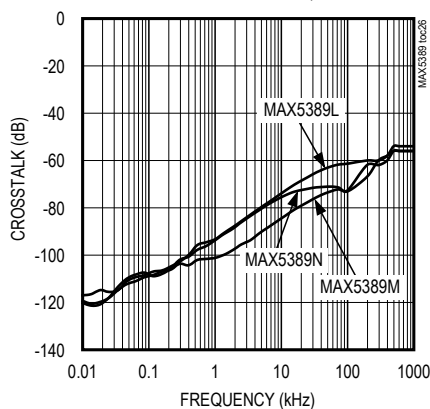
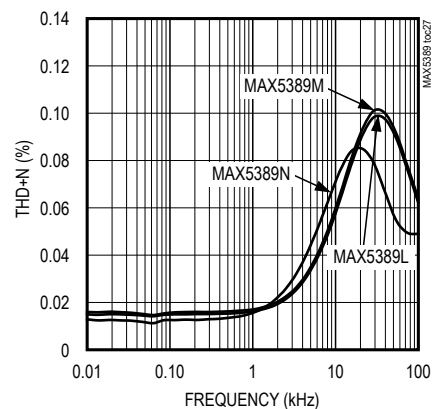
## Typical Operating Characteristics (continued)

(V<sub>DD</sub> = +5V, T<sub>A</sub> = +25°C, unless otherwise noted.)TAP-TO-TAP SWITCHING TRANSIENT  
(CODE 127 TO 128) 50k $\Omega$ TAP-TO-TAP SWITCHING TRANSIENT  
(CODE 127 TO 128) 100k $\Omega$ POWER-ON WIPER TRANSIENT  
(CODE 0 TO 128)

MIDSCALE FREQUENCY RESPONSE



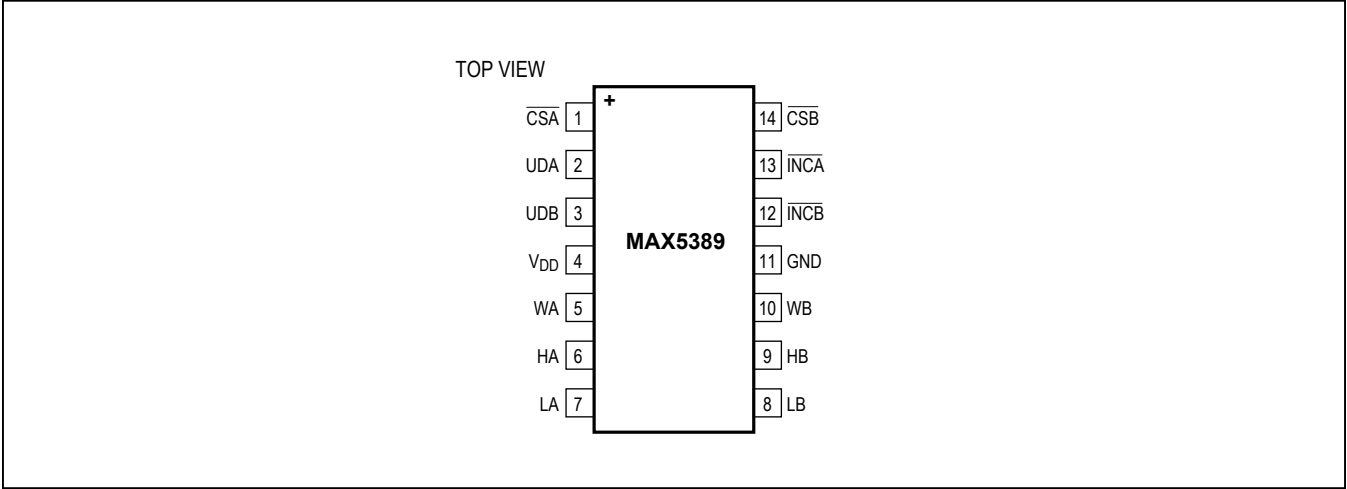
CROSSTALK vs. FREQUENCY

TOTAL HARMONIC DISTORTION PLUS NOISE  
vs. FREQUENCY

MAX5389

Dual, 256-Tap, Volatile, Low-Voltage  
Linear Taper Digital Potentiometer

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{CSA}}$	Active-Low Register A Chip-Select Input. Drive $\overline{\text{CSA}}$ low to change wiper position WA through $\overline{\text{INCA}}$ and UDA.
2	UDA	Register A Up/Down Control Input. With UDA low, a high-to-low transition at $\overline{\text{INCA}}$ decrements the WA position towards LA. With UDA high, a high-to-low transition at $\overline{\text{INCA}}$ increments WA position toward HA.
3	UDB	Register B Up/Down Control Input. With UDB low, a high-to-low transition at $\overline{\text{INCB}}$ decrements the WB position towards LB. With UDB high, a high-to-low transition at $\overline{\text{INCB}}$ increments WB position toward HB.
4	$V_{\text{DD}}$	Power-Supply Input. Bypass $V_{\text{DD}}$ to GND with a 0.1 $\mu\text{F}$ capacitor close to the device.
5	WA	Resistor A Wiper Terminal
6	HA	Resistor A High Terminal. The voltage at HA can be higher or lower than the voltage at LA. Current can flow into or out of HA.
7	LA	Resistor A Low Terminal. The voltage at LA can be higher or lower than the voltage at HA. Current can flow into or out of LA.
8	LB	Resistor B Low Terminal. The voltage at LB can be higher or lower than the voltage at HB. Current can flow into or out of LB.
9	HB	Resistor B High Terminal. The voltage at HB can be higher or lower than the voltage at LB. Current can flow into or out of HB.
10	WB	Resistor B Wiper Terminal
11	GND	Ground
12	$\overline{\text{INCB}}$	Register B Wiper Increment Control Input. With UDB low, a high-to-low transition at $\overline{\text{INCB}}$ decrements the WB position towards LB. With UDB high, a high-to-low transition at $\overline{\text{INCB}}$ increments WB position toward HB.
13	$\overline{\text{INCA}}$	Register A Wiper Increment Control Input. With UDA low, a high-to-low transition at $\overline{\text{INCA}}$ decrements the WA position towards LA. With UDA high, a high-to-low transition at $\overline{\text{INCA}}$ increments WA position toward HA.
14	$\overline{\text{CSB}}$	Active-Low Register B Chip-Select Input. Drive $\overline{\text{CSB}}$ low to change wiper position WB through $\overline{\text{INCB}}$ and UDB.



Detailed Description

The MAX5389 dual, 256-tap, volatile, low-voltage linear taper digital potentiometer offers three end-to-end resistance values of 10kΩ, 50kΩ, and 100kΩ. The potentiometer consists of 255 fixed resistors in series between terminals H<sub>-</sub> and L<sub>-</sub>. The potentiometer wiper, W<sub>-</sub>, is programmable to access any one of the 256 tap points on the resistor string. On power-up, the wiper position is set to midscale (tap 128).

The potentiometers are programmable independent of each other. The MAX5389 features an up/down interface.

Up/Down Interface

Logic inputs  $\overline{CS}_-$ , UD<sub>-</sub>, and  $\overline{INC}_-$  determine the wiper position of the device (Table 1). With  $\overline{CS}_-$  low and UD<sub>-</sub> high, a high-to-low (falling edge) transition on  $\overline{INC}_-$  increments the internal counter which moves the wiper, W<sub>-</sub>, closer to H<sub>-</sub>. When both  $\overline{CS}_-$  and UD<sub>-</sub> are low, the falling edge of  $\overline{INC}_-$  decrements the internal counter and moves the tap point, W<sub>-</sub> closer to L<sub>-</sub> (Figure 2). The wiper per-

forms a make-before-break transition ensuring that W<sub>-</sub> is never disconnected from the resistor string during a transition from one tap point to another. When the wiper is at either end of the resistor array additional transitions in the direction of the end point do not change the counter value.

Table 1. Up/Down Control Table

$\overline{CS}_-$	UD <sub>-</sub>	$\overline{INC}_-$	W <sub>-</sub>
H	X	X	No change
L	L	↑	No change
L	H	↑	No change
L	L	↓	Decrement
L	H	↓	Increment

X = Don't care.  
↑ = Low-to-high transition.  
↓ = High-to-low transition.

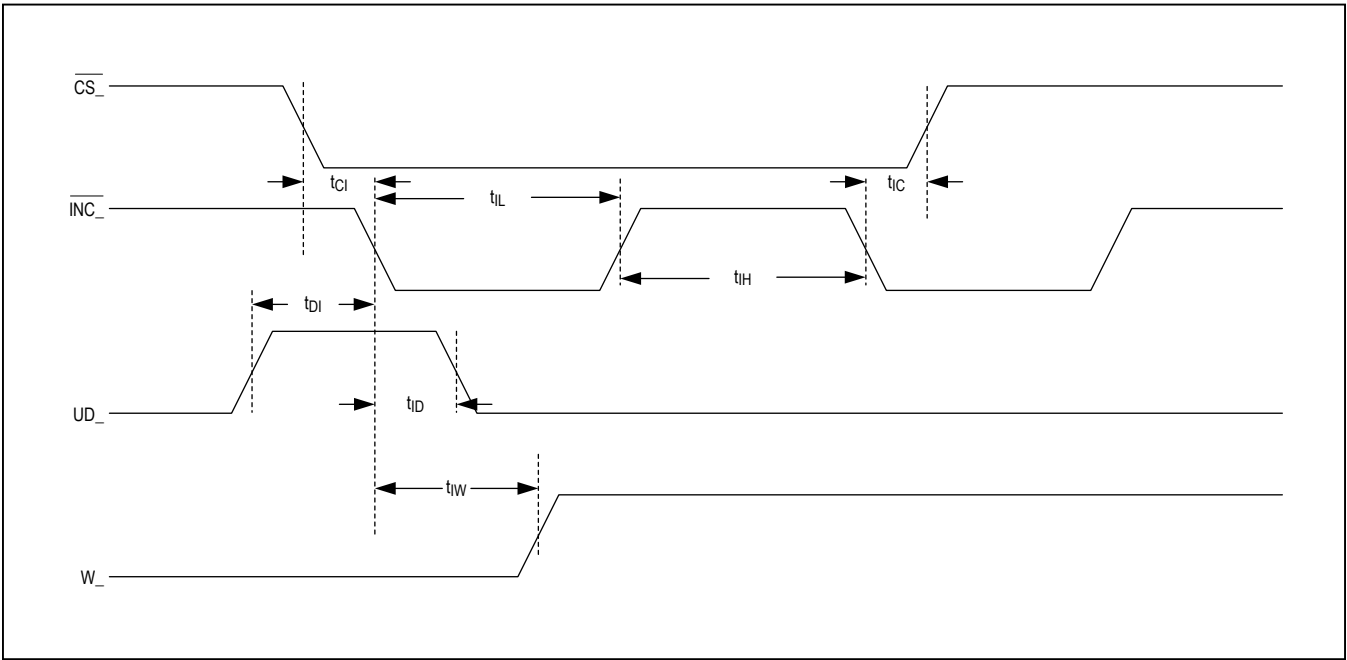


Figure 2. Up/Down Interface Timing Diagram

## Applications Information

### Variable Gain Amplifier

Figure 3 shows a potentiometer adjusting the gain of a noninverting amplifier. Figure 4 shows a potentiometer adjusting the gain of an inverting amplifier.

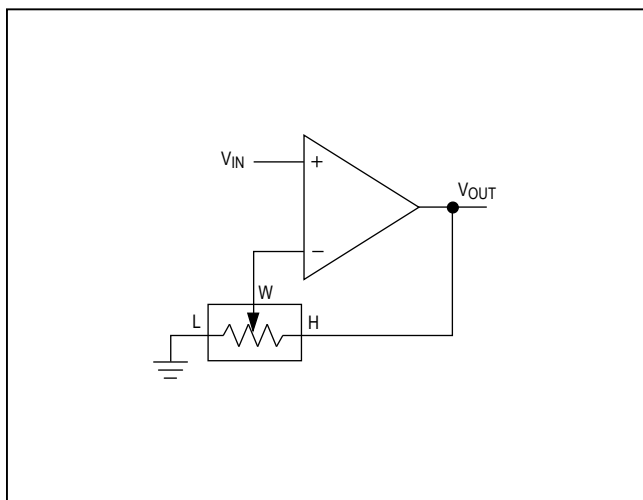


Figure 3. Variable Gain Noninverting Amplifier

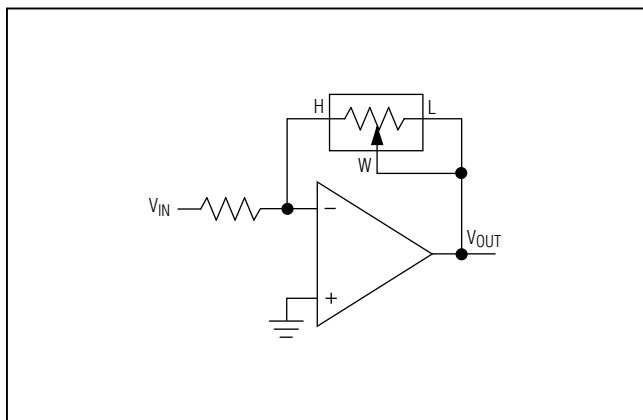


Figure 4. Variable Gain Inverting Amplifier

### Adjustable Dual Linear Regulator

Figure 5 shows an adjustable dual linear regulator using a dual potentiometer as two variable resistors.

### Adjustable Voltage Reference

Figure 6 shows an adjustable voltage reference circuit using a potentiometer as a voltage-divider.

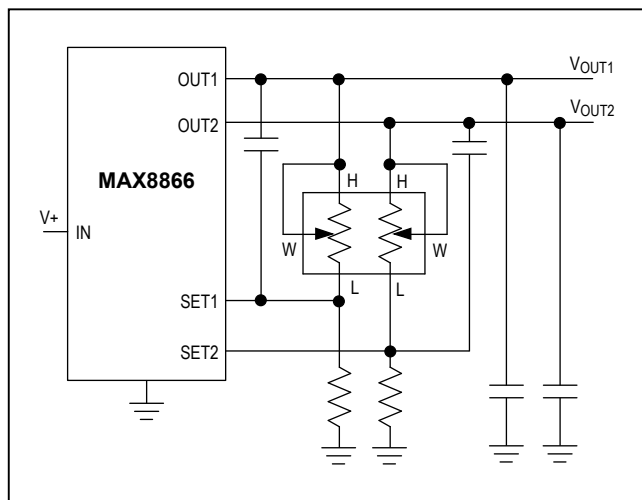


Figure 5. Adjustable Dual Linear Regulator

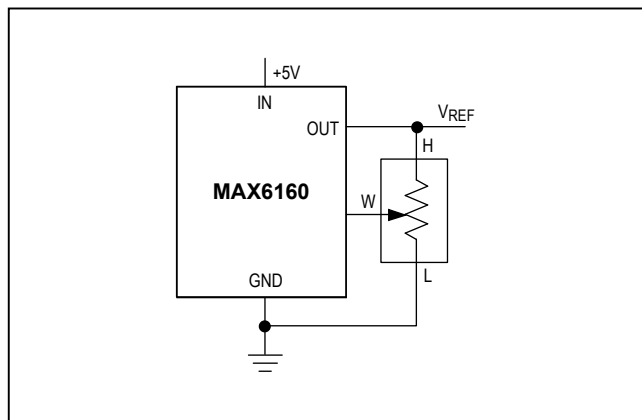


Figure 6. Adjustable Voltage Reference

**Variable Gain Current to Voltage Converter**

Figure 7 shows a variable gain current to voltage converter using a potentiometer as a variable resistor.

**LCD Bias Control**

Figure 8 shows a positive LCD bias control circuit using a potentiometer as a voltage-divider.

Figure 9 shows a positive LCD bias control circuit using a potentiometer as a variable resistor

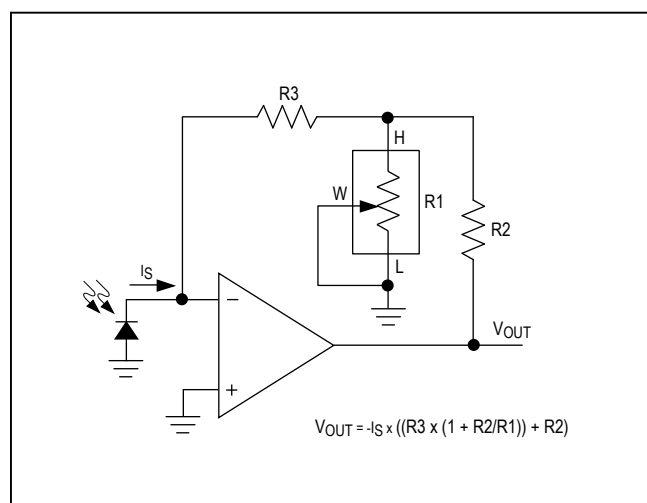


Figure 7. Variable Gain I-to-V Converter

**Programmable Filter**

Figure 10 shows a programmable filter using a dual potentiometer.

**Offset Voltage Adjustment Circuit**

Figure 11 shows an offset voltage adjustment circuit using a dual potentiometer

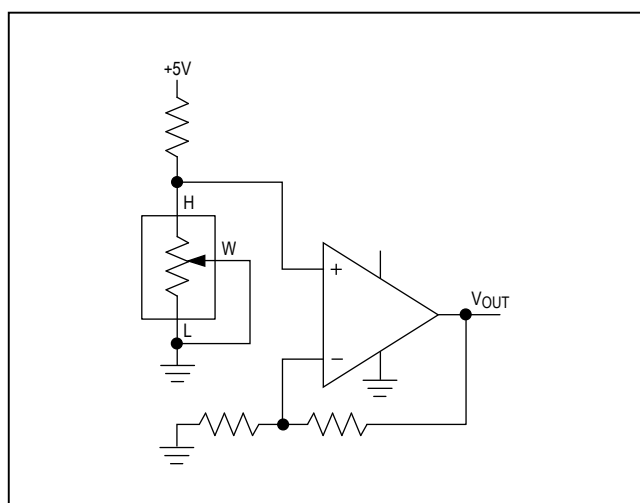


Figure 9. Positive LCD Bias Control Using a Variable Resistor

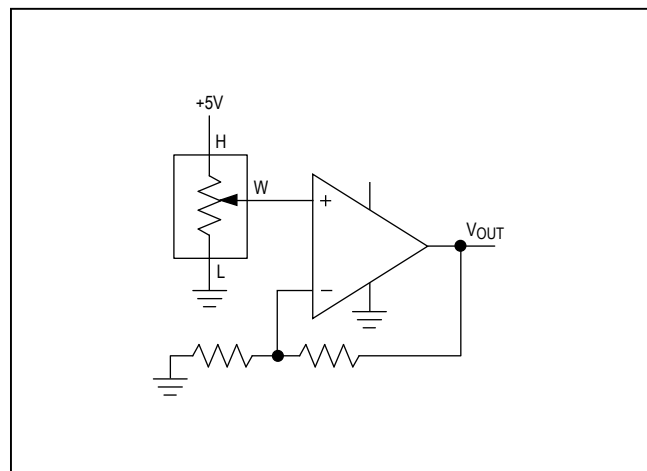


Figure 8. Positive LCD Bias Control Using a Voltage-Divide

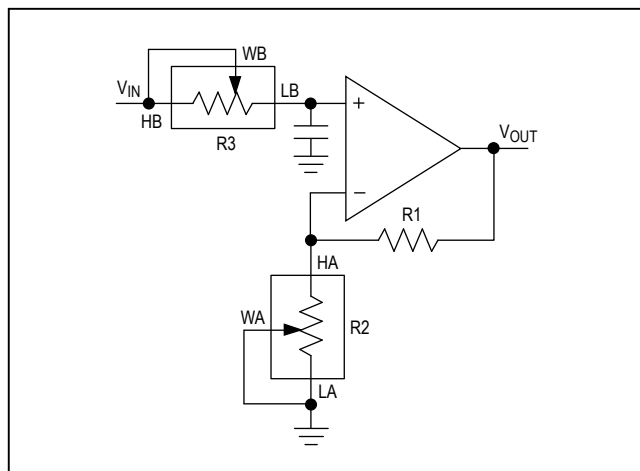


Figure 10. Programmable Filter

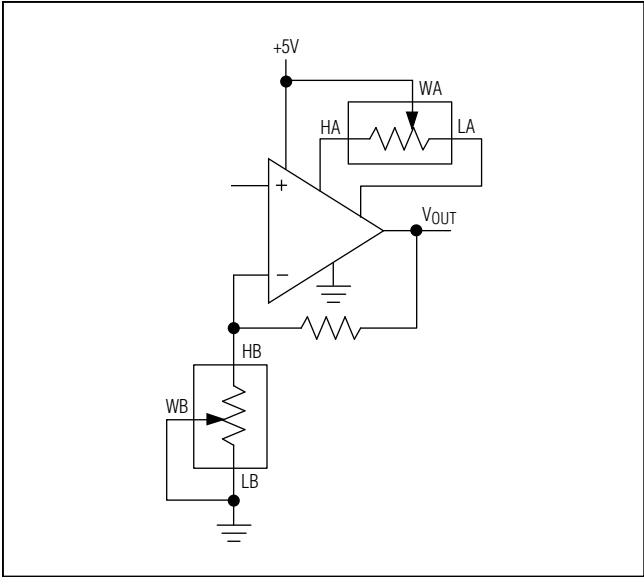


Figure 11. Offset Voltage Adjustment Circuit

Process Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP	U14+1	<a href="#">21-0066</a>	<a href="#">90-0113</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/10	Initial release	—
1	4/10	Added Soldering Temperature in <i>Absolute Maximum Ratings</i> ; corrected code in Conditions of -3dB Bandwidth specification in Electrical Characteristics; corrected Table 1 and Figure 5	2, 3, 9, 10
2	11/10	Updated <i>Electrical Characteristics</i> table globals, updated drawings for optimal circuit operation	2, 3, 10, 11, 12
3	9/14	Removed automotive reference from data sheet	1

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