Dual Monolithic 1.4A, 1.1MHz Step-Down Switching Regulator

FEATURES

- **Wide Input Voltage Range**
  LT1940: 3.6V to 25V
  LT1940L: 3.6V to 7V
- **Two 1.4A Output Switching Regulators with Internal Power Switches**
- **Constant 1.1MHz Switching Frequency**
- **Anti-Phase Switching Reduces Ripple**
- Independent Shutdown/Soft-Start Pins
- Independent Power Good Indicators Ease Supply Sequencing
- Uses Small Inductors and Ceramic Capacitors
- Small 16-Lead Thermally Enhanced TSSOP Surface Mount Package

APPLICATIONS

- Disk Drives
- DSP Power Supplies
- Wall Transformer Regulation
- Distributed Power Regulation
- DSL Modems
- Cable Modems

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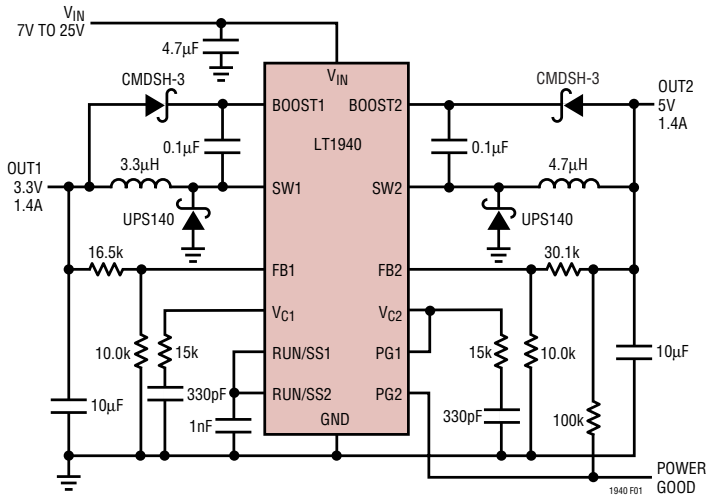
DESCRIPTION

The LT®1940 is a dual current mode PWM step-down DC/DC converter with internal 2A power switches. Both converters are synchronized to a single 1.1MHz oscillator and run with opposite phases, reducing input ripple current. The output voltages are set with external resistor dividers, and each regulator has independent shutdown and soft-start circuits. Each regulator generates a power-good signal when its output is in regulation, easing power supply sequencing and interfacing with microcontrollers and DSPs.

The LT1940's 1.1MHz switching frequency allows the use of tiny inductors and capacitors, resulting in a very small dual 1.4A output solution. Constant frequency and ceramic capacitors combine to produce low, predictable output ripple voltage. With its wide input range of 3.6V to 25V, the LT1940 regulates a wide variety of power sources, from 4-cell batteries and 5V logic rails to unregulated wall transformers, lead acid batteries and distributed-power supplies. The LT1940L is intended to operate from regulated 5V supplies. A current mode PWM architecture provides fast transient response with simple compensation components and cycle-by-cycle current limiting. Frequency foldback and thermal shutdown provide additional protection.

TYPICAL APPLICATION



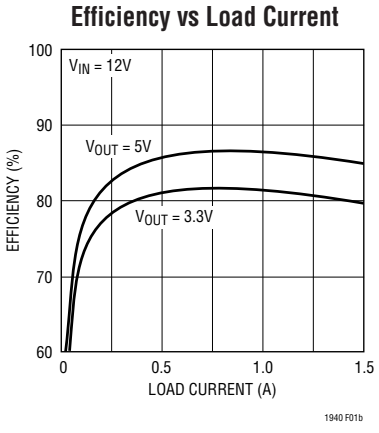


Figure 1. 3.3V and 5V Dual Output Step-Down Converter with Output Sequencing (LT1940)

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage
- LT1940 ..... (–0.3), 25V
- LT1940L ..... (–0.3), 7V

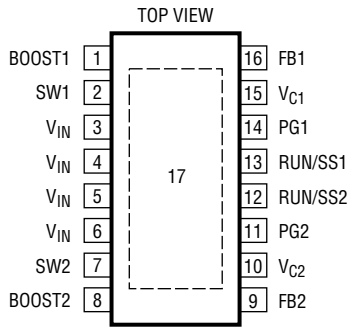
BOOST Pin Voltage
- LT1940 ..... 35V
- LT1940L 16V

BOOST Pin Above SW Pin
- LT1940 ..... 25V
- LT1940L 16V

PG Pin Voltage
- LT1940 ..... 25V
- LT1940L 7V

SW Voltage ..... V_{IN}
RUN/SS, FB Pins 6V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) ... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
16-LEAD PLASTIC TSSOP
EXPOSED PAD (PIN 17) IS GND
MUST BE SOLDERED TO PCB

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W

ORDER PART NUMBER
LT1940EFE LT1940LEFE
FE PART MARKING
1940EFE 1940LEFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_{BOOST} = 8V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage		●		3.4	3.6	V
Quiescent Current	Not Switching			3.8	4.8	mA
Shutdown Current	V_{RUNSS} = 0V			30	45	µA
Feedback Voltage			1.230	1.250	1.270	V
	0°C to 70°C	●	1.225	1.250	1.270	V
	–40°C to 85°C	●	1.215	1.250	1.270	V
FB Pin Bias Current	V_{FB} = 1.25V, V_C = 0.4V	●		240	1200	nA
Reference Line Regulation	LT1940: V_{IN} 5V to 25V			0.005		%/V
	LT1940L: V_{IN} 4V to 7V			0.005		%/V
Error Amp GM				330		uMhos
Error Amp Voltage Gain				180		
V_C Source Current	V_{FB} = 1V			42		µA
V_C Sink Current	V_{FB} = 1.5V			60		µA
V_C Pin to Switch Current Gain				2.4		A/V
V_C Switching Threshold				0.75		V
V_C Clamp Voltage				1.8		V
Switching Frequency	V_{FB} = 1.1V		1	1.1	1.25	MHz
		●	0.95	1.1	1.35	MHz
Switching Phase			150	180	210	Deg
Maximum Duty Cycle		●	78	88		%
Frequency Shift Threshold on FB	f_{SW} = 1MHz			0.5		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_{BOOST} = 8V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Foldback Frequency	V_{FB} = 0V			150		kHz
Switch Current Limit	Note 3		1.8	2.4	3.2	A
Switch V_{CESAT}	I_{SW} = 1A			210	320	mV
Switch Leakage Current					10	µA
Minimum Boost Voltage Above Switch (Note 4)	I_{SW} = 1A			1.8	2.5	V
BOOST Pin Current	I_{SW} = 1A			20	30	mA
RUN/SS Current				2.3		µA
RUN/SS Threshold			0.3	0.6		V
PG Threshold Offset	V_{FB} Rising		90	125	160	mV
PG Voltage Output Low	V_{FB} = 1V, I_{PG} = 250µA			0.22	0.4	V
PG Pin Leakage	V_{PG} = 2V			0.1	1	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

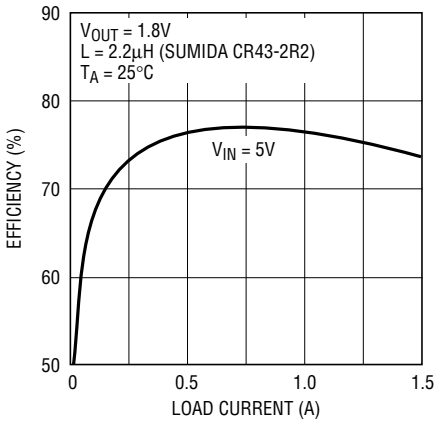
Note 2: The LT1940E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at high duty cycle.

Note 4: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

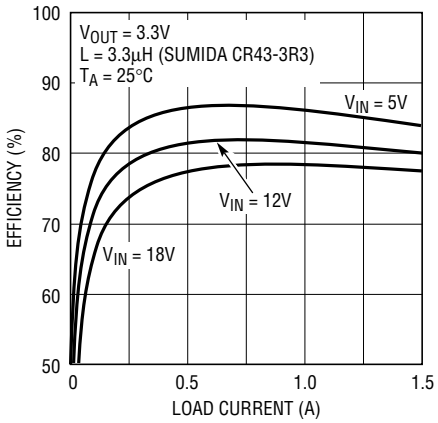
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency, V_{OUT} = 1.8V



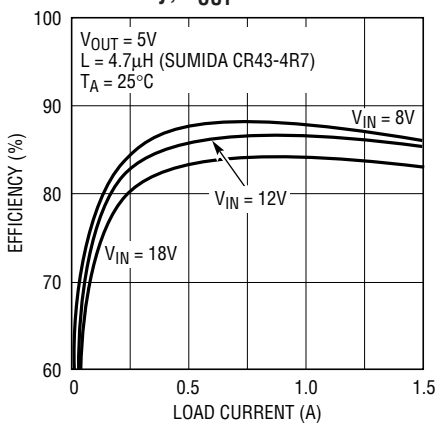
1940 G01

Efficiency, V_{OUT} = 3.3V



1940 G02

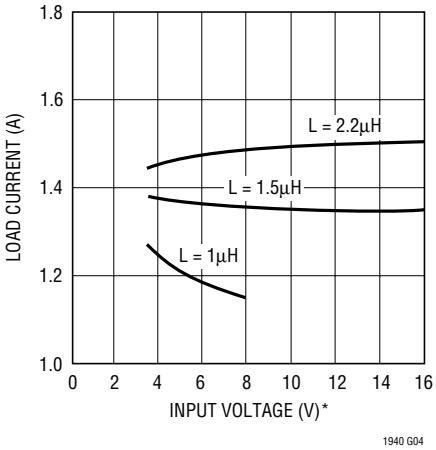
Efficiency, V_{OUT} = 5V



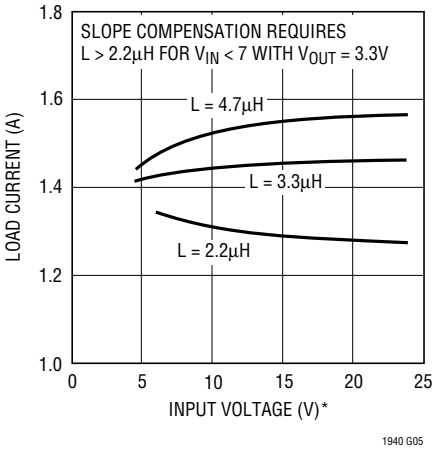
1940 G03

TYPICAL PERFORMANCE CHARACTERISTICS

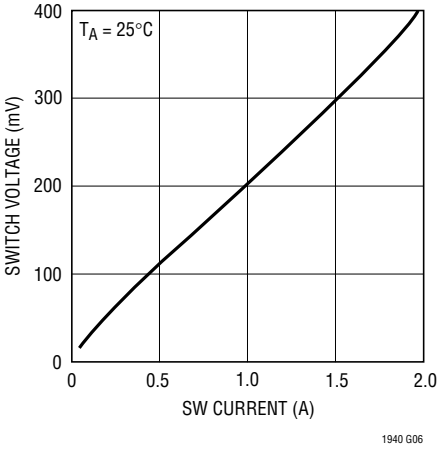
Maximum Load Current, V_{OUT} = 1.8V



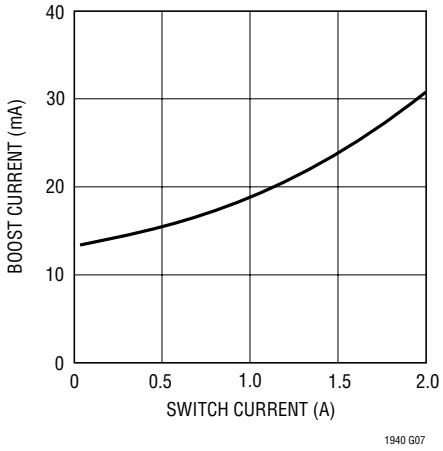
Maximum Load Current, V_{OUT} = 3.3V



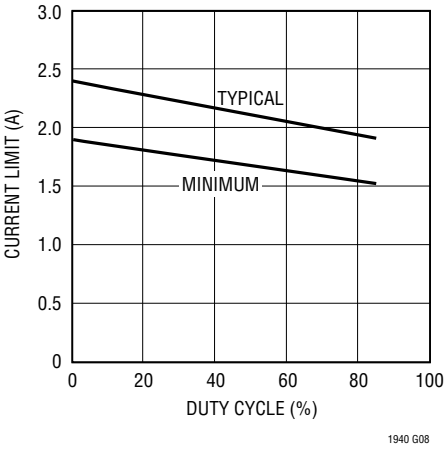
Switch V_{CESAT}



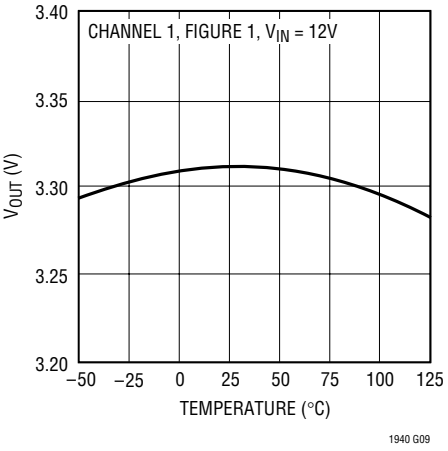
Boost Pin Current



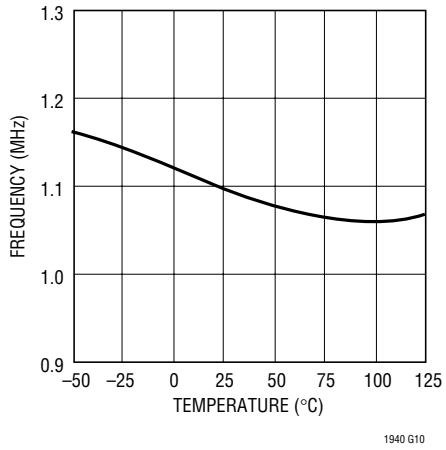
Current Limit vs Duty Cycle



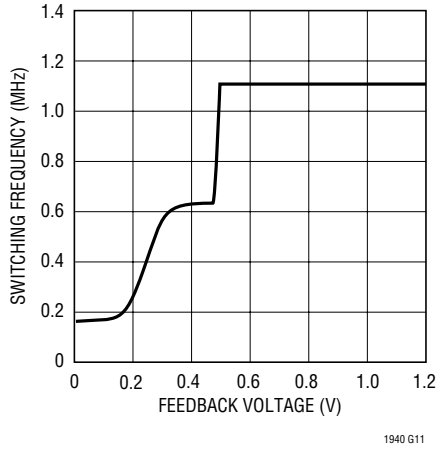
V_{OUT} vs Temperature



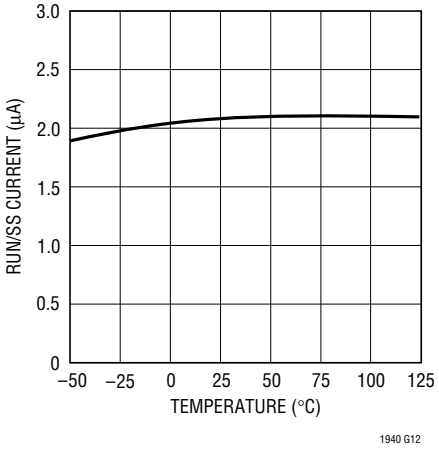
Frequency vs Temperature



Frequency Foldback



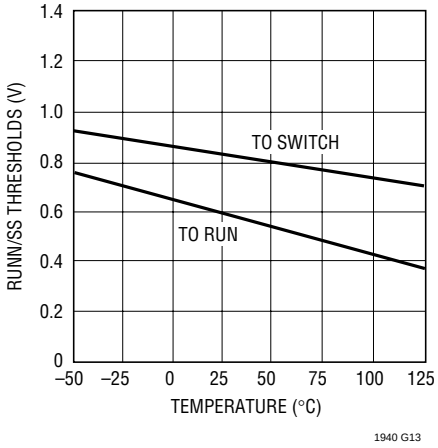
$I_{RUN/SS}$ vs Temperature



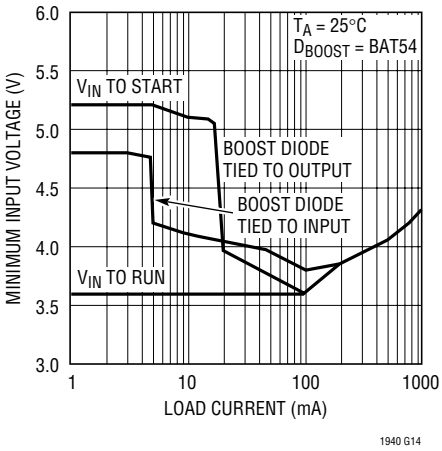
*Maximum V_{IN} is 7V for LT1940L.

TYPICAL PERFORMANCE CHARACTERISTICS

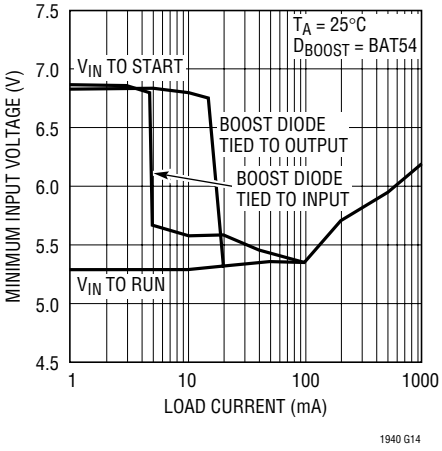
RUN/SS Thresholds vs Temperature



Minimum Input Voltage, V_{OUT} = 3.3V



Minimum Input Voltage, V_{OUT} = 5V



PIN FUNCTIONS

BOOST1, BOOST2 (Pins 1, 8): The BOOST pins are used to provide drive voltages, higher than the input voltage, to the internal bipolar NPN power switches.Tie through a diode from V_{OUT} or from V_{IN}.

SW1, SW2 (Pins 2, 7): The SW pins are the outputs of the internal power switches. Connect these pins to the inductors, catch diodes and boost capacitors.

V_{IN} (Pins 3, 4, 5, 6): The V_{IN} pins supply current to the LT1940's internal regulator and to the internal power switches. These pins must be tied to the same source, and must be locally bypassed.

FB1, FB2 (Pins 9, 16): The LT1940 regulates each feedback pin to 1.25V. Connect the feedback resistor divider taps to these pins.

V_{C1}, V_{C2} (Pins 10, 15): The V_C pins are the outputs of the internal error amps. The voltages on these pins control the peak switch currents. These pins are normally used to compensate the control loops, but can also be used to override the loops. Pull these pins to ground with an open drain to shut down each switching regulator.

PG1, PG2 (Pins 11, 14): The Power Good pins are the open collector outputs of an internal comparator. PG remains low until the FB pin is within 10% of the final regulation voltage. As well as indicating output regulation, the PG pins can be used to sequence the two switching regulators. These pins can be left unconnected. The PG outputs are valid when V_{IN} is greater than 2.4V and either of the RUN/SS pins is high. The PG comparators are disabled in shutdown.

RUN/SS1, RUN/SS2 (Pins 12, 13): The RUN/SS pins are use to shut down the individual switching regulators and the internal bias circuits. They also provide a soft-start function. To shut down either regulator, pull the RUN/SS pin to ground with an open drain or collector. Tie a capacitor from these pins to ground to limit switch current during start-up. If neither feature is used, leave these pins unconnected.

GND (Pin 17): The Exposed Pad of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The Exposed Pad must be soldered to the circuit board for proper operation.

BLOCK DIAGRAM

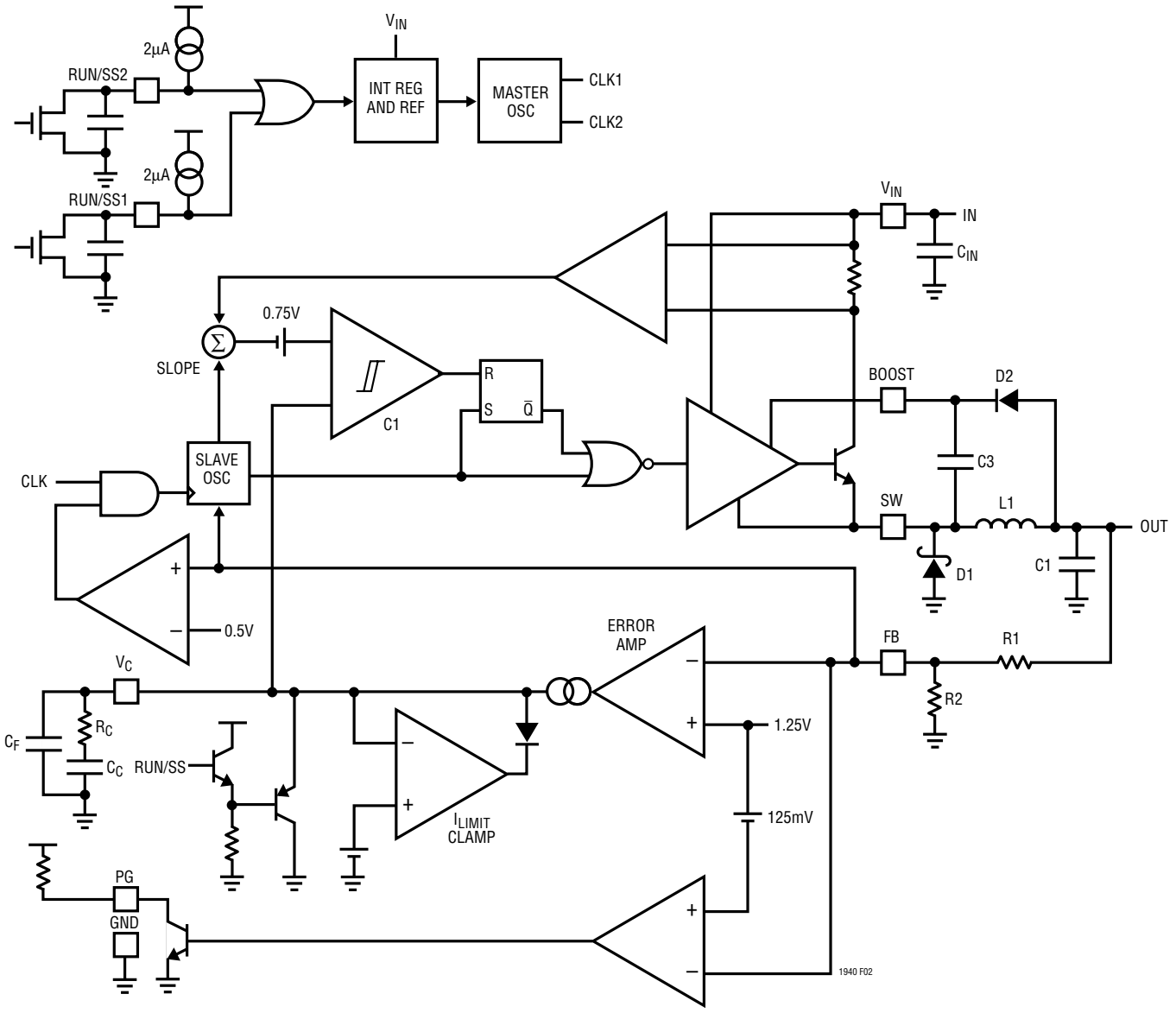


Figure 2. Block Diagram of the LT1940 with Associated External Components (One of Two Switching Regulators Shown)

The LT1940 is a dual, constant frequency, current mode buck regulator with internal 2A power switches. The two regulators share common circuitry including input source, voltage reference and oscillator, but are otherwise independent. This section describes the operation of the LT1940; refer to the Block Diagram.

If the RUN/SS (run/soft-start) pins are both tied to ground, the LT1940 is shut down and draws 30µA from the input source tied to V_{IN}. Internal 2µA current sources charge external soft-start capacitors, generating voltage ramps at these pins. If either RUN/SS pin exceeds 0.6V, the internal bias circuits turn on, including the internal regulator, 1.25V reference and 1.1MHz master oscillator. In this state, the LT1940 draws 3.5mA from V_{IN}, whether one or both RUN/SS pins are high. Neither switching regulator will begin to operate until its RUN/SS pin reaches ~0.8V. The master oscillator generates two clock signals of opposite phase.

The two switchers are current mode step-down regulators. This means that instead of directly modulating the

BLOCK DIAGRAM

duty cycle of the power switch, the feedback loop controls the peak current in the switch during each cycle. This current mode control improves loop dynamics and provides cycle-by-cycle current limit.

The Block Diagram shows only one of the two switching regulators. A pulse from the slave oscillator sets the RS flip-flop and turns on the internal NPN bipolar power switch. Current in the switch and the external inductor begins to increase. When this current exceeds a level determined by the voltage at V_C, current comparator C1 resets the flip-flop, turning off the switch. The current in the inductor flows through the external Schottky diode, and begins to decrease. The cycle begins again at the next pulse from the oscillator. In this way the voltage on the V_C pin controls the current through the inductor to the output. The internal error amplifier regulates the output voltage by continually adjusting the V_C pin voltage.

The threshold for switching on the V_C pin is 0.75V, and an active clamp of 1.8V limits the output current. The V_C pin is also clamped to the RUN/SS pin voltage. As the internal current source charges the external soft-start capacitor, the current limit increases slowly.

Each switcher contains an independent oscillator. This slave oscillator is normally synchronized to the master oscillator. However, during start-up, short-circuit or overload conditions, the FB pin voltage will be near zero and an internal comparator gates the master oscillator clock signal. This allows the slave oscillator to run the regulator at a lower frequency. This frequency foldback behavior helps to limit switch current and power dissipation under fault conditions.

The switch driver operates from either the input or from the BOOST pin. An external capacitor and diode are used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation.

A power good comparator trips when the FB pin is at 90% of its regulated value. The PG output is an open collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. Power good is valid when the LT1940 is enabled (either RUN/SS pin is high) and V_{IN} is greater than ~2.4V.

APPLICATIONS INFORMATION

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the 1% resistors according to:

$$R1 = R2(V_{OUT}/1.25 - 1)$$

R2 should be 10.0kΩ or less to avoid bias current errors. Reference designators refer to the Block Diagram in Figure 2.

Input Voltage Range

The minimum input voltage is determined by either the LT1940's minimum operating voltage of ~3.5V, or by its maximum duty cycle. The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltages:

$$DC = (V_{OUT} + V_D)/(V_{IN} - V_{SW} + V_D)$$

where V_D is the forward voltage drop of the catch diode (~0.4V) and V_{SW} is the voltage drop of the internal switch (~0.3V at maximum load). This leads to a minimum input voltage of:

$$V_{INMIN} = (V_{OUT} + V_D)/DC_{MAX} - V_D + V_{SW}$$

with $DC_{MAX} = 0.78$.

A more detailed analysis includes inductor loss and the dependence of the diode and switch drop on operating current. A common application where the maximum duty cycle limits the input voltage range is the conversion of 5V to 3.3V. The maximum load current that the LT1940 can deliver at 3.3V depends on the accuracy of the 5V input supply. With a low loss inductor (DCR less than 80mΩ), the LT1940 can deliver 1A for $V_{IN} > 4.7V$ and 1.4A for $V_{IN} > 4.85V$.

APPLICATIONS INFORMATION

The maximum input voltage is determined by the absolute maximum ratings of the V_{IN} and BOOST pins and by the minimum duty cycle DC_{MIN} = 0.15:

$$V_{INMAX} = (V_{OUT} + V_D)/DC_{MIN} – V_D + V_{SW}.$$

This limits the maximum input voltage to ~14V with V_{OUT} = 1.8V and ~19V with V_{OUT} = 2.5V. Note that this is a restriction on the operating input voltage; the circuit will tolerate transient inputs up to the absolute maximum rating. For the LT1940L, the maximum input voltage is 7V.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = (V_{OUT} + V_D)/1.2$$

where V_D is the voltage drop of the catch diode (~0.4V) and L is in μH. With this value the maximum load current will be ~1.4A, independent of input voltage. The inductor's RMS current rating must be greater than your maximum load current and its saturation current should be about 30% higher. To keep efficiency high, the series resistance (DCR) should be less than 0.1Ω. Table 1 lists several vendors and types that are suitable.

Of course, such a simple design guide will not always result in the optimum inductor for your application. A larger value provides a slightly higher maximum load current, and will reduce the output voltage ripple. If your load is lower than 1.4A, then you can decrease the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that if the inductance differs from the simple rule above, then the maximum load current will depend on input voltage. There are several graphs in the Typical Performance Characteristics section of this data sheet that show the maximum load current as a function of input voltage and inductor value for several popular output voltages. Also, low inductance may result in discontinuous mode operation, which is okay, but further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} < 0.5$), there is a minimum inductance required to avoid subharmonic oscillations. See AN19. The discussion below assumes continuous inductor current.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT1940 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT1940 will deliver depends on the current limit, the inductor value, and the input and output voltages. L is chosen based on output current requirements, output voltage ripple requirements, size restrictions and efficiency goals.

When the switch is off, the inductor sees the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = (1 – DC)(V_{OUT} + V_D)/(L \bullet f)$$

where f is the switching frequency of the LT1940 and L is the value of the inductor. The peak inductor and switch current is

$$I_{SWPK} = I_{LPK} = I_{OUT} + \Delta I_L/2.$$

To maintain output regulation, this peak current must be less than the LT1940's switch current limit I_{LIM}. I_{LIM} is at least 1.8A at low duty cycle and decreases linearly to 1.5A at DC = 0.8. The maximum output current is a function of the chosen inductor value:

$$I_{OUTMAX} = I_{LIM} – \Delta I_L/2 = 1.8A \bullet (1 – 0.21 \bullet DC) – \Delta I_L/2$$

If the inductor value is chosen so that the ripple current is small, then the available output current will be near the switch current limit.

One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors, and choose one to meet cost or space goals. Then use these equations to check that the LT1940 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT} is less than $\Delta I_L/2$ as calculated above.

APPLICATIONS INFORMATION

Table 1. Inductors.

Part Number	Value (μH)	I_{SAT} (A) DC	DCR (Ω)	Height (mm)
Sumida				
CR43-1R4	1.4	2.52	0.056	3.5
CR43-2R2	2.2	1.75	0.071	3.5
CR43-3R3	3.3	1.44	0.086	3.5
CR43-4R7	4.7	1.15	0.109	3.5
CDRH3D16-1R5	1.5	1.55	0.040	1.8
CDRH3D16-2R2	2.2	1.20	0.050	1.8
CDRH3D16-3R3	3.3	1.10	0.063	1.8
CDRH4D28-3R3	3.3	1.57	0.049	3.0
CDRH4D28-4R7	4.7	1.32	0.072	3.0
CDRH5D28-5R3	5.3	1.9	0.028	3.0
CDRH5D18-4R1	4.1	1.95	0.042	2.0
Coilcraft				
DO1606T-152	1.5	2.10	0.060	2.0
DO1606T-222	2.2	1.70	0.070	2.0
DO1606T-332	3.3	1.30	0.100	2.0
DO1606T-472	4.7	1.10	0.120	2.0
DO1608C-152	1.5	2.60	0.050	2.9
DO1608C-222	2.2	2.30	0.070	2.9
DO1608C-332	3.3	2.00	0.080	2.9
DO1608C-472	4.7	1.50	0.090	2.9
1812PS-222M	2.2	1.7	0.070	3.81
1008PS-182M	1.8	2.1	0.090	2.74
Murata				
LQH32CN1R0M11L	1.0	1.00	0.078	2.2
LQH32CN2R2M11L	2.2	0.79	0.126	2.2
LQH43CN1R5M01L	1.5	1.00	0.090	2.8
LQH43CN2R2M01L	2.2	0.90	0.110	2.8
LQH43CN3R3M01L	3.3	0.80	0.130	2.8

Input Capacitor Selection

Bypass the input of the LT1940 circuit with a 4.7μF or higher ceramic capacitor of X7R or X5R type. A lower value or a less expensive Y5V type can be used if there is additional bypassing provided by bulk electrolytic or tantalum capacitors. The following paragraphs describe the input capacitor considerations in more detail.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT1940 and to force this very high frequency switching current into a tight local loop, minimizing EMI. The input capacitor must have low impedance at the switching frequency to do this effectively, and it must have an adequate ripple current rating. With two switchers operating at the same frequency but with different phases and duty cycles, calculating the input capacitor RMS current is not simple. However, a conservative value is the RMS input current for the channel that is delivering most power ($V_{OUT} \bullet I_{OUT}$). This is given by:

$$C_{INRMS} = I_{OUT} \sqrt{[V_{OUT} \bullet (V_{IN} - V_{OUT})]}/V_{IN} < I_{OUT}/2$$

and is largest when $V_{IN} = 2V_{OUT}$ (50% duty cycle). As the second, lower power channel draws input current, the input capacitor's RMS current actually decreases as the out-of-phase current cancels the current drawn by the higher power channel. Considering that the maximum load current from a single channel is ~1.4A, RMS ripple current will always be less than 0.7A.

The high frequency of the LT1940 reduces the energy storage requirements of the input capacitor, so that the capacitance required is less than 10μF. The combination of small size and low impedance (low equivalent series resistance or ESR) of ceramic capacitors make them the preferred choice. The low ESR results in very low voltage ripple and the capacitors can handle plenty of ripple current. They are also comparatively robust and can be used in this application at their rated voltage. X5R and X7R types are stable over temperature and applied voltage, and give dependable service. Other types (Y5V and Z5U) have very large temperature and voltage coefficients of capacitance, so they may have only a small fraction of their nominal capacitance in your application. While they will still handle the RMS ripple current, the input voltage ripple may become fairly large, and the ripple current may end up flowing from your input supply or from other bypass capacitors in your system, as opposed to being fully sourced from the local input capacitor.

An alternative to a high value ceramic capacitor is a lower value along with a larger electrolytic capacitor, for example a 1μF ceramic capacitor in parallel with a low ESR tantalum capacitor. For the electrolytic capacitor, a value larger than 10μF will be required to meet the ESR and ripple current requirements. Because the input capacitor

APPLICATIONS INFORMATION

is likely to see high surge currents when the input source is applied, tantalum capacitors should be surge rated. The manufacturer may also recommend operation below the rated voltage of the capacitor. Be sure to place the 1µF ceramic as close as possible to the V_{IN} and GND pins on the IC for optimal noise immunity.

A final caution is in order regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit. If power is applied quickly (for example by plugging the circuit into a live power source) this tank can ring, doubling the input voltage and damaging the LT1940. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor in parallel with the ceramic capacitor. For details, see AN88.

Output Capacitor Selection

For 5V and 3.3V outputs with greater than 1A output, a 10µF 6.3V ceramic capacitor (X5R or X7R) at the output results in very low output voltage ripple and good transient response. For lower voltages, 10µF is adequate but increasing C_{OUT} to 15µF or 22µF will improve transient performance. Other types and values can be used; the following discusses tradeoffs in output ripple and transient performance.

The output capacitor filters the inductor current to generate an output with low voltage ripple. It also stores energy in order satisfy transient loads and to stabilize the LT1940's control loop. Because the LT1940 operates at a high frequency, you don't need much output capacitance. Also, the current mode control loop doesn't require the presence of output capacitor series resistance (ESR). For these reasons, you are free to use ceramic capacitors to achieve very low output ripple and small circuit size.

Estimate output ripple with the following equations:

$V_{RIPPLE} = \Delta I_L/(8f\ C_{OUT})$ for ceramic capacitors, and

$V_{RIPPLE} = \Delta I_L$ ESR for electrolytic capacitors (tantalum and aluminum);

where ΔI_L is the peak-to-peak ripple current in the inductor. The RMS content of this ripple is very low, and the RMS current rating of the output capacitor is usually not of concern.

Another constraint on the output capacitor is that it must have greater energy storage than the inductor; if the stored energy in the inductor is transferred to the output, you would like the resulting voltage step to be small compared to the regulation voltage. For a 5% overshoot, this requirement becomes $C_{OUT} > 10L(I_{LIM}/V_{OUT})^2$.

Finally, there must be enough capacitance for good transient performance. The last equation gives a good starting point. Alternatively, you can start with one of the designs in this data sheet and experiment to get the desired performance. This topic is covered more thoroughly in the section on loop compensation.

The high performance (low ESR), small size and robustness of ceramic capacitors make them the preferred type for LT1940 applications. However, all ceramic capacitors are not the same. As mentioned above, many of the higher value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and temperature extremes. Because the loop stability and transient response depend on the value of C_{OUT}, you may not be able to tolerate this loss. Use X7R and X5R types.

You can also use electrolytic capacitors. The ESRs of most aluminum electrolytics are too large to deliver low output ripple. Tantalum and newer, lower ESR organic electrolytic capacitors intended for power supply use are suitable, and the manufacturers will specify the ESR. The choice of capacitor value will be based on the ESR required for low ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give you similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current. Table 2 lists several capacitor vendors.

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Table 2. Low-ESR Surface Mount Capacitors

Vendor	Type	Series
Taiyo Yuden	Ceramic X5R, X7R	
AVX	Ceramic X5R, X7R Tantalum	 TPS
Kemet	Tantalum Ta Organic Al Organic	T491,T494,T495 T520 A700
Sanyo	Ta or Al Organic	POSCAP
Panasonic	Al Organic	SP CAP
TDK	Ceramic X5R, X7R	

Catch Diode

Use a 1A Schottky diode for the catch diode (D1 in Figure 2). The diode must have a reverse voltage rating greater than the maximum input voltage. The ON Semiconductor MBRM120LT3 (20V) and MBRM130LT3 (30V) are good choices; they have a tiny package with good thermal properties. Many vendors have surface mount versions of the 1N5817 (20V) and 1N5818 (30V) 1A Schottky diodes such as the Microsemi UPS120 that are suitable.

Boost Pin Considerations

The capacitor and diode tied to the BOOST pin generate a voltage that is higher than the input voltage. In most cases a 0.1µF capacitor and fast switching diode (such as the CMDSH-3 or FMMD914) will work well. Figure 3 shows three ways to arrange the boost circuit. The BOOST pin must be more than 2.5V above the SW pin for full efficiency. For outputs of 3.3V and higher the standard circuit (Figure 3a) is best. For outputs between 2.8V and 3.3V, use a small Schottky diode (such as the BAT-54). For lower output voltages the boost diode can be tied to the input (Figure 3b). The circuit in Figure 3a is more efficient because the BOOST pin current comes from a lower voltage source. Finally, as shown in Figure 3c, the anode of the boost diode can be tied to another source that is at least 3V. For example, if you are generating 3.3V and 1.8V and the 3.3V is on whenever the 1.8V is on, the 1.8V boost diode can be connected to the 3.3V output. In any case, you must also be sure that the maximum voltage at the BOOST pin is less than the maximum specified in the Absolute Maximum Ratings section.

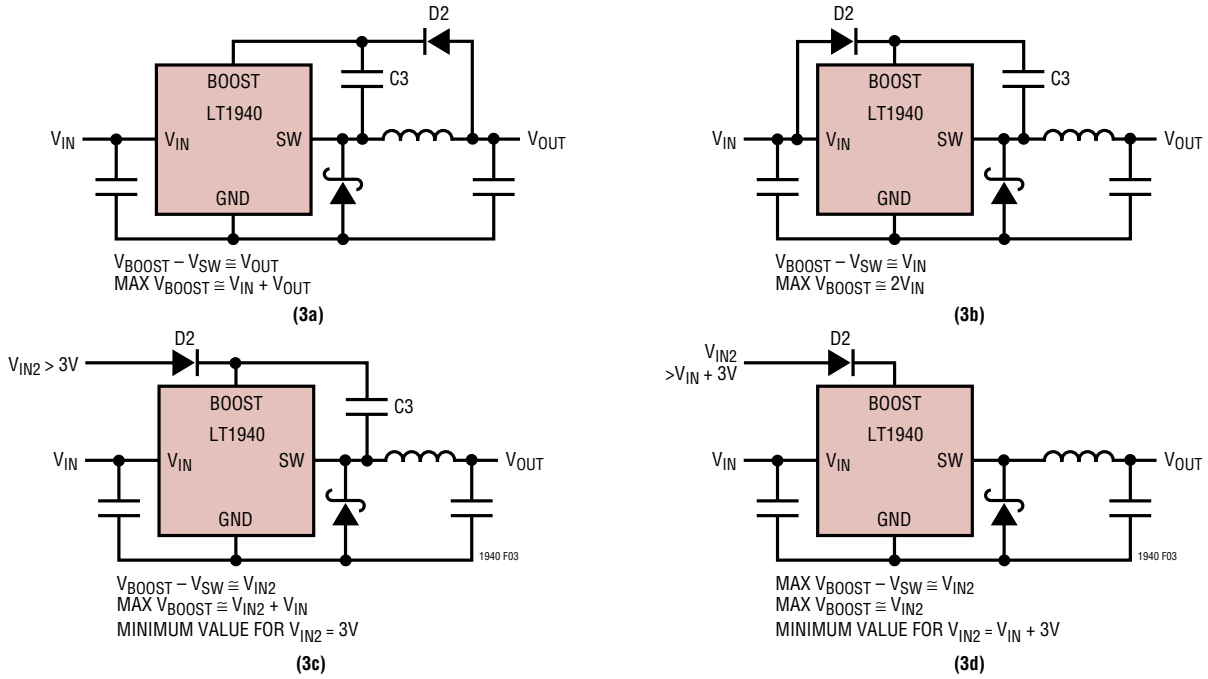

Figure 3. Generating the Boost Voltage

APPLICATIONS INFORMATION

The boost circuit can also run directly from a DC voltage that is higher than the input voltage by more than 3V, as in Figure 3d. The diode is used to prevent damage to the LT1940 in case V_{IN2} is held low while V_{IN} is present. The circuit saves several components (both BOOST pins can be tied to D2). However, efficiency may be lower and dissipation in the LT1940 may be higher. Also, if V_{IN2} is absent, the LT1940 will still attempt to regulate the output, but will do so with very low efficiency and high dissipation because the switch will not be able to saturate, dropping 1.5V to 2V in conduction.

The minimum input voltage of an LT1940 application is limited by the minimum operating voltage (<3.6V) and by the maximum duty cycle as outlined above. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT1940 is turned on with its RUN/SS pin when the output is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. The Typical Performance Characteristics section shows plots of the minimum load current to start and to run as a function of input voltage for 3.3V and 5V outputs. In many cases the discharged output capacitor will present a load to the switcher which will allow it to start. The plots show the worst-case situation where V_{IN} is ramping very slowly. Use a Schottky diode (such as the BAT-54) for the lowest start-up voltage.

Frequency Compensation

The LT1940 uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT1940 does not require the ESR of the output capacitor for stability so you are free to use ceramic capacitors to achieve low output ripple and small circuit size.

Frequency compensation is provided by the components tied to the V_C pin. Generally a capacitor and a resistor in series to ground determine loop gain. In addition, there is a lower value capacitor in parallel. This capacitor is not part of the loop compensation but is used to filter noise at the switching frequency.

Loop compensation determines the stability and transient performance. Designing the compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitor. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

Figure 4 shows an equivalent circuit for the LT1940 control loop. The error amp is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current, and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. In most cases a zero is required and comes from either the output capacitor ESR or from a resistor in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (C_{PL}) across the feedback divider may improve the transient response.

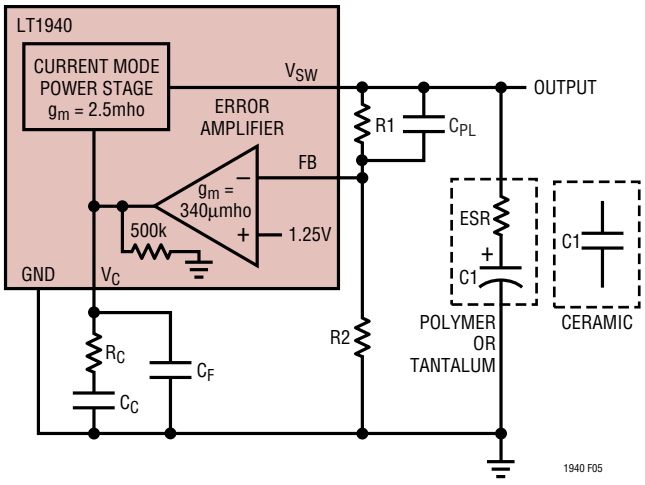

Figure 4. Model for Loop Response

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Soft-Start and Shutdown

The RUN/SS (Run/Soft-Start) pins are used to place the individual switching regulators and the internal bias circuits in shutdown mode. They also provide a soft-start function. To shut down either regulator, pull the RUN/SS pin to ground with an open-drain or collector. If both RUN/SS pins are pulled to ground, the LT1940 enters its shutdown mode with both regulators off and quiescent current reduced to ~30μA. Internal 2μA current sources pull up on each pin. If either pin reaches ~0.5V, the internal bias circuits start and the quiescent current increases to ~3.5mA.

If a capacitor is tied from the RUN/SS pin to ground, then the internal pull-up current will generate a voltage ramp on this pin. This voltage clamps the V_C pin, limiting the peak switch current and therefore input current during start up. A good value for the soft-start capacitor is C_{OUT}/10,000, where C_{OUT} is the value of the output capacitor.

The RUN/SS pins can be left floating if the shutdown feature is not used. They can also be tied together with a single capacitor providing soft-start. The internal current sources will charge these pins to ~2.5V.

The RUN/SS pins provide a soft-start function that limits peak input current to the circuit during start-up. This helps to avoid drawing more current than the input source can supply or glitching the input supply when the LT1940 is enabled. The RUN/SS pins do not provide an accurate delay to start or an accurately controlled ramp at the output voltage, both of which depend on the output capacitance and the load current. However, the power good indicators can be used to sequence the two outputs, as described below.

Power Good Indicators

The PG pin is the open collector output of an internal comparator. PG remains low until the FB pin is within 10% of the final regulation voltage. Tie the PG pin to any supply with a pull-up resistor that will supply less than 250μA. Note that this pin will be open when the LT1940 is placed in shutdown mode (both RUN/SS pins at ground) regardless of the voltage at the FB pin. Power good is valid when the LT1940 is enabled (either RUN/SS pin is high) and V_{IN} is greater than ~2.4V.

Output Sequencing

The PG and RUN/SS pins can be used to sequence the two outputs. Figure 5 shows several circuits to do this. In each case channel 1 starts first. Note that these circuits sequence the outputs during start-up. When shut down the two channels turn off simultaneously.

In Figure 5a, a larger capacitor on RUN/SS2 delays channel 2 with respect to channel 1. The soft-start capacitor on RUN/SS2 should be at least twice the value of the capacitor on RUN/SS1. A larger ratio may be required, depending on the output capacitance and load on each channel. Make sure to test the circuit in the system before deciding on final values for these capacitors.

The circuit in Figure 5b requires the fewest components, with both channels sharing a single soft-start capacitor. The power good comparator of channel 1 disables channel 2 until output 1 is in regulation.

For independent control of channel 2, use the circuit in Figure 5c. The capacitor on RUN/SS1 is smaller than the capacitor on RUN/SS2. This allows the LT1940 to start up and enable its power good comparator before RUN/SS2 gets high enough to allow channel 2 to start switching. Channel 2 only operates when it is enabled with the external control signals and output 1 is in regulation.

The circuit in Figure 5a leaves both power good indicates free. However, the circuits in Figures 5b and 5c have another advantage. As well as sequencing the two outputs at start-up, they also disable channel 2 if output 1 falls out of regulation (due to a short circuit or a collapsing input voltage).

Finally, be aware that **the circuit in Figure 5d does not work**, because the power good comparators are disabled in shutdown. When the system is placed in shutdown mode by pulling down on RUN/SS1, then output 1 will go low, PG1 will pull down on RUN/SS2, and the LT1940 will enter its low current shutdown state. This disables PG1, and RUN/SS2 ramps up again to enable the LT1940. The circuit will oscillate and pull extra current from the input.

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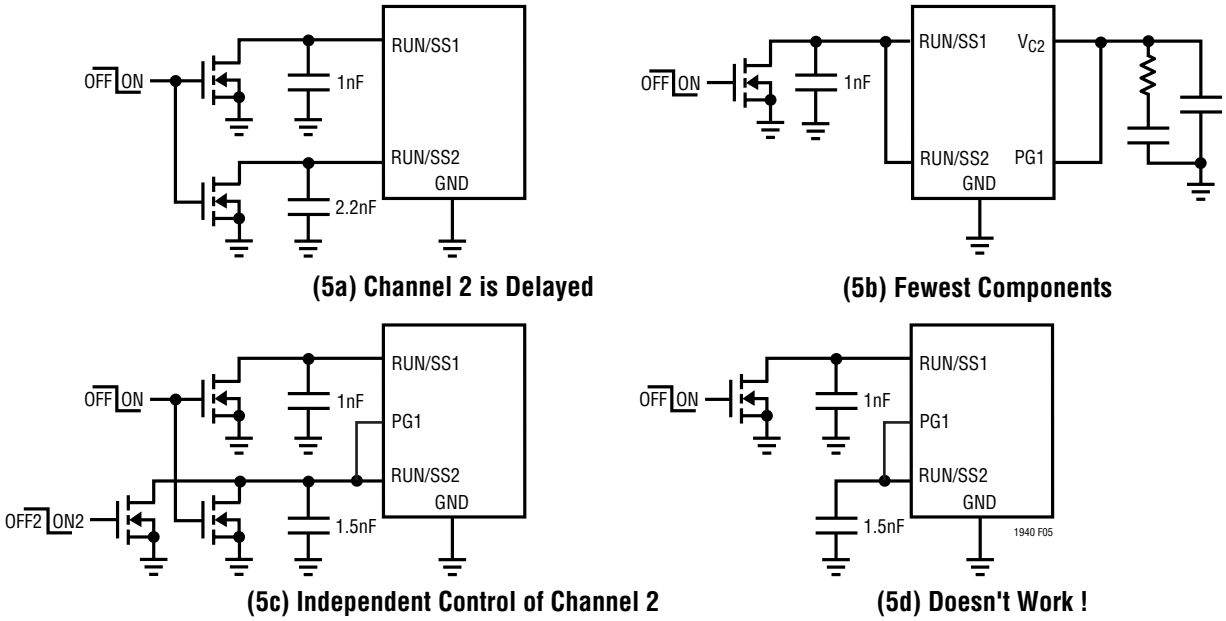


Figure 5. Several Methods of Sequencing the Two Outputs. Channel 1 Starts First.

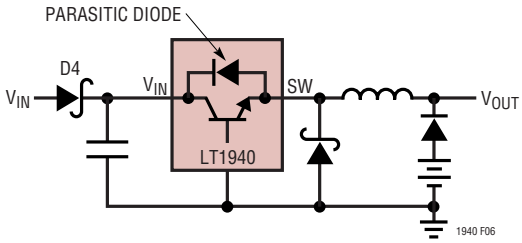


Figure 6. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output.

Shorted Input Protection

If the inductor is chosen so that it won't saturate excessively, the LT1940 will tolerate a shorted output. There is another situation to consider in systems where the output will be held high when the input to the LT1940 is absent. If the V_{IN} and one of the RUN/SS pins are allowed to float, then the LT1940's internal circuitry will pull its quiescent current through its SW pin. This is fine if your system can tolerate a few mA of load in this state. With both RUN/SS pins grounded, the LT1940 enters shutdown mode and the SW pin current drops to ~30µA. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT1940 can pull large currents from the output through the SW pin and the V_{IN} pin. A Schottky diode in series with the input to the LT1940 will protect the LT1940 and the system from a shorted or reversed input.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board (PCB) layout. Figure 7 shows the high-di/dt paths in the buck regulator circuit. Note that large, switched currents flow in the power switch, the catch diode and the input capacitor. The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components, and tie this ground plane to system ground at one location, ideally at the ground terminal of the output capacitor C2. Additionally, the SW and BOOST nodes should be kept as small as possible. Figure 8 shows recommended component placement with trace and via locations.

APPLICATIONS INFORMATION

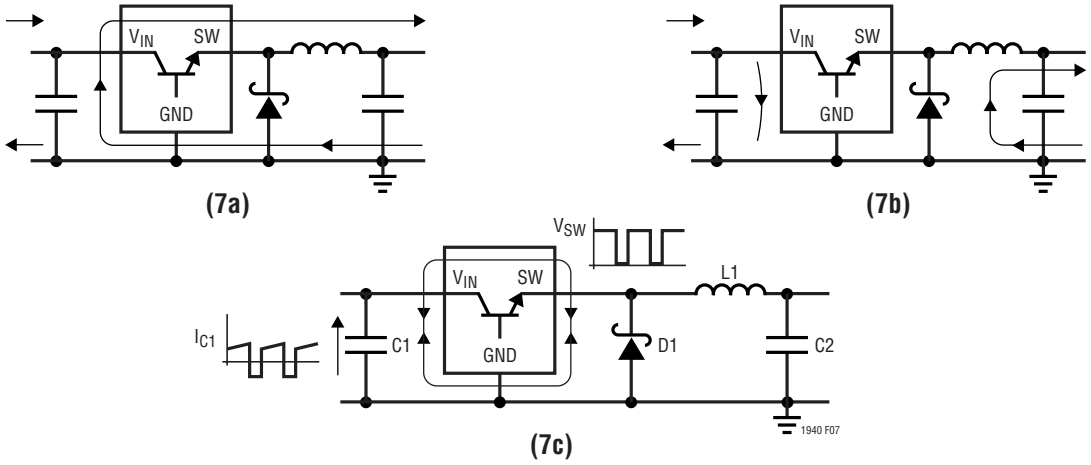


Figure 7. Subtracting the Current when the Switch is ON (a) From the Current when the Switch is OFF (b) Reveals the Path of the High Frequency Switching Current (c) Keep This Loop Small. The Voltage on the SW and BOOST Nodes will also be Switched; Keep these Nodes as Small as Possible. Finally, Make Sure the Circuit is Shielded with a Local Ground Plane.

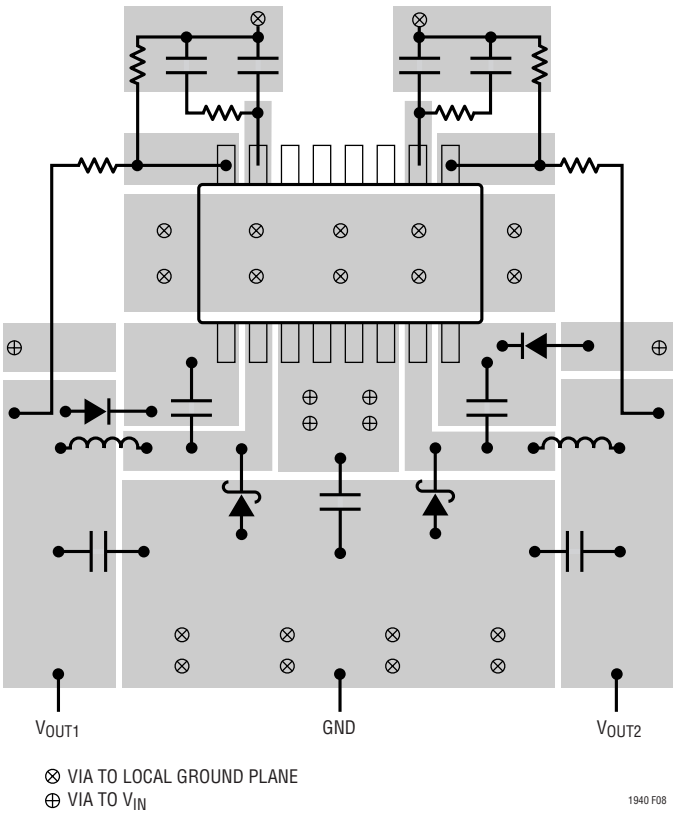


Figure 8. A Good PCB Layout Ensures Proper Low EMI Operation

Thermal Considerations

The PCB must also provide heat sinking to keep the LT1940 cool. The exposed metal on the bottom of the package must be soldered to a ground plane. This ground should be tied to other copper layers below with thermal vias; these layers will spread the heat dissipated by the LT1940. Place additional vias near the catch diodes. Adding more copper to the top and bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to θ_{JA} = 45°C/W.

The power dissipation in the other power components—catch diodes, boost diodes and inductors, cause additional copper heating and can further increase what the IC sees as ambient temperature. See the LT1767 data sheet's Thermal Considerations section.

Single, Low-Ripple 2.8A Output

The LT1940 can generate a single, low-ripple 2.8A output if the outputs of the two switching regulators are tied together and share a single output capacitor. By tying the two FB pins together and the two V_C pins together, the two channels will share the load current. There are several advantages to this two-phase buck regulator. Ripple currents at the input and output are reduced, reducing voltage ripple and allowing the use of smaller, less expensive

APPLICATIONS INFORMATION

capacitors. Although two inductors are required, each will be smaller than the inductor required for a single-phase regulator. This may be important when there are tight height restrictions on the circuit. The Typical Applications section shows circuits with maximum heights of 1.4mm, 1.8mm and 2.1mm.

There is one special consideration regarding the two-phase circuit. When the difference between the input voltage and output voltage is less than 2.5V, then the boost circuits may prevent the two channels from properly sharing current. If, for example, channel 1 gets started first, it can supply the load current, while channel 2 never switches enough current to get its boost capacitor charged. In this case, channel 1 will supply the load until it reaches current limit, the output voltage drops, and channel 2 gets started. The solution is to generate a boost supply generated from either SW pin that will service both BOOST pins. The low profile, single output 5V to 3.3V converter shown in the Typical Applications section shows how to do this.

Generating an Output Under 1.25V

The LT1940 regulates its feedback pins to 1.25V. Two resistors can be used to program an output that is higher than 1.25V. Generating an output voltage that is less than the internal reference is generally more difficult, but the LT1940 can easily generate an output voltage less than 1.25V if the other output is greater than 1.25V. Figure 9 shows how.

V_{OUT1}, which must be greater than 1.25V, is used as a reference voltage for the feedback divider from V_{OUT2} to the FB2 pin (R3 and R4). Calculate the resistor values with these equations:

$$R2/R1 = V_{OUT1}/1.25V - 1$$

$$R4/R3 = (1.25V - V_{OUT2})/(V_{OUT1} - 1.25V)$$

R5 prevents the current through R3 and R4 from pulling V_{OUT2} high when there is no load current.

$$R5 < (R3 + R4)\ V_{OUT2}/(V_{OUT1} - V_{OUT2}).$$

If V_{OUT1} is out of regulation (during start-up or if it is overloaded or shorted) then V_{OUT2} will regulate to a higher voltage than intended. To avoid this, the power good output from the channel 1 (PG1) is tied to the compensation pin (V_{C2}) of the channel 2. This disables channel 2 until V_{OUT1} is in regulation. Accuracy is good, especially when R4/R3 is small.

For example, for V_{OUT1} = 3.3V and V_{OUT2} = 1.2V, choose R1 = 10k, R2 = 16.5k, R3 = 10k, R4 = 243Ω and R5 = 4.7k.

Other Linear Technology Publications

Application notes AN19, AN35 and AN44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design note DN100 shows how to generate a dual (+ and –) output supply using a buck regulator.

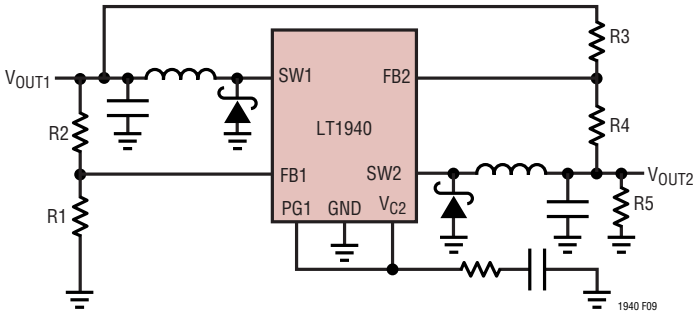
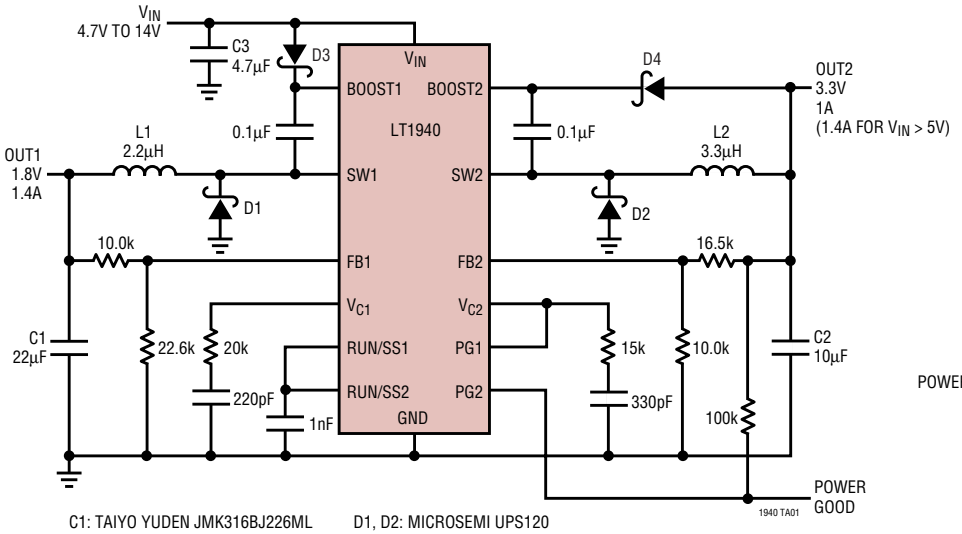


Figure 9. This circuit can be used when V_{OUT1} is greater than 1.25V and V_{OUT2} is less than 1.25V.

TYPICAL APPLICATIONS

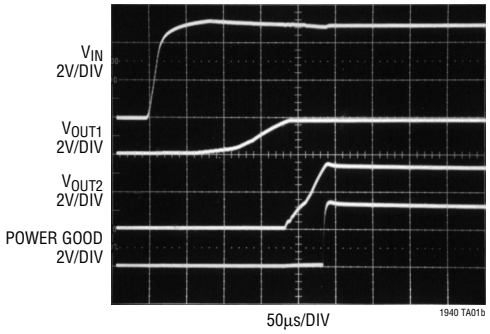
3.3V and 1.8V Outputs with Sequencing



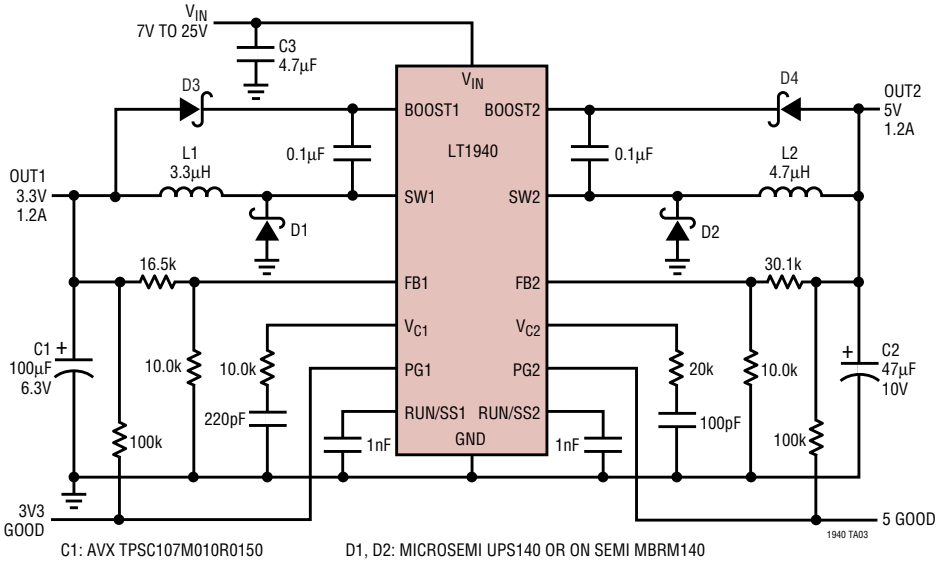
C1: TAIYO YUDEN JMK316BJ226ML
C2: TAIYO YUDEN JMK316BJ106ML
C3: TAIYO YUDEN EMK316BJ475ML

D1, D2: MICROSEMI UPS120
D3, D4: CENTRAL CMDSH-3
L1: SUMIDA CR43-2R2
L2: SUMIDA CR43-3R3

Start-Up Waveforms



5V/3.3V with Tantalum Output Capacitors

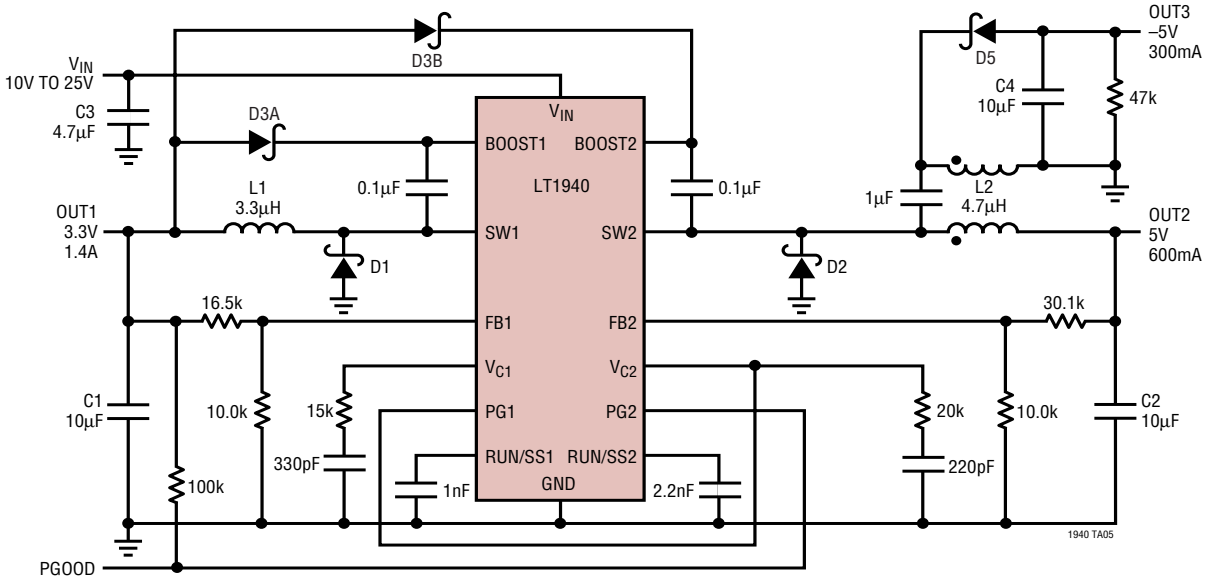


C1: AVX TPSC107M010R0150
C2: AVX TPSC476M010R0350
C3: TAIYO YUDEN TMK325BJ475ML

D1, D2: MICROSEMI UPS140 OR ON SEMI MBRM140
D3, D4: CENTRAL CMDSH-3
L1: SUMIDA CDRH4D28-3R3
L2: SUMIDA CDRH4D28-4R7

TYPICAL APPLICATIONS

3.3V, ±5V

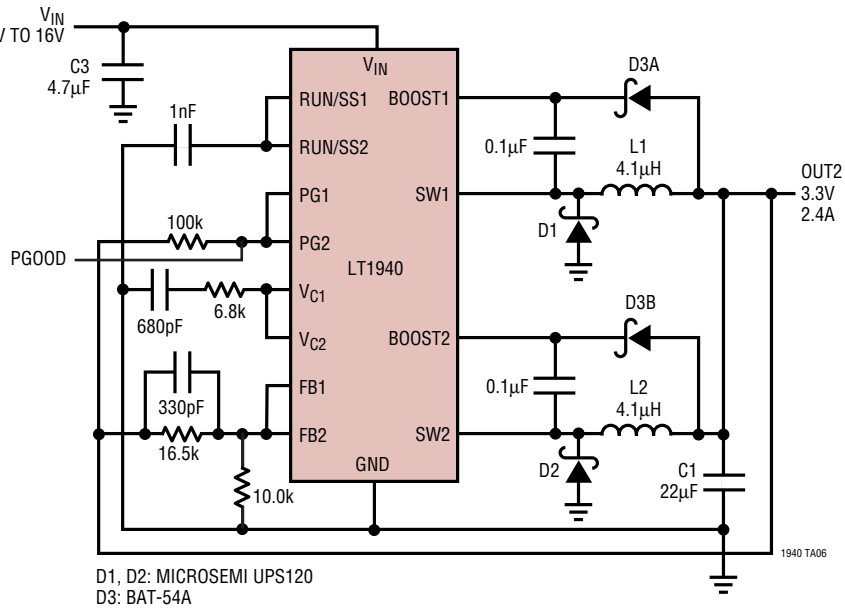


–5V LOAD SHOULD BE LESS THAN 1/2 5V LOAD (SEE DESIGN NOTE 100).

C1, C2, C4: TAIYO YUDEN JMK316BJ106ML
C3: TAIYO YUDEN TMK325BJ475ML
D1, D2: MICROSEMI UPS140 OR ON SEMI MBRM140
D3: BAT-54A

D5: ON SEMI MBR0530
L1: SUMIDA CR43-3R3
L2: COILTRONICS CTX5-1A

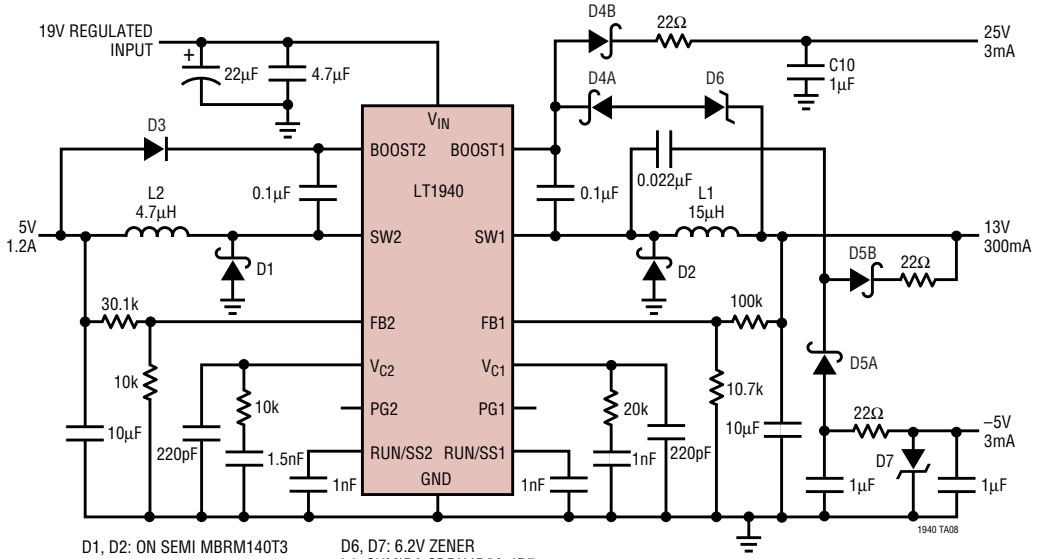
Low Ripple, Low Profile 12V to 3.3V/2.4A
Maximum Height = 2.1mm



D1, D2: MICROSEMI UPS120
D3: BAT-54A
L1, L2: SUMIDA CDRH5D18-4R1
C1: TAIYO YUDEN JMK316BJ226ML
C3: TAIYO YUDEN EMK325BJ475MN

TYPICAL APPLICATIONS

TFT LCD Supply

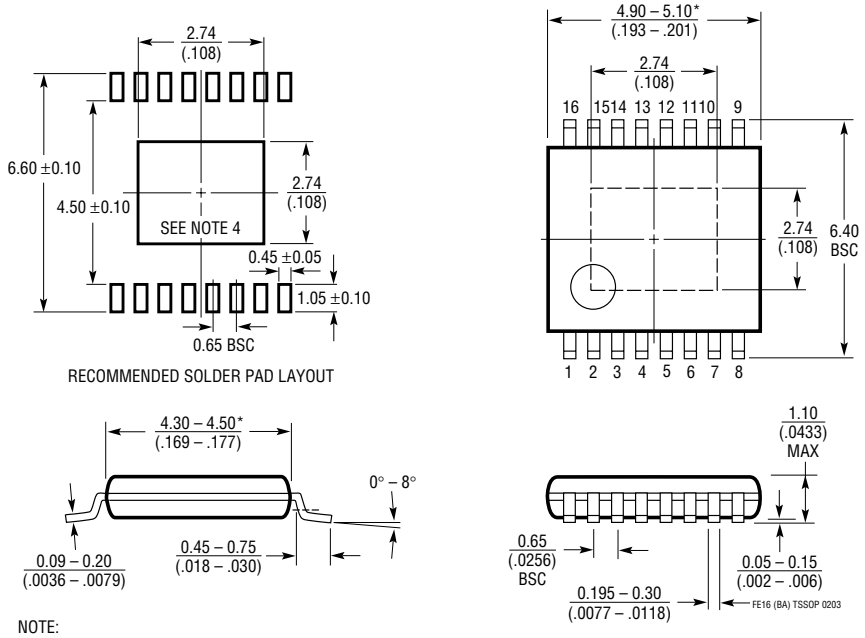


D1, D2: ON SEMI MBRM140T3
D3: CENTRAL CMPD914
D4, D5: BAT-54S

D6, D7: 6.2V ZENER
L1: SUMIDA CDRH4D28-4R7
L2: SUMIDA CDRH5D28-150

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BA

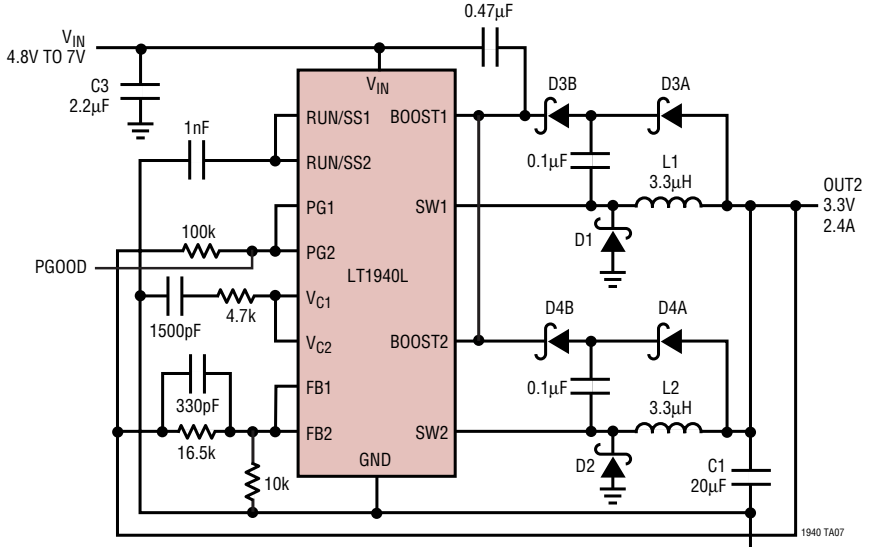


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

Low Ripple, Low Profile 5V to 3.3V/2.4A Maximum Height = 1.4mm



D1, D2: MICROSEMI UPS120
D3, D4: BAT-54S
L1, L2: COILCRAFT LPO1704-332M

C1: 2X TAIYO YUDEN JMK212BJ106ML
C3: 2X TAIYO YUDEN EMK212BJ105MN

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1765	25V, 2.75A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$: 1.20V, I_Q: 1mA, I_{SD}: 15µA S8, TSSOP16E Package
LT1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$: 1.2V, I_Q: 2.5mA, I_{SD}: 25µA TSSOP16/TSSOP16E Package
LT1767	25V, 1.2A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$: 1.2V, I_Q: 1mA, I_{SD}: 6µA MS8, MS8E Package
LT1944	Dual Output 350mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$: 34V, I_Q: 20µA, I_{SD}: <1µA, MS Package
LT1944-1	Dual Output 150mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$: 34V, I_Q: 20µA, I_{SD}: <1µA, MS Package
LT1945	Dual Output, Pos/Neg, 350mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$: ±34V, I_Q: 20µA, I_{SD}: <1µA, MS Package Package
LT1956	60V, 1.2A (I_{OUT}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$: 1.2V, I_Q: 2.5mA, I_{SD}: 25µA TSSOP16/TSSOP16E Package
LTC3407	Dual 600mA, 1.5MHz, Synchronous Step-Down Regulator	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$: 0.6V, I_Q: 40µA, MSE Package
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$: 0.8V, I_Q: 60µA, I_{SD}: <1µA MS Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$: 0.8V, I_Q: 60µA, I_{SD}: <1µA TSSOP16E Package
LT3430	60V, 2.75A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$: 1.20V, I_Q: 2.5mA, I_{SD}: 25µA TSSOP16E Package
LTC3701	Two Phase,Dual, 500kHz, Constant Frequency, Current Mode, High Efficiency Step-Down DC/DC Controller	V_{IN}: 2.5V to 10V, $V_{OUT(MIN)}$: 0.8V, I_Q: 460µA, I_{SD}: 9µA SSOP-16 Package

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