DATA SHEET

74F827
10-bit buffer/line driver, non-inverting (3-State)

74F828
10-bit buffer/line driver, inverting (3-State)

Product specification

1994 Dec 5

IC15 Data Handbook

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74F827 10-bit buffer/line driver, non-inverting (3-State)
74F828 10-bit buffer/line driver, inverting (3-State)

FEATURES

- High impedance NPN base inputs for reduced loading (20µA in High and Low states)
- I_{IL} is 20µA vs FAST family spec of 600µA and 1000µA for AMD 29827/29828 series
- Ideal where high speed, light bus loading and increased fan-in are required
- Controlled rise and fall times to minimize ground bounce
- Glitch free power-up in 3-State
- Flow through pinout architecture for microprocessor oriented applications
- Outputs sink 64mA
- 74F827 available in SSOP type II package

DESCRIPTION

The 74F827 and 74F828 10-Bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE}0$, $\overline{OE}1$) for maximum control flexibility.

The 74F827 and 74F828 are functionally and pin compatible to AMD AM29827 and AM29828. The 74F828 is an inverting version of 74F827.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F827	6.0ns	60mA
74F828	6.0ns	55mA

ORDERING INFORMATION

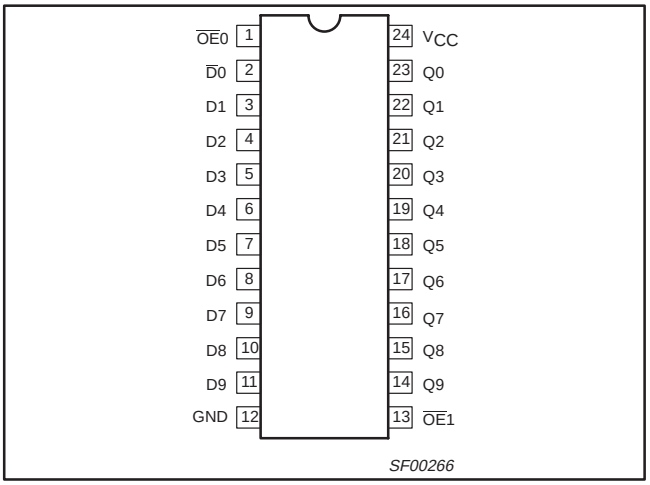
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C	DRAWING NUMBER
24-Pin Plastic DIP (300 mil)	N74F827N, N74F828N	SOT222-1
24-Pin Plastic SOL	N74F827D, N74F828D	SOT137-1
24-Pin Plastic SSOP Type II	N74F827DB	SOT340-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0-D9	Data inputs	1.0/0.033	20µA/20µA
$\overline{OE}0$-$\overline{OE}1$	Output enable inputs (active Low)	1.0/0.033	20µA/20µA
Q0-Q9	Data outputs (74F827)	1200/106.7	24mA/64mA
$\overline{Q}0$-$\overline{Q}9$	Data outputs (74F828)	1200/106.7	24mA/64mA

NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6 mA in the Low state.

PIN CONFIGURATION - 74F827



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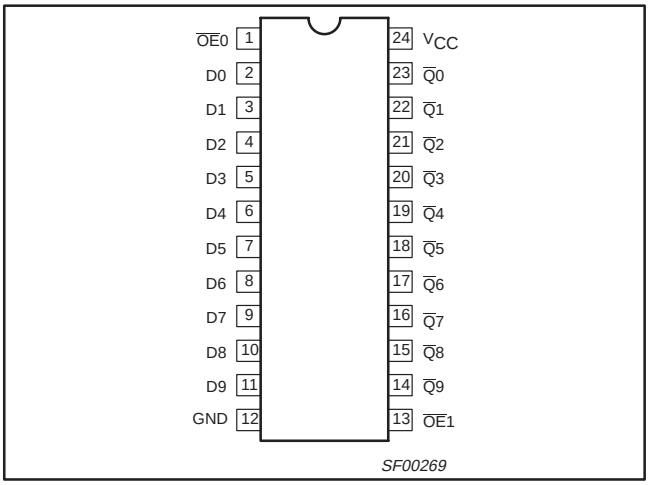
PIN CONFIGURATION - 74F828



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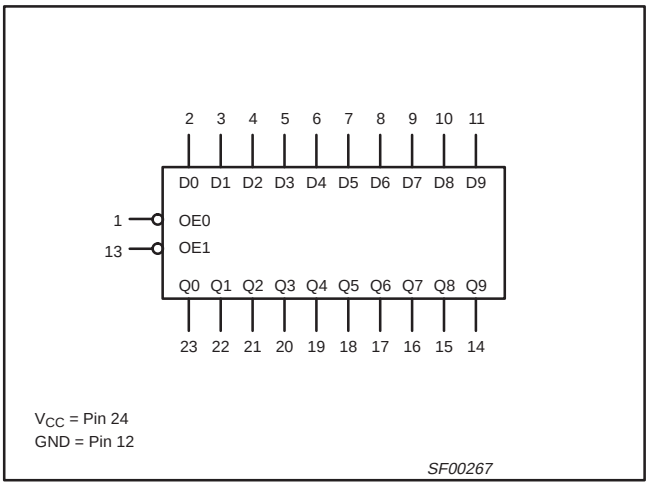
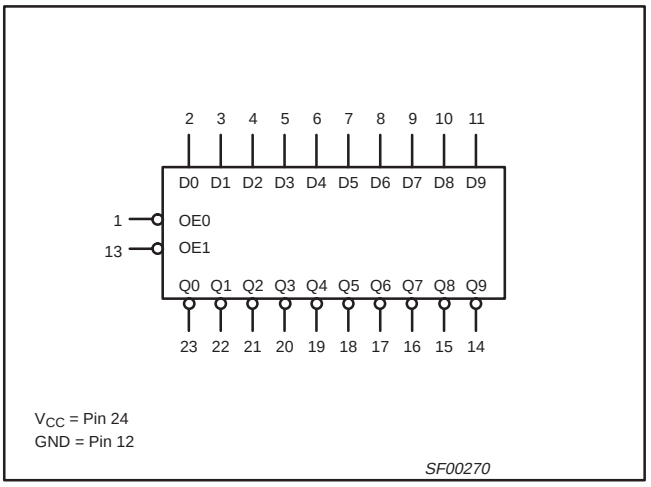
LOGIC SYMBOL - 74F827



V_{CC} = Pin 24
GND = Pin 12

SF00267

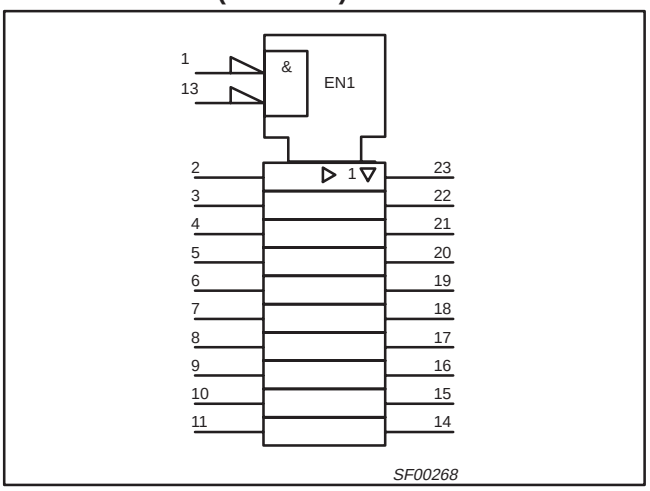
LOGIC SYMBOL - 74F828



V_{CC} = Pin 24
GND = Pin 12

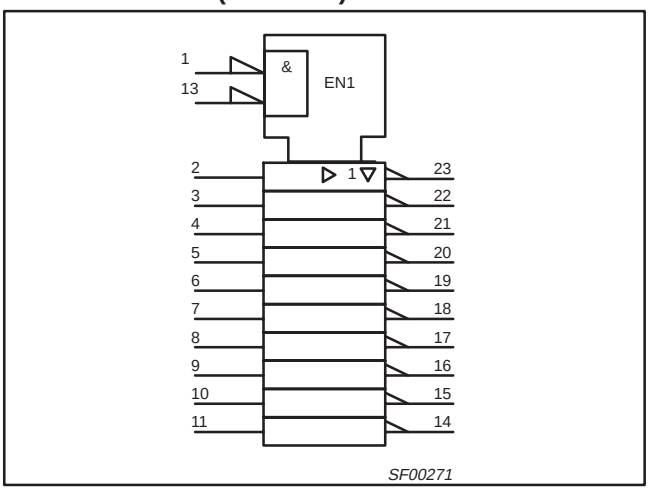
SF00270

LOGIC SYMBOL (IEEE/IEC) - 74F827



SF00268

LOGIC SYMBOL (IEEE/IEC) - 74F828



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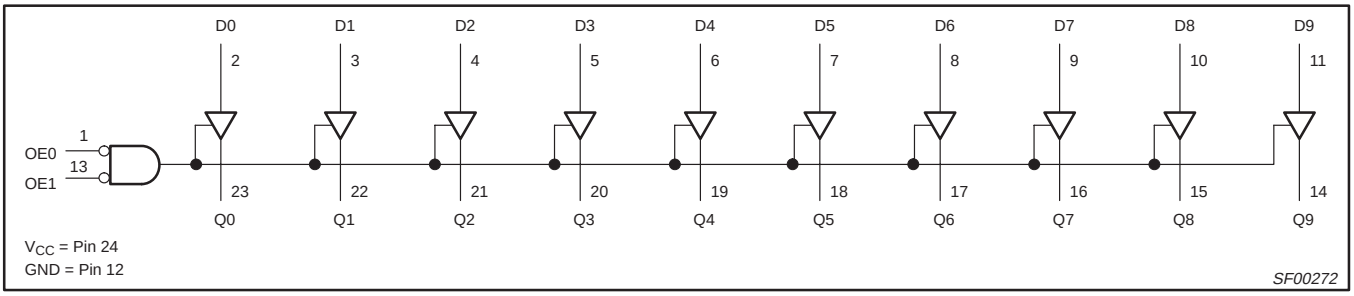
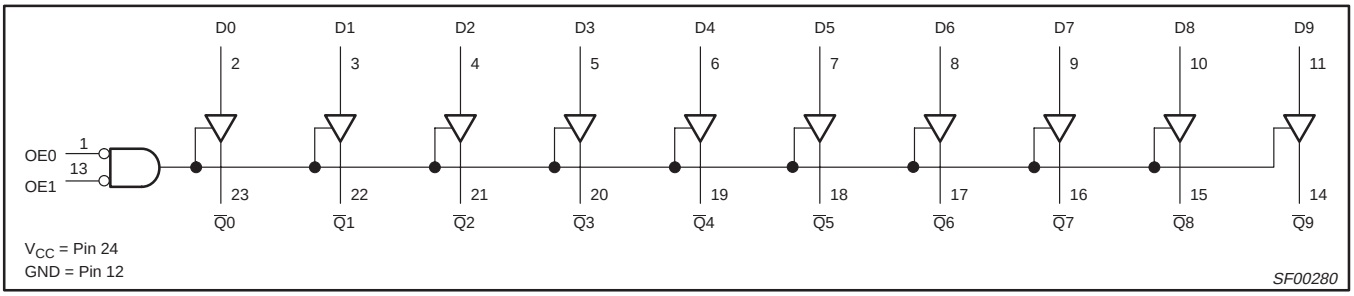
LOGIC DIAGRAM 74F827



LOGIC DIAGRAM 74F828



FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
		74F827	74F828	
$\overline{OE}n$	Dn	Qn	$\overline{Q}n$	
L	L	L	H	Transparent
L	H	H	L	Transparent
H	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to + 70	°C
T_{stg}	Storage temperature range	–65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –15mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.4	3.3		V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					–20	µA
I_{OZH}	Off-state output current, High voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low voltage applied			V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX			–100		–225	mA
I_{CC}	Supply current (total)	74F827	I_{CCH}	V_{CC} = MAX				50	70	mA
			I_{CCL}					70	100	mA
			I_{CCZ}					60	90	mA
		74F828	I_{CCH}	V_{CC} = MAX				30	45	mA
			I_{CCL}					65	85	mA
			I_{CCZ}					55	70	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at one time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC CHARACTERISTICS

SYMBOL	PARAMETER			LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_{amb} = 0 °C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1	2.0 2.0	5.5 4.5	8.5 8.5	2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	5.0 4.0	8.0 6.0	12.0 10.5	4.5 4.0	14.0 11.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2	2.0 1.0	6.0 3.0	8.5 7.0	2.0 1.0	9.5 8.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	6.0 5.0	8.0 7.0	11.5 10.5	5.5 4.5	14.0 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	2.5 1.5	5.0 4.0	8.5 7.0	2.0 1.5	9.0 8.0	ns

AC CHARACTERISTICS

for 1 Output switching with C_L = 300pF and R_L = 500Ω load

SYMBOL	PARAMETER			LIMITS					UNIT
				T_{amb} = +25°C V_{CC} = 5V C_L = 300pF R_L = 500Ω			T_{amb} = 0 °C to +70°C V_{CC} = 5V ±10% C_L = 300pF R_L = 500Ω		
				MIN	Typ	Max	MIN	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1		9.5 7.5	13.0 10.0		14.0 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 9.5	20.0 13.0		21.0 14.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 9.5	19.0 13.5		20.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2		10.0 6.0	13.0 9.0		14.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		15.5 10.5	19.0 13.0		21.0 14.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		15.0 10.0	18.0 13.0		20.0 14.5	ns

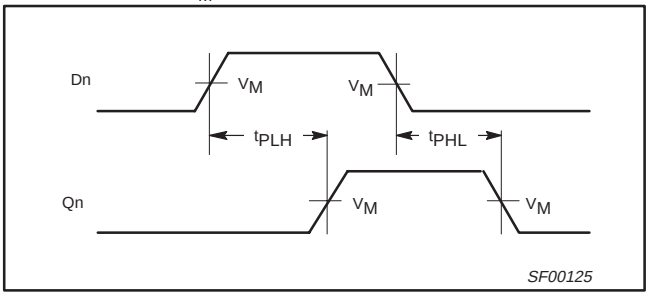
AC CHARACTERISTICS

for 10 Outputs switching with C_L = 300pF and R_L = 500Ω load

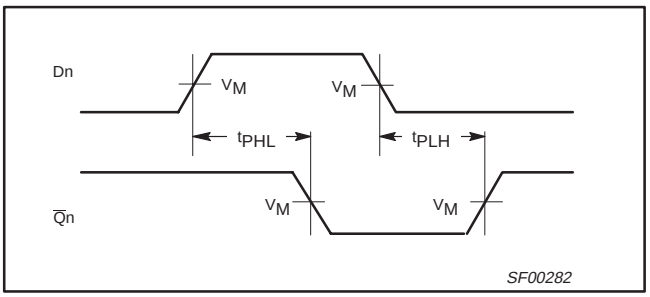
SYMBOL	PARAMETER			LIMITS					UNIT
				T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 °C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				MIN	Typ	Max	MIN	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1		12.0 14.0	16.0 17.0		17.0 18.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 17.0	20.0 21.0		21.0 21.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4		15.0 12.5	19.0 15.5		20.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2		10.0 10.0	17.0 13.5		18.0 14.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		18.0 15.0	21.0 18.0		23.0 19.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4		16.5 11.5	19.5 14.5		22.5 15.0	ns

AC WAVEFORMS

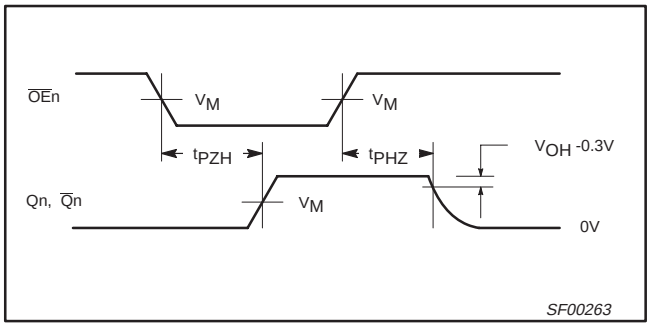
For all waveforms, V_M = 1.5V



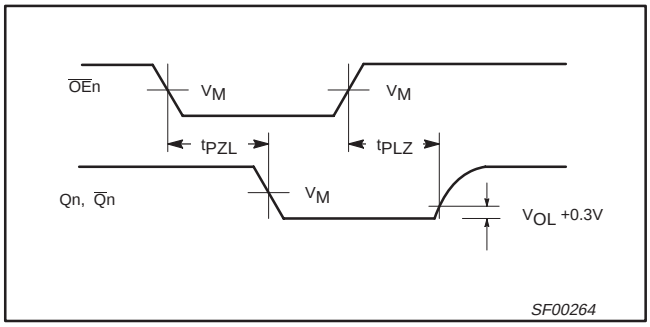
Waveform 1. Propagation Delay for Non-Inverting Output



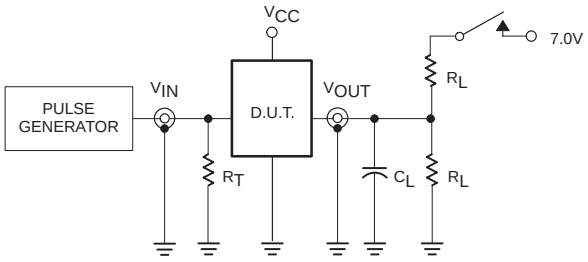
Waveform 2. Propagation Delay for Inverting Output



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Test Circuit for Open Collector Outputs

SWITCH POSITION

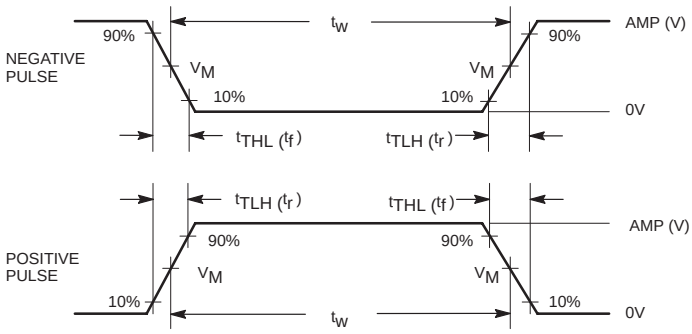
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

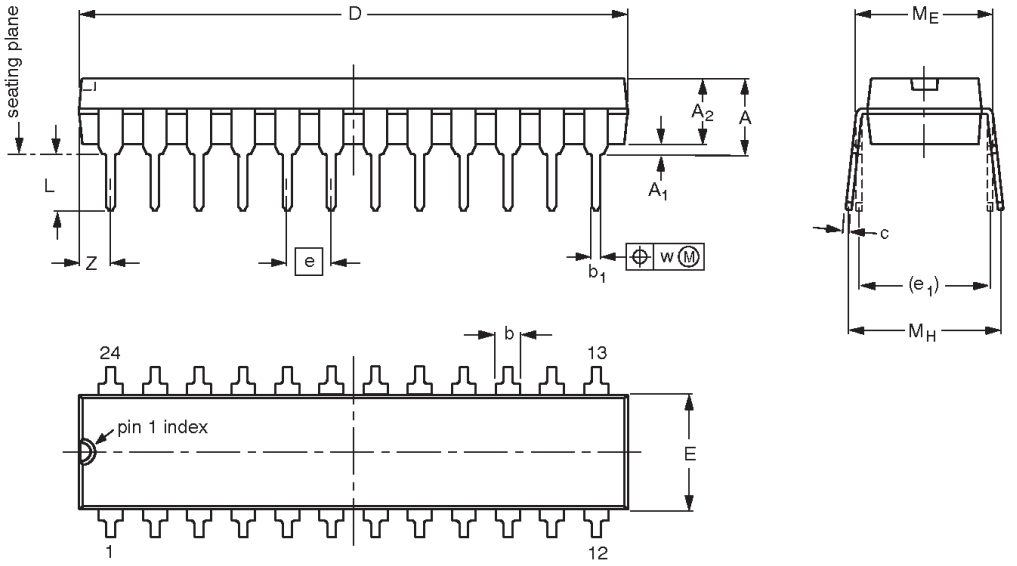


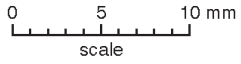
Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

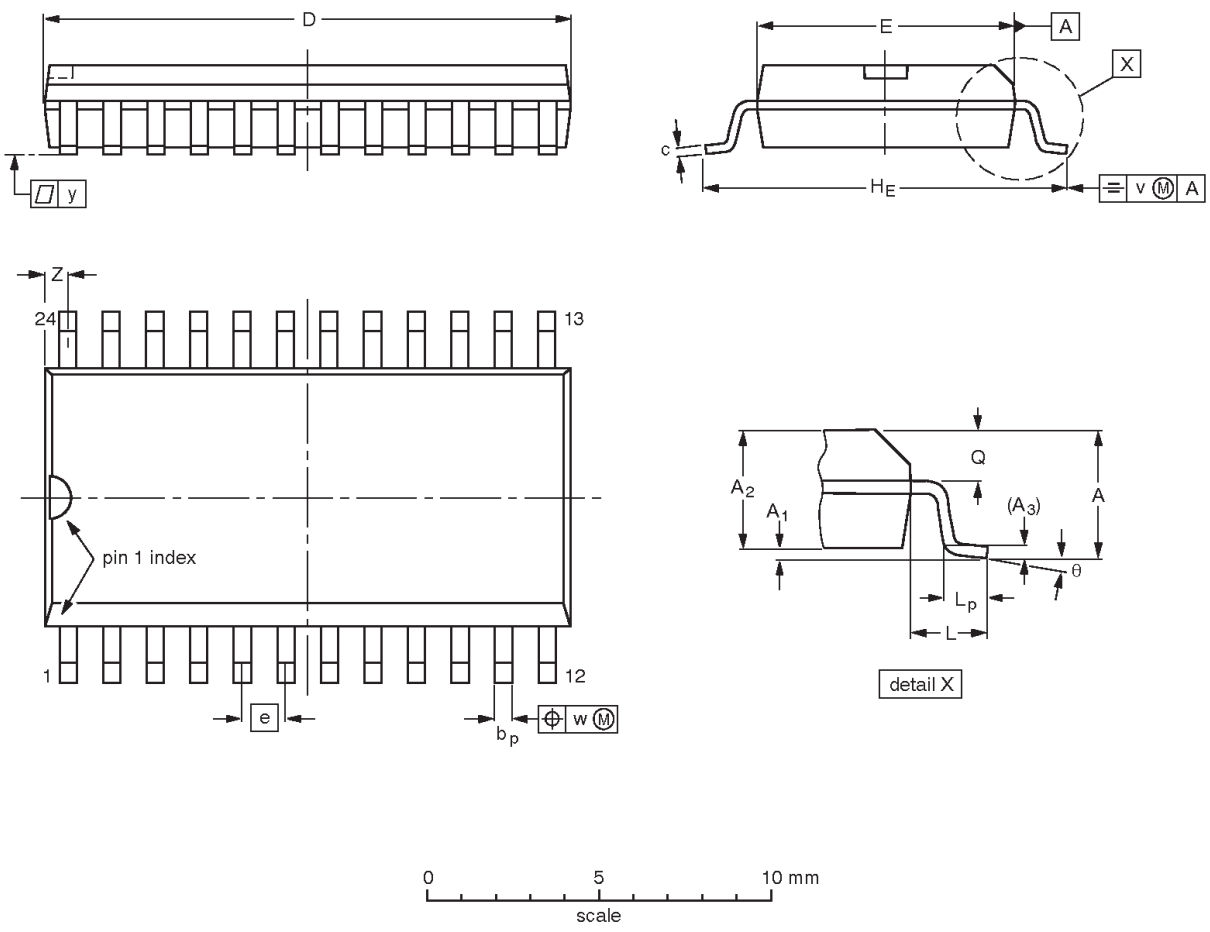
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

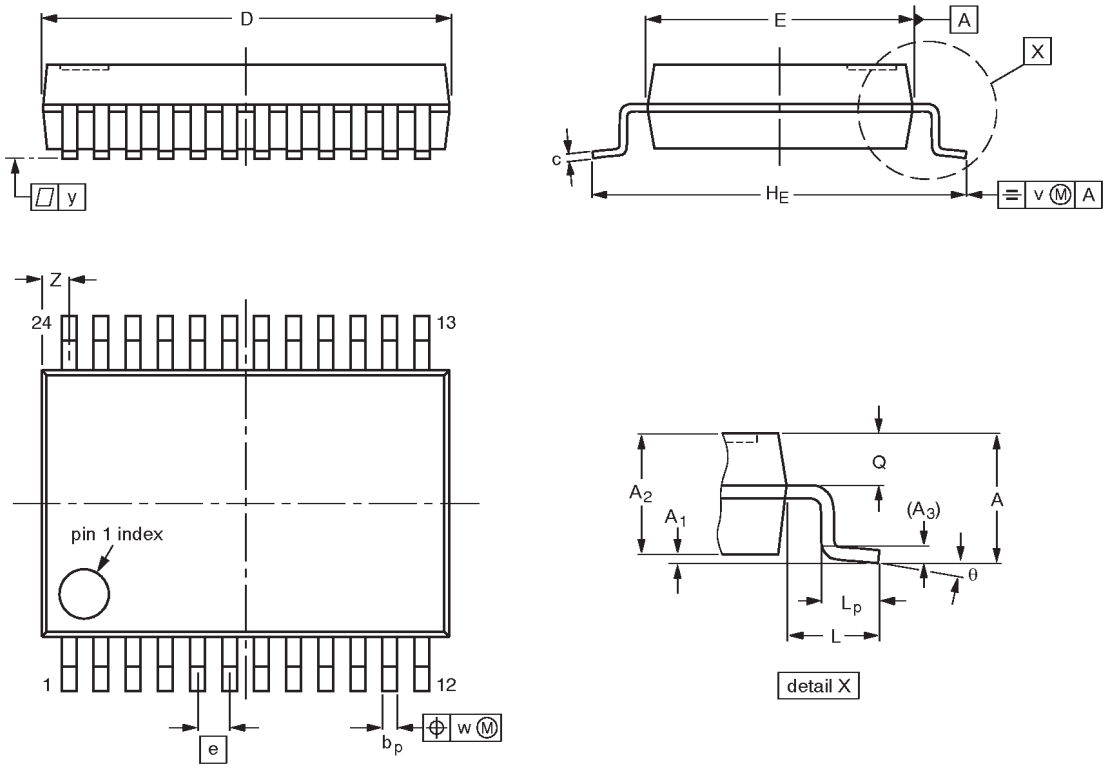
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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