

# M62363FP

## 8-bit 8ch D/A Converter

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### Description

The M62363FP is an integrated circuit semiconductor of CMOS structured with 8 channels of built-in 8-bit multiplication type D/A converters.

The input data is a easy-to-use 3-wire serial method and it is able to cascading serial use with  $D_O$  terminal.

The device is suited for use in automatic adjustment combination of microcomputer.

### Features

- Digital data transfer method: 3-wire serial data transfer method
- D/A converter system  
Employment of the additional higher-order segment R-2R method doubled precision compared to the conventional R-2R method.
- Short setting time
- 4 quadrant multiplication

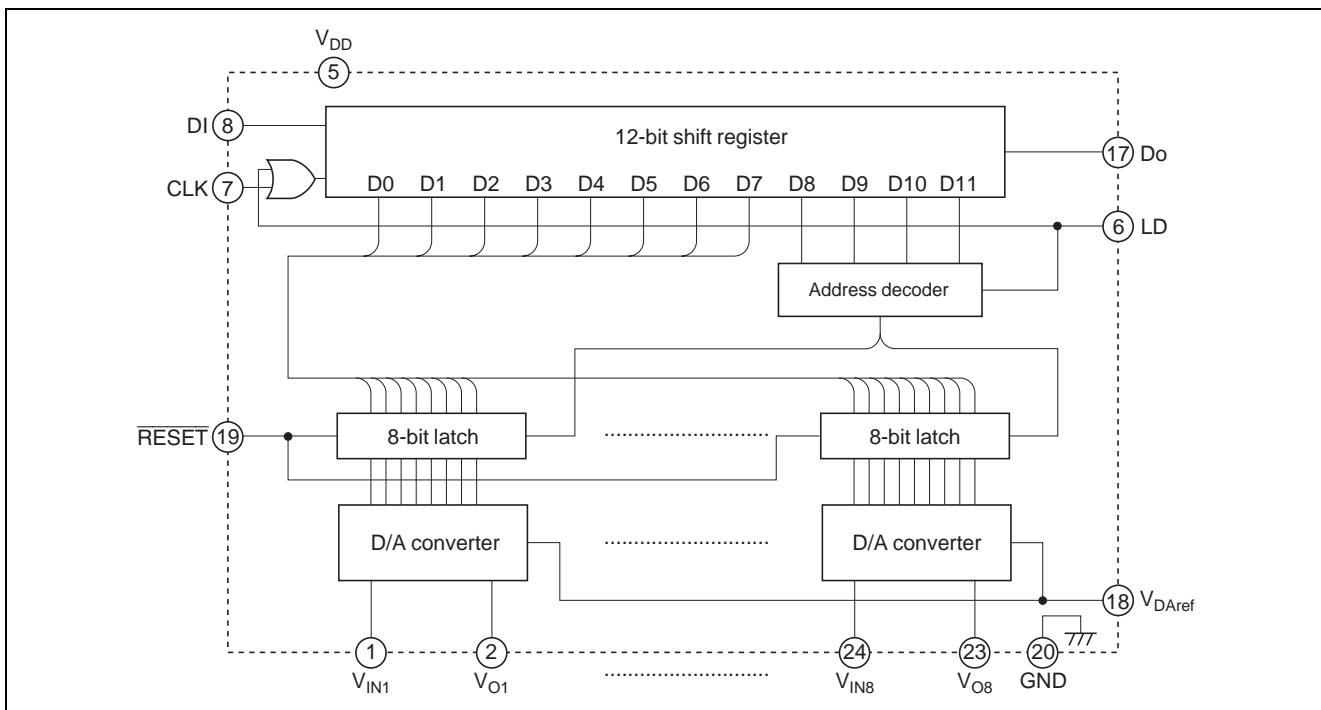
### Application

Conversion from digital control data to analog control data for home-use and industrial equipment.

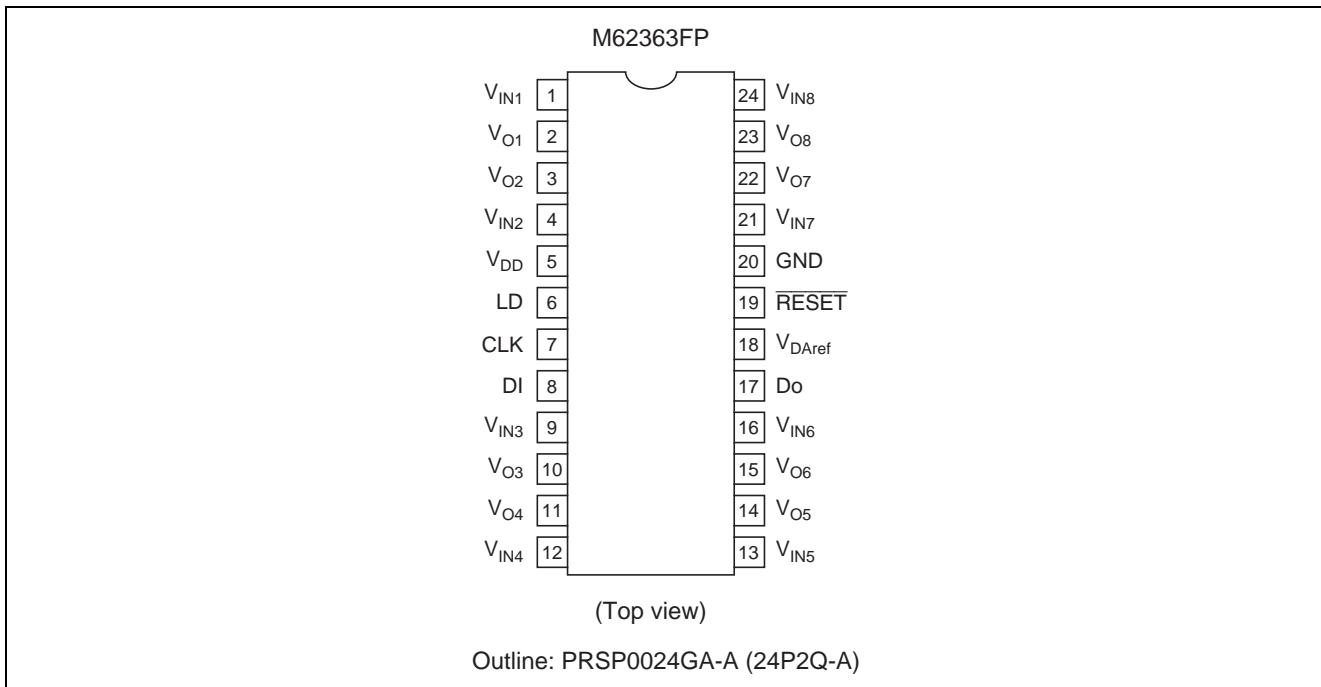
Automatic adjustment by combination with EEPROM and microcomputer. (Replacement of conventional half-fixed resistor.)

Signal gain control of display-monitor or CTV

### Block Diagram



## Pin Arrangement



## Pin Description

Pin No.	Pin Name	Function
8	DI	Serial data input terminal
17	Do	Serial data output terminal
7	CLK	Serial clock input terminal
6	LD	LD terminal input high level then latch circuit data load
19	RESET	Reset terminal
2	V_O1	8-bit resolution D/A output
3	V_O2	
10	V_O3	
11	V_O4	
14	V_O5	
15	V_O6	
22	V_O7	
23	V_O8	
5	V_DD	Power supply terminal
20	GND	GND terminal
1	V_IN1	D/A converter input terminal
4	V_IN2	
9	V_IN3	
12	V_IN4	
13	V_IN5	
16	V_IN6	
21	V_IN7	
24	V_IN8	
18	V_DAref	D/A converter reference voltage input terminal $V_O = (V_{IN} - V_{DAref}) \times n / 256 + V_{DAref}$

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{DD}$	−0.3 to +7.0	V
Input voltage	$V_{IND}$	−0.3 to +7.0	V
Input voltage	$V_{IN}$	−0.3 to $V_{DD} + 0.3$	V
Output voltage	$V_O$	−0.3 to $V_{DD} + 0.3$	V
D/A reference voltage	$V_{DAref}$	−0.3 to $V_{DD} + 0.3$	V
Operating temperature	$T_{opr}$	−20 to +75	°C
Storage temperature	$T_{stg}$	−40 to +125	°C

## Electrical Characteristics

### <Digital Part>

( $V_{DD}$ ,  $V_{IN} = +5 \text{ V} \pm 10\%$ ,  $V_{DD} \geq V_{IN}$ , GND =  $V_{DAref} = 0 \text{ V}$ ,  $T_a = -20$  to  $+75^\circ\text{C}$ , unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	$V_{DD}$	4.5	5.0	5.5	V	
Input leak current	$I_{ILK}$	−10	—	10	$\mu\text{A}$	$V_{IN} = 0$ to $V_{DD}$
Input low voltage	$V_{IL}$	—	—	0.2 $V_{DD}$	V	
Input high voltage	$V_{IH}$	0.8 $V_{DD}$	—	—	V	
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.5 \text{ mA}$
Output high voltage	$V_{OH}$	$V_{DD} - 0.4$	—	—	V	$I_{OH} = -400 \mu\text{A}$

### <Analog Part>

( $V_{DD}$ ,  $V_{IN} = +5 \text{ V} \pm 10\%$ ,  $V_{DD} \geq V_{IN}$ , GND =  $V_{DAref} = 0 \text{ V}$ ,  $T_a = -20$  to  $+75^\circ\text{C}$ , unless otherwise noted.)

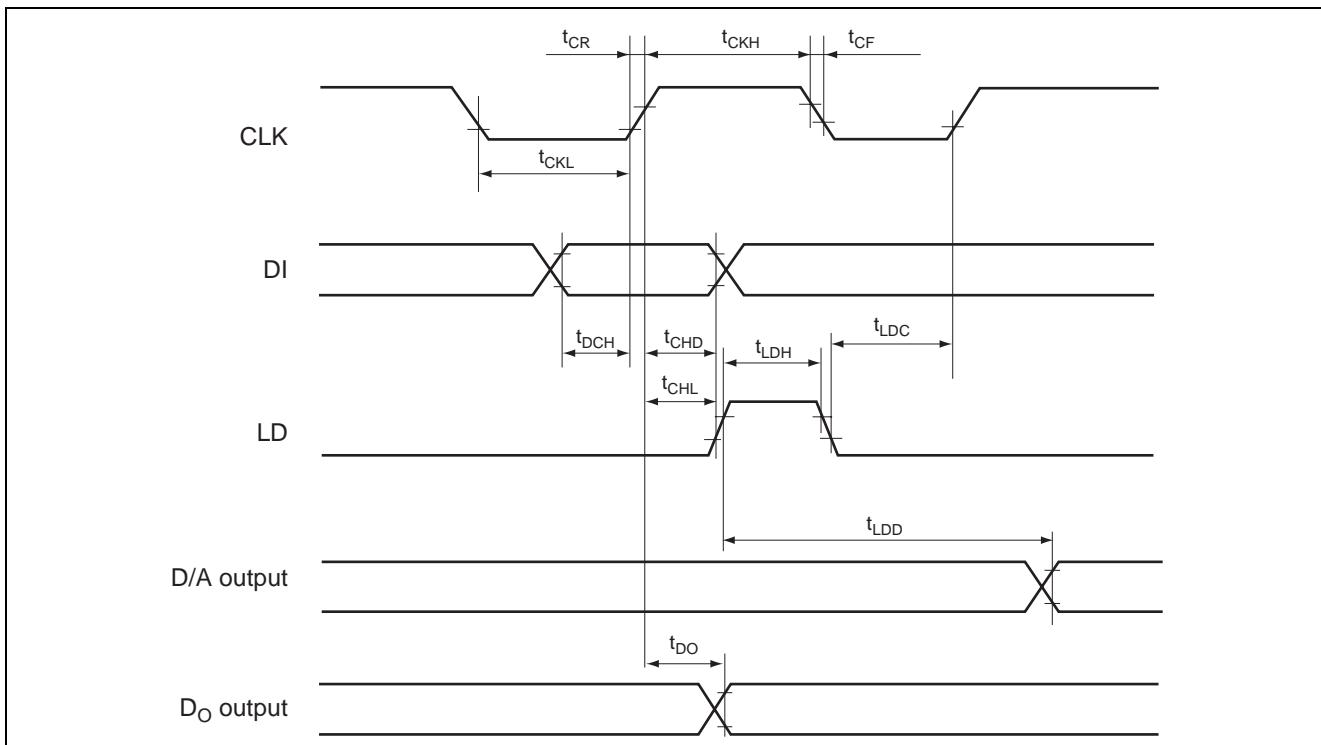
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input current	$I_{IN}$	—	—	0.30	mA	$V_{IN} = 5 \text{ V}$ , $V_{DAref} = 0 \text{ V}$ Proportional to Max. input current condition ( $V_{IN} - V_{DAref}$ ) and digital data of each channels
D/A reference input current	$I_{DAref}$	−2.40	—	—	mA	$V_{IN1}$ to $V_{IN8} = 5 \text{ V}$ , $V_{DAref} = 0 \text{ V}$ Proportional to Max. input current condition ( $V_{IN} - V_{DAref}$ ) and digital data of each channels
Output impedance	$R_O$	—	—	50	$\text{k}\Omega$	Constant for all D/A output mode
Resolution	RES	—	8	—	bit	
Differential nonlinearity	DNL	−1	—	1	LSB	
Nonlinearity	NL	−1	—	1	LSB	

## AC Characteristics

(V<sub>DD</sub>, V<sub>IN</sub> = +5 V ± 10%, V<sub>DD</sub> ≥ V<sub>IN</sub>, GND = V<sub>DAref</sub> = 0 V, Ta = -20 to +75°C, unless otherwise noted.)

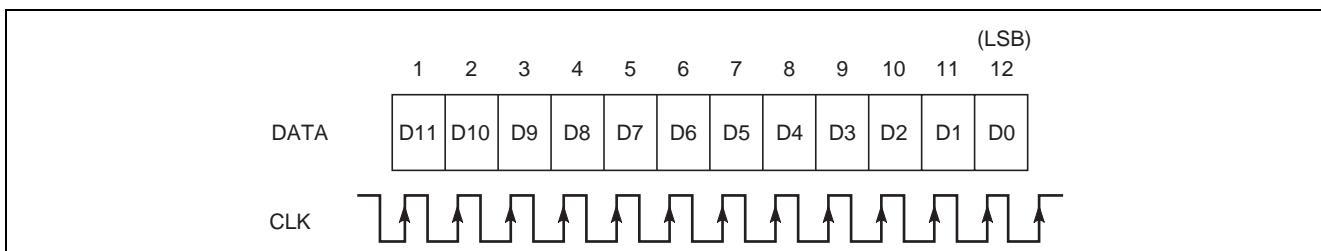
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	t <sub>CKL</sub>	200	—	—	ns	
Clock "H" pulse width	t <sub>CKH</sub>	200	—	—	ns	
Clock rise time	t <sub>CR</sub>	—	—	200	ns	
Clock fall time	t <sub>CF</sub>	—	—	200	ns	
Data setup time	t <sub>DCH</sub>	60	—	—	ns	
Data hold time	t <sub>CHD</sub>	100	—	—	ns	
LD setup time	t <sub>CHL</sub>	200	—	—	ns	
LD hold time	t <sub>LDC</sub>	100	—	—	ns	
LD "H" pulse width	t <sub>LDH</sub>	100	—	—	ns	
Data output delay time	t <sub>DO</sub>	70	—	350	ns	Less than C <sub>L</sub> = 100 pF
D/A output setting time	t <sub>LDD</sub>	—	—	5	μs	Without load
Input/output replay time	—	—	—	5	μs	f = 10 kHz

## Timing Chart



## Digital Data Format

### 12-bit serial data



### Data assignment

D0	D1	D2	D3	D4	D5	D6	D7	: DAC data				
(LSB)								(MSB)				
	D8	D9	D10	D11	: DAC select data							

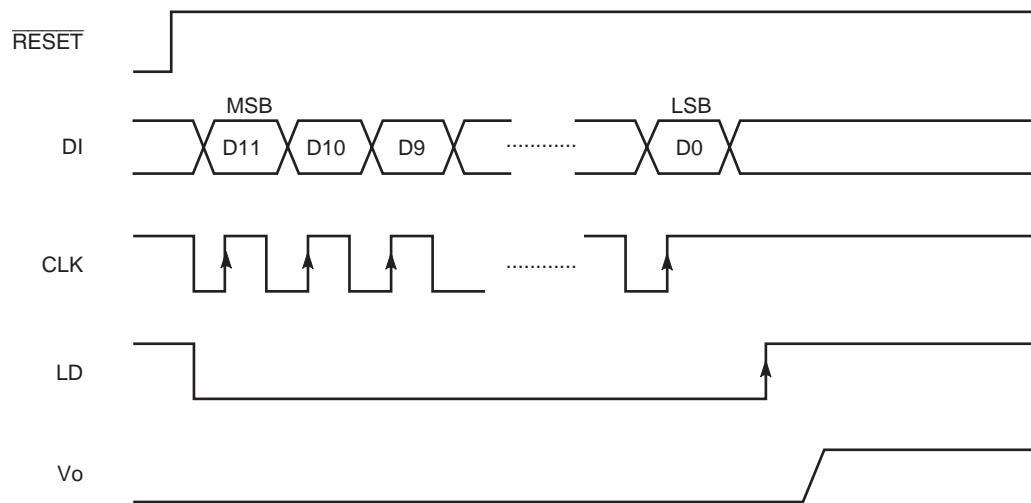
### DAC Data

(LSB)								(MSB)				
D0	D1	D2	D3	D4	D5	D6	D7	D/A Output				
0	0	0	0	0	0	0	0					$V_{D\text{Aref}}$
1	0	0	0	0	0	0	0					$(V_{IN} - V_{D\text{Aref}}) / 256 \times 1 + V_{D\text{Aref}}$
0	1	0	0	0	0	0	0					$(V_{IN} - V_{D\text{Aref}}) / 256 \times 2 + V_{D\text{Aref}}$
1	1	0	0	0	0	0	0					$(V_{IN} - V_{D\text{Aref}}) / 256 \times 3 + V_{D\text{Aref}}$
:	:	:	:	:	:	:	:					:
1	1	1	1	1	1	1	1					$(V_{IN} - V_{D\text{Aref}}) / 256 \times 255 + V_{D\text{Aref}}$

### DAC Select Data

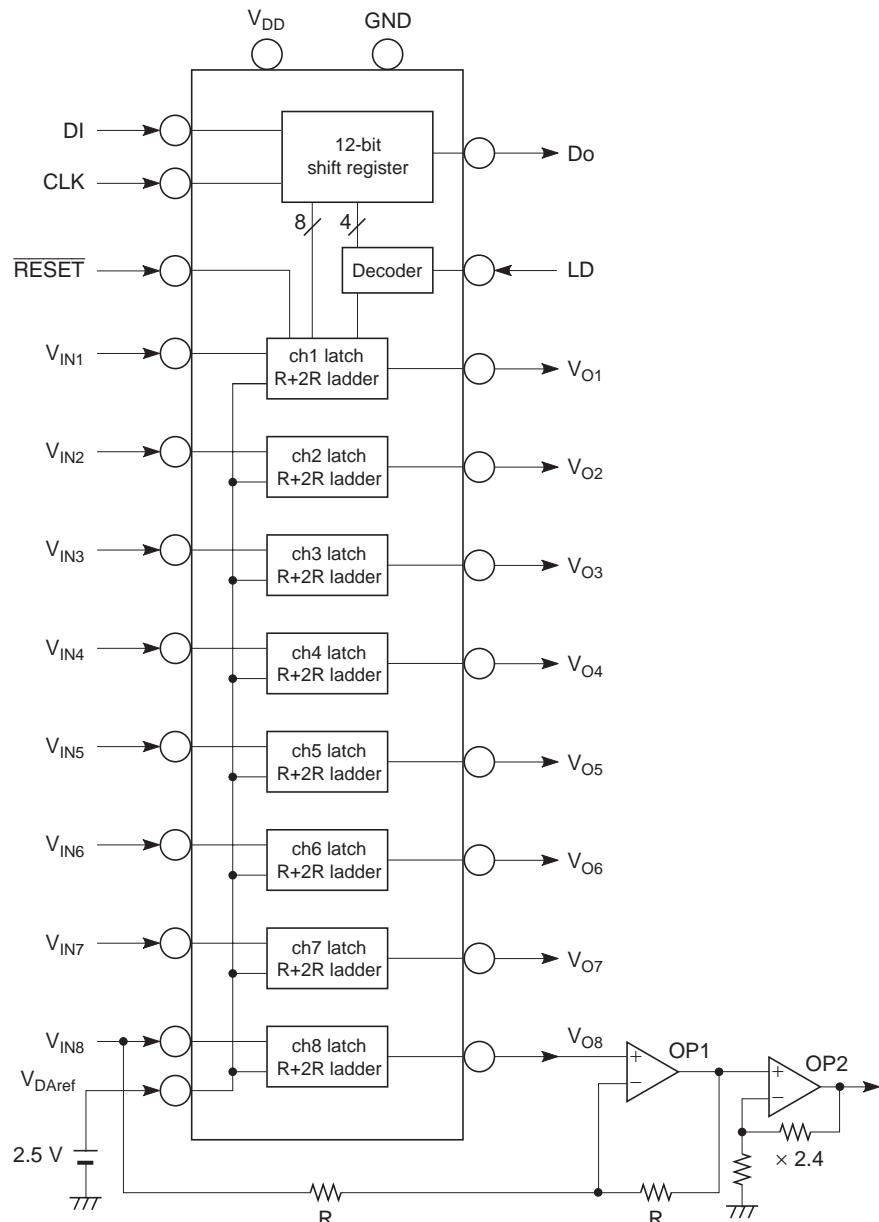
D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	$V_{O1}$ selection
0	0	1	0	$V_{O2}$ selection
0	0	1	1	$V_{O3}$ selection
0	1	0	0	$V_{O4}$ selection
0	1	0	1	$V_{O5}$ selection
0	1	1	0	$V_{O6}$ selection
0	1	1	1	$V_{O7}$ selection
1	0	0	0	$V_{O8}$ selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

## Timing Chart (Model)



Note: Input data is carried out LD signal low besides CLK signal positive edge. CLK, LD, is keep generally high level.

## Operating Description



Note: ch1 to ch7 becomes multiplication type D/A converter action of 0 to 5 V range by each output adds OP1.

ch8 become 4 quadrant multiplication of 0 to 12 V range at 6 V center by add OP1 and OP2 to this channel.

1. The value of  $V_o$  depend on output direct buffer.

$$V_O = (V_{IN} - V_{DAref}) \cdot \frac{n}{256} + V_{DAref} \dots (n = 0 \text{ to } 255) \dots (1)$$

$<V_{IN} = 5 V>$	
<b>n</b>	<b>V<sub>O</sub></b>
0	0
128	3.75
255	4.99

$<V_{IN} = 0 V>$	
<b>n</b>	<b>V<sub>O</sub></b>
0	2.5
128	1.25
255	0.01

2. The value of  $V_o$  depend on application of ch8.

$$V_{OP1} = (V_{IN} - V_{DAref}) \bullet \left( \frac{n}{128} - 1 \right) + V_{DAref} \dots (n = 0 \text{ to } 255) \dots (2)$$

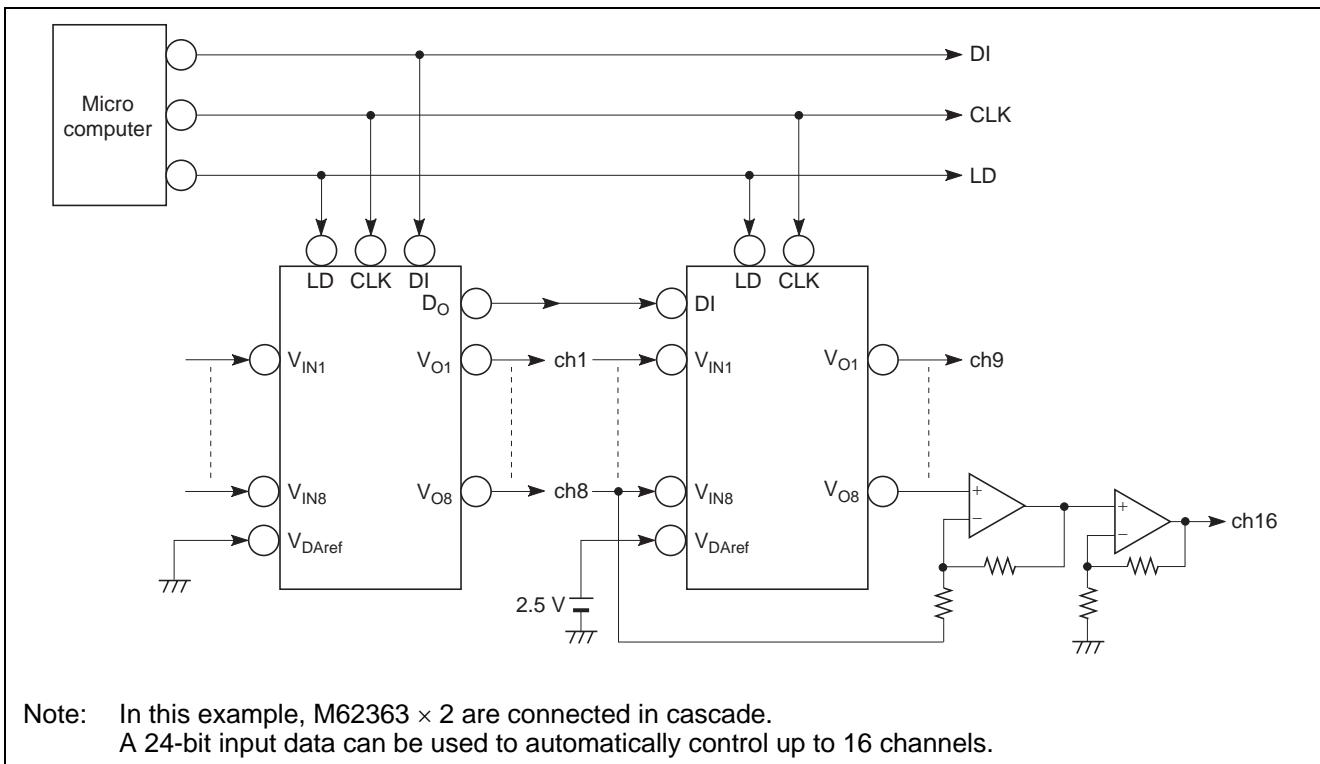
$<V_{IN} = 5 V>$	
<b>n</b>	<b>V<sub>OP1</sub></b>
0	0
128	2.50
255	4.98

$\langle V_{IN} = 0 \rangle V$	
<b>n</b>	<b>V<sub>OP1</sub></b>
0	5.00
128	2.50
255	0.02

<b>n</b>	<b>V<sub>OP1</sub></b>
0	0
128	6.00
255	11.95

<b>n</b>	<b>V<sub>OP1</sub></b>
0	12.00
128	6.00
255	0.05

## Application Example of Cascade Connection



## Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP24-5.3x10.1-0.80	PRSP0024GA-A	24P2Q-A	0.2g

**NOTE)**

1. DIMENSIONS \*\*1\*\* AND \*\*2\*\* DO NOT INCLUDE MOLD FLASH.
2. DIMENSION \*\*3\*\* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	10.0	10.1	10.2
E	5.2	5.3	5.4
A <sub>2</sub>	—	1.8	—
A	—	—	2.1
A <sub>1</sub>	0	0.1	0.2
b <sub>p</sub>	0.3	0.35	0.45
c	0.18	0.2	0.25
θ	0°	—	8°
H <sub>E</sub>	7.5	7.8	8.1
e	0.65	0.8	0.95
y	—	—	0.10
L	0.4	0.6	0.8

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