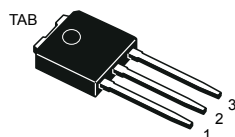
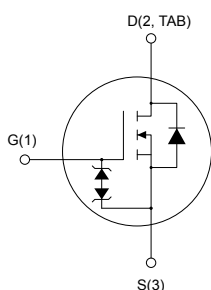


N-channel 900 V, 4.7 Ω typ., 2.1 A SuperMESH Power MOSFET in an IPAK package



IPAK



AM01476v1_tab



Product status link

[STD2NK90Z-1](#)

Product summary

Order code	STD2NK90Z-1
Marking	D2NK90Z
Package	IPAK
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD2NK90Z-1	900 V	6.5 Ω	2.1 A

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	900	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	2.1	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	1.3	
$I_{DM}^{(1)}$	Drain current (pulsed)	8.4	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	70	W
ESD	Gate-source, human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	2	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 2.1\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\%V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.78	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	100	$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	2.1	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	150	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	900			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 900\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 900\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			50	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.05\text{ A}$		4.7	6.5	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	485		pF
C_{oss}	Output capacitance		-	50		pF
C_{rss}	Reverse transfer capacitance		-	10		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V to } 720\text{ V}$	-	24		pF
Q_g	Total gate charge	$V_{DD} = 720\text{ V}$, $I_D = 2\text{ A}$, $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	19.5	27 ⁽²⁾	nC
Q_{gs}	Gate-source charge		-	3.4		nC
Q_{gd}	Gate-drain charge		-	10.8		nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450\text{ V}$, $I_D = 1\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	21	-	ns
t_r	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	43	-	ns
t_f	Fall time		-	40	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.1	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		8.4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.1 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 50 \text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	415		ns
Q_{rr}	Reverse recovery charge		-	1.5		μC
I_{RRM}	Reverse recovery current		-	7.2		A
t_{rr}	Reverse recovery time	$I_{SD} = 2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 50 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	515		ns
Q_{rr}	Reverse recovery charge		-	1.9		μC
I_{RRM}	Reverse recovery current		-	7.5		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2. Pulse width is limited by safe operating area.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

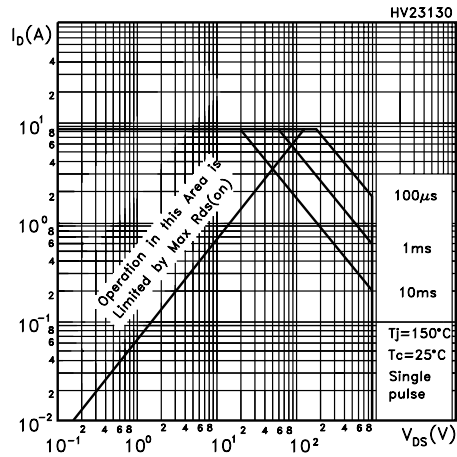


Figure 2. Thermal impedance

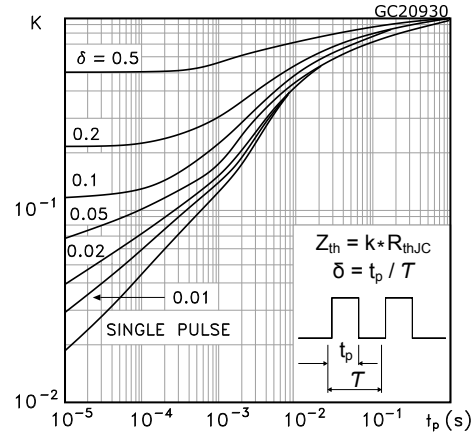


Figure 3. Output characteristics

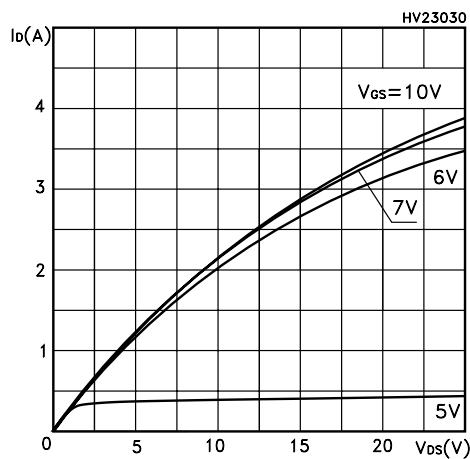


Figure 4. Transfer characteristics

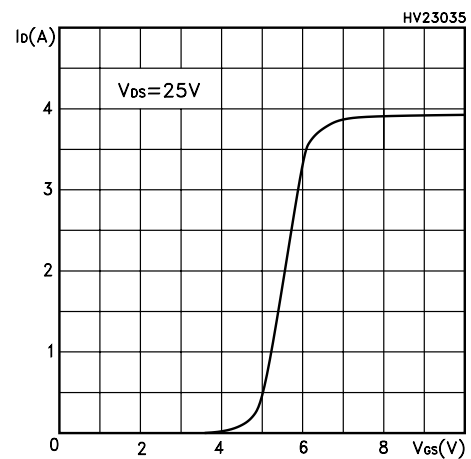


Figure 5. Static drain-source on resistance

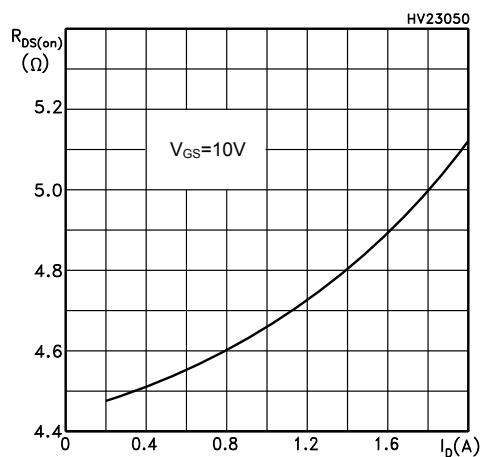


Figure 6. Gate charge vs gate-source voltage

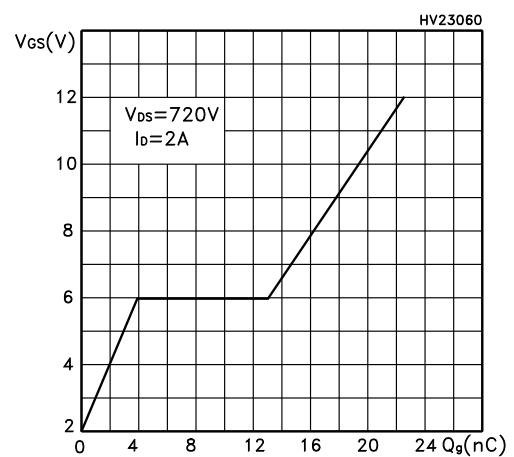


Figure 7. Capacitance variations

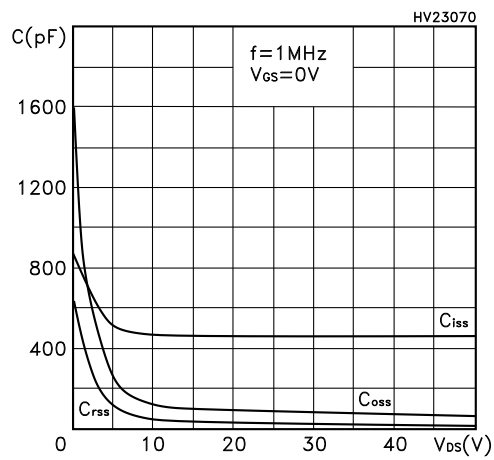


Figure 8. Normalized gate threshold voltage vs temperature

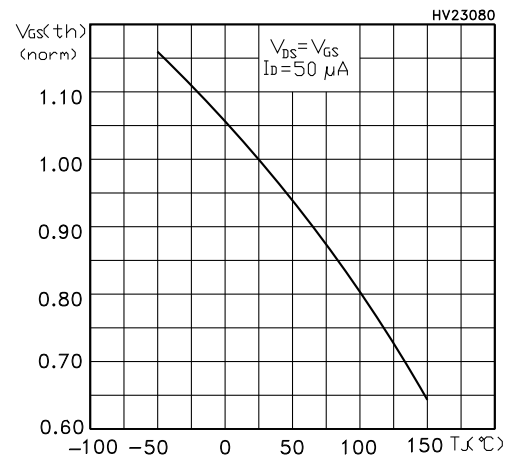


Figure 9. Normalized on resistance vs temperature

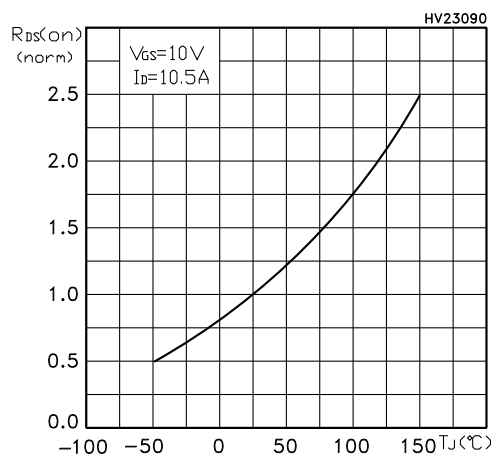


Figure 10. Source-drain diode forward characteristics

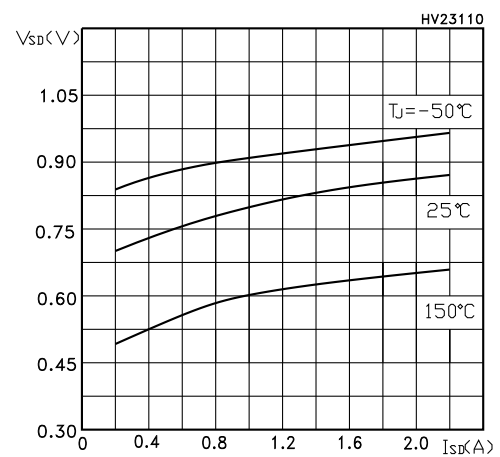


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

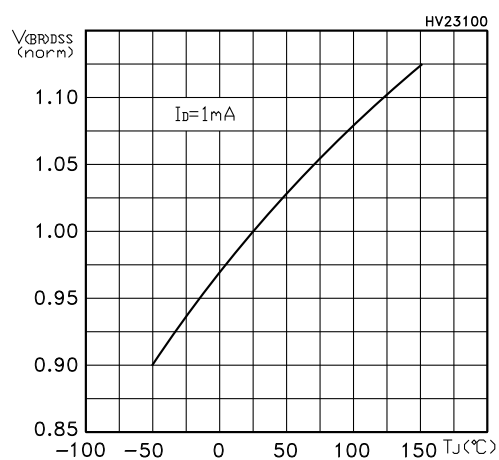
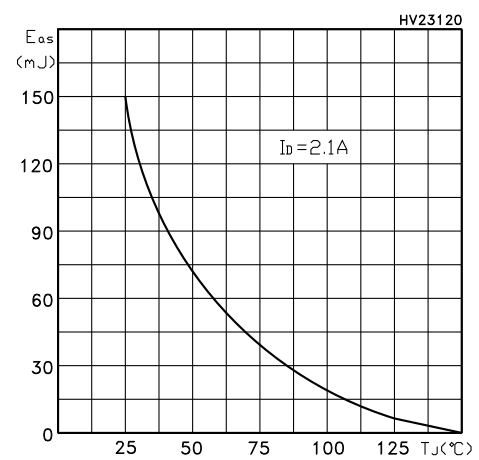


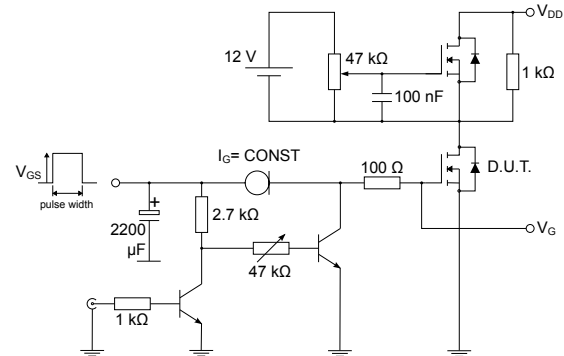
Figure 12. Maximum avalanche energy vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times


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Figure 14. Test circuit for gate charge behavior


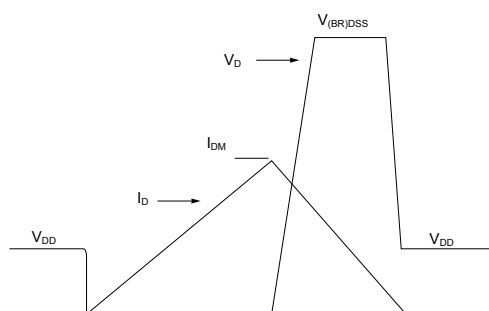
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Figure 15. Test circuit for inductive load switching and diode recovery times


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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform

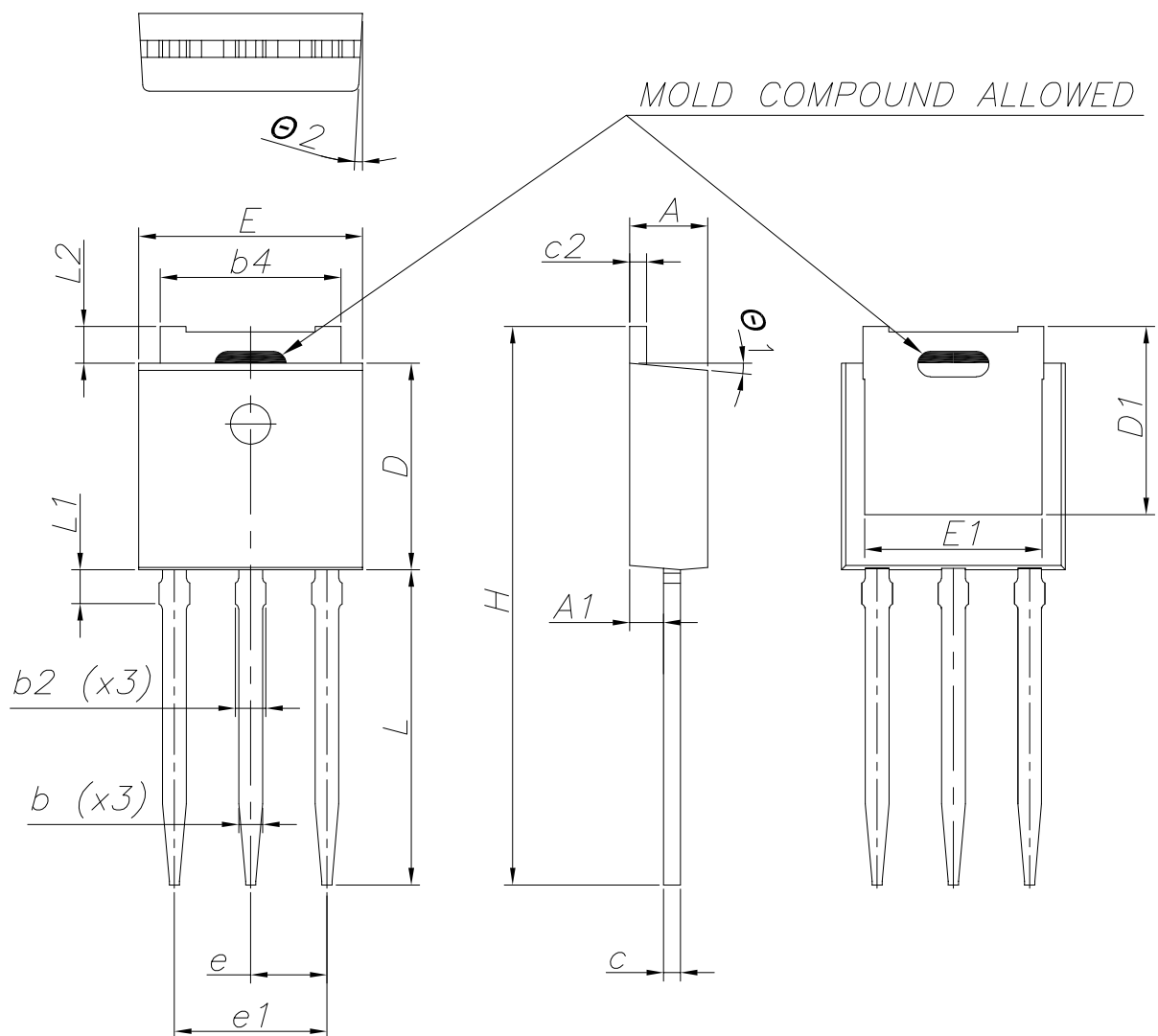

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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 IPAK (TO-251) type E package information

Figure 19. IPAK (TO-251) type E package outline



0068771_E_rev.16

Table 8. IPAK (TO-251) type E package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.30	5.53	5.75
E	6.50	6.60	6.70
E1	5.05	5.23	5.40
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
Ø1	3°	5°	7°
Ø2	1°	3°	5°

Revision history

Table 9. Document revision history

Date	Revision	Changes
09-Oct-2023	1	First release. The part number STD2NK90Z-1 was previously inserted in the DS4030.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	IPAK (TO-251) type E package information	8
	Revision history	10

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