

LM3875 Overture™ Audio Power Amplifier Series High-Performance 56W Audio Power Amplifier

General Description

The LM3875 is a high-performance audio power amplifier capable of delivering 56W of continuous average power to an 8Ω load with 0.1% (THD + N) from 20 Hz–20 kHz.

The performance of the LM3875, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) Protection Circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** Protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM3875 maintains an excellent Signal-to-Noise Ratio of greater than 95 dB(min) with a typical low noise floor of 2.0 μV. It exhibits extremely low (THD + N) values of 0.06% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

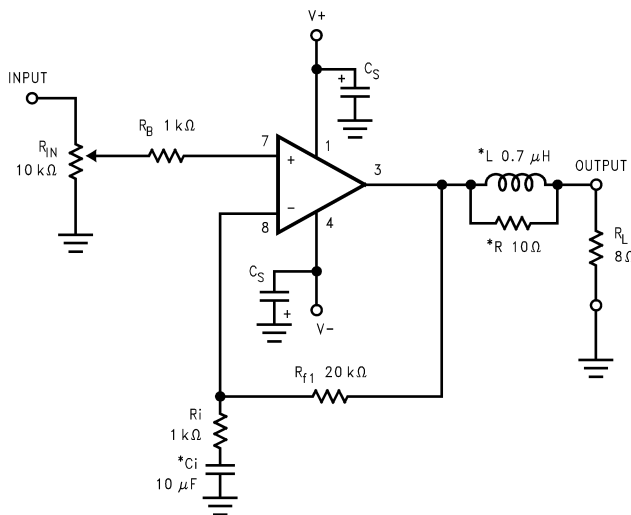
Features

- 56W continuous average output power into 8Ω
- 100W instantaneous peak output power capability
- Signal-to-Noise Ratio >95 dB (min)
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11 lead TO-220 package

Applications

- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application



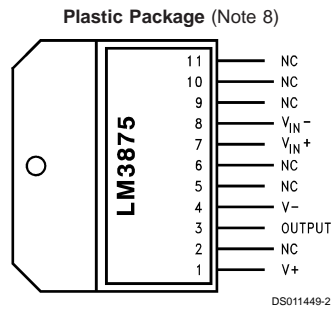
DS011449-1

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component function description.

FIGURE 1. Typical Audio Amplifier Application Circuit

Overture™ and SPiKe™ Protection are trademarks of National Semiconductor Corporation.

Connection Diagram



Top View
Order Number LM3875T or LM3875TF
See NS Package Number TA11B for
Staggered Lead Non-Isolated Package
or TF11B for Staggered Lead Isolated Package

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $ V^+ + V^- $ (No Signal)	94V
Supply Voltage $ V^+ + V^- $ (Input Signal)	84V
Common Mode Input Voltage	(V^+ or V^-) and $ V^+ + V^- \leq 80V$
Differential Input Voltage	60V
Output Current	Internally Limited
Power Dissipation (Note 3)	125W
ESD Susceptibility (Note 4)	2500V
Junction Temperature (Note 5)	150°C
Soldering Information	
T package (10 seconds)	260°C

Storage Temperature

–40°C to +150°C

Thermal Resistance

θ_{JC}

1°C/W

θ_{JA}

43°C/W

Operating Ratings (Notes 1, 2)

Temperature Range

$T_{MIN} \leq T_A \leq T_{MAX}$

–20°C $\leq T_A \leq$ +85°C

Supply Voltage $|V^+| + |V^-|$

20V to 84V

Note: Operation is guaranteed up to 84V, however, distortion may be introduced from the **SPIke** Protection Circuitry when operating above 70V if proper thermal considerations are not taken into account. Refer to the Thermal Considerations section for more information. (See **SPIke** Protection Response)

Electrical Characteristics (Notes 1, 2)

The following specifications apply for $V^+ = +35V$, $V^- = -35V$ with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM3875		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
$ V^+ + V^- $	Power Supply Voltage			20 84	V (Min) V (Max)
**P _O	Output Power (Continuous Average)	THD + N = 0.1% (Max) f = 1 kHz, f = 20 kHz	56	40	W (Min)
Peak P _O	Instantaneous Peak Output Power		100		W
THD + N	Total Harmonic Distortion Plus Noise	40W, 20 Hz $\leq f \leq$ 20 kHz A _v = 26 dB	0.06		%
**SR	Slew Rate (Note 9)	V _{IN} = 1.414 V _{rms} , f = 10 kHz Square-wave, R _L = 2 k Ω	11	5	V/ μ s (Min)
*I ₊	Total Quiescent Power Supply Current	V _{CM} = 0V, V _O = 0V, I _o = 0 mA	30	70	mA (Max)
*V _{OS}	Input Offset Voltage	V _{CM} = 0V, I _o = 0 mA	1	10	mV (Max)
I _B	Input Bias Current	V _{CM} = 0V, I _o = 0 mA	0.2	1	μ A (Max)
I _{OS}	Input Offset Current	V _{CM} = 0V, I _o = 0 mA	0.01	0.2	μ A (Max)
I _o	Output Current Limit	$ V^+ = V^- = 10V$, t _{on} = 10 ms, V _O = 0V	6	4	A (Min)
*V _{od}	Output Dropout Voltage	$ V^+ - V_{O-} $, V ⁺ = 20V, I _o = +100 mA $ V_{O-} - V^- $, V [–] = –20V, I _o = –100 mA	1.6 2.7	5 5	V (Max) V (Max)
*PSRR	Power Supply Rejection Ratio	V ⁺ = 40V to 20V, V [–] = –40V, V _{cm} = 0V, I _o = 0 mA V ⁺ = 40V, V [–] = –40V to –20V, V _{cm} = 0V, I _o = 0 mA	120 120	85 85	dB (Min)
*CMRR	Common Mode Rejection Ratio	V ⁺ = 60V to 20V, V [–] = –20V to –60V, V _{cm} = 20V to –20V, I _o = 0 mA	120	80	dB (Min)
*A _{VOL}	Open Loop Voltage Gain	$ V^+ = V^- = 40V$, R _L = 2 k Ω , $\Delta V_O = 60V$	120	90	dB (Min)
GBWP	Gain-Bandwidth Product	$ V^+ = V^- = 40V$ f _O = 100 kHz, V _{IN} = 50 mV _{rms}	8	2	MHz (Min)
**e _{IN}	Input Noise	IHF – A Weighting Filter R _{IN} = 600 Ω (Input Referred)	2.0	8.0	μ V (Max)

Electrical Characteristics (Notes 1, 2) (Continued)

The following specifications apply for $V^+ = +35V$, $V^- = -35V$ with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	LM3875		Units (Limits)
			Typical (Note 6)	Limit (Note 7)	
SNR	Signal-to-Noise Ratio	$P_O = 1W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	98 dB		dB
		$P_O = 40W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	114 dB		dB
		$P_{pk} = 100W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$	122 dB		dB
IMD	Intermodulation Distortion Test	60 Hz, 7 kHz, 4:1 (SMPTE)	0.004		%
		60 Hz, 7 kHz, 1:1 (SMPTE)	0.006		%

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: All voltages are measured with respect to supply GND, unless otherwise specified.

Note 3: For operating at case temperatures above $25^\circ C$, the device must be derated based on a $150^\circ C$ maximum junction temperature and a thermal resistance of $\theta_{JC} = 1.0^\circ C/W$ (junction to case). Refer to the Thermal Resistance figure in the Application Information section under **Thermal Considerations**.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: The operating junction temperature maximum is $150^\circ C$, however, the instantaneous Safe Operating Area temperature is $250^\circ C$.

Note 6: Typicals are measured at $25^\circ C$ and represent the parametric norm.

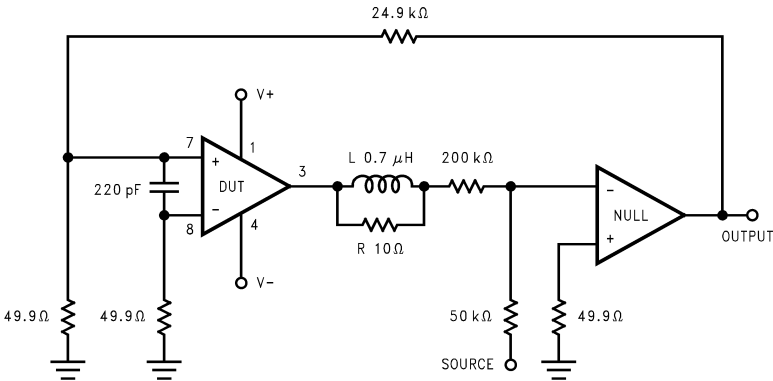
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The LM3875T package TA11B is a non-isolated package, setting the tab of the device and the heat sink at V^- potential when the LM3875 is directly mounted to the heat sink using only thermal compound. If a mica washer is used in addition to thermal compound, θ_{CS} (case to sink) is increased, but the heat sink will be isolated from V^- .

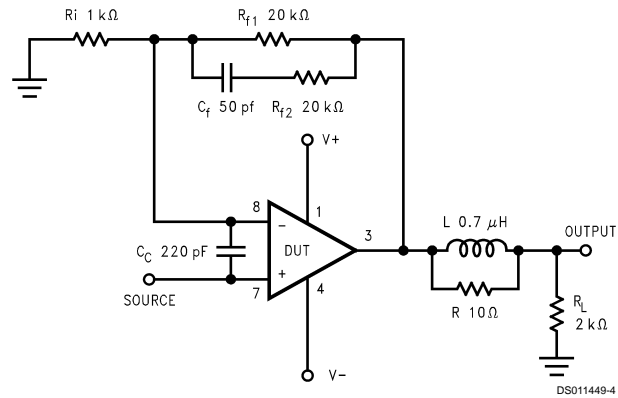
Note 9: The feedback compensation network limits the bandwidth of the closed-loop response and so the slew rate will be reduced due to the high frequency roll-off. Without feedback compensation, the slew rate is typically 16V/ μs .

Note 10: The output dropout voltage is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs. Supply Voltage graph in the **Typical Performance Characteristics** section.

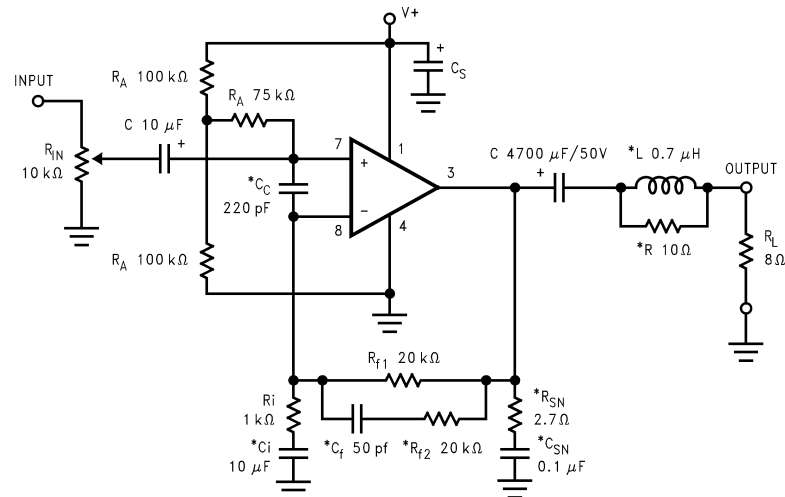
Test Circuit #1 (DC Electrical Test Circuit)



Test Circuit #2 (AC Electrical Test Circuit)



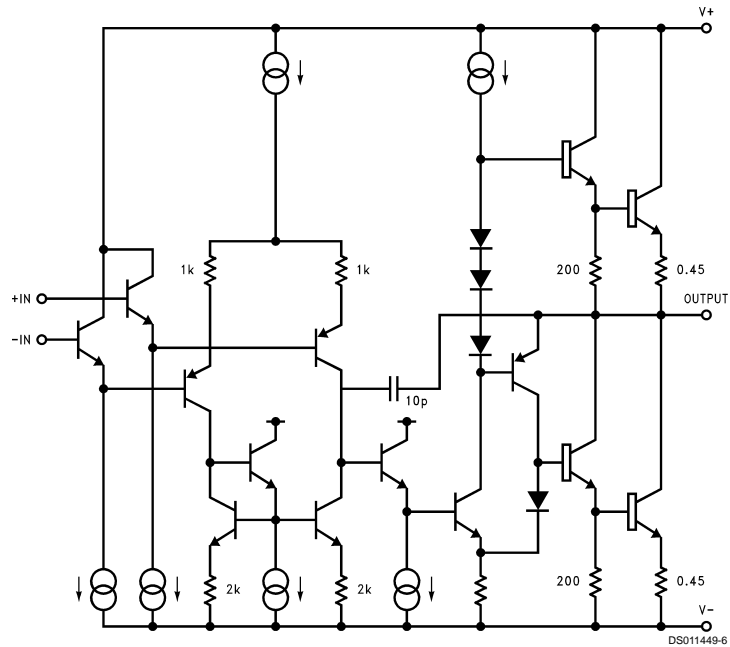
Single Supply Application Circuit



*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component function description.

FIGURE 2. Typical Single Supply Audio Amplifier Application Circuit

Equivalent Schematic (Excluding active protection circuitry)



External Components Description

(Figure 1 and Figure 2)

Components	Functional Description
1. R_{IN}	Acts as a volume control by setting the voltage level allowed to the amplifier's input terminals.
2. R_A	Provides DC voltage biasing for the single supply operation and bias current for the positive input terminal.
3. C_A	Provides bias filtering.
4. C	Provides AC coupling at the input and output of the amplifier for single supply operation.
5. R_B	Prevents currents from entering the amplifier's non-inverting input which may be passed through to the load upon power-down of the system due to the low input impedance of the circuitry when the under-voltage circuitry is off. This phenomenon occurs when the supply voltages are below 1.5V.
6. $*C_C$	Reduces the gain (bandwidth of the amplifier) at high frequencies to avoid quasi-saturation oscillations of the output transistor. The capacitor also suppresses external electromagnetic switching noise created from fluorescent lamps.
7. R_i	Inverting input resistance to provide AC Gain in conjunction with R_{f1} .
8. $*C_i$	Feedback capacitor. Ensures unity gain at DC. Also a low frequency pole (highpass roll-off) at: $f_c = 1/(2\pi R_i C_i)$.
9. R_{f1}	Feedback resistance to provide AC Gain in conjunction with R_i .
10. $*R_{f2}$	At higher frequencies feedback resistance works with C_f to provide lower AC Gain in conjunction with R_{f1} and R_i . A high frequency pole (lowpass roll-off) exists at: $f_c = [R_{f1} R_{f2}] (s + 1/R_{f2} C_f) / [(R_{f1} + R_{f2}) (s + 1/C_f (R_{f1} + R_{f2}))]$.
11. $*C_f$	Compensation capacitor that works with R_{f1} and R_{f2} to reduce the AC Gain at higher frequencies.
12. $*R_{SN}$	Works with C_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations.
13. $*C_{SN}$	Works with R_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations. $f_c = 1/(2\pi R_{SN} C_{SN})$.
14. $*L$	Provides high impedance at high frequencies so that R may decouple a highly capacitive load and reduce the Q of the series resonant circuit due to capacitive load. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load.
15. $*R$	

External Components Description (Figure 1 and Figure 2) (Continued)

Components	Functional Description
16. C_S	Provides power supply filtering and bypassing.

*Optional components dependent upon specific design requirements. Refer to the Application Information section for more information.

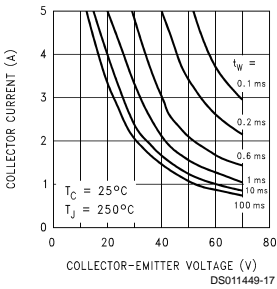
OPTIONAL EXTERNAL COMPONENT INTERACTION

Although the optional external components have specific desired functions that are designed to reduce the bandwidth and eliminate unwanted high frequency oscillations they may cause certain undesirable effects when they interact. Interaction may occur for components whose reactances are in close proximity to one another. One example would be the coupling capacitor, C_C , and the compensation capacitor, C_f . These two components act as low impedances to certain frequencies which will couple signals from the input to the output. Please take careful note of basic amplifier component functionality when designing in these components.

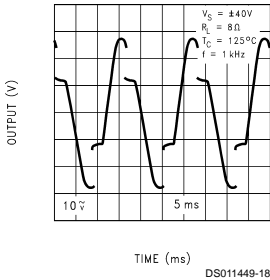
The optional external components shown in Figure 2 and described above are applicable in both single and split voltage supply configurations.

Typical Performance Characteristics

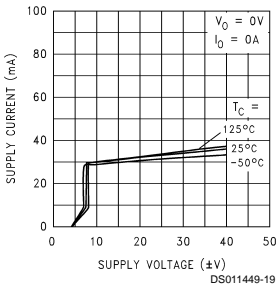
Safe Area



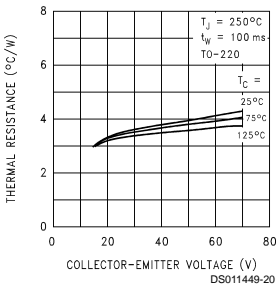
SPIKe Protection Response



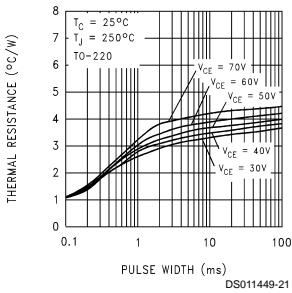
Supply Current vs Supply Voltage



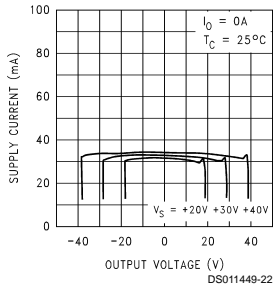
Pulse Thermal Resistance



Pulse Thermal Resistance

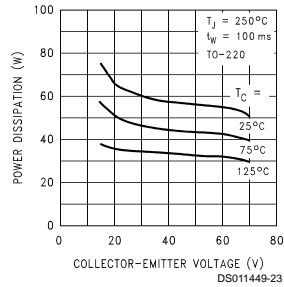


Supply Current vs Output Voltage



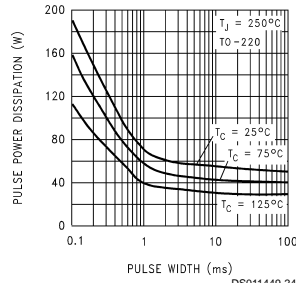
Typical Performance Characteristics (Continued)

Pulse Power Limit



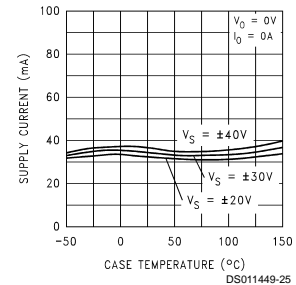
DS011449-23

Pulse Power Limit



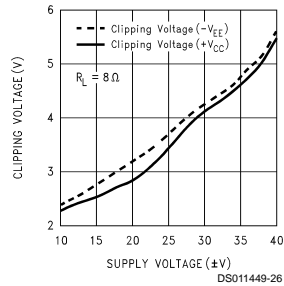
DS011449-24

Supply Current vs Case Temperature



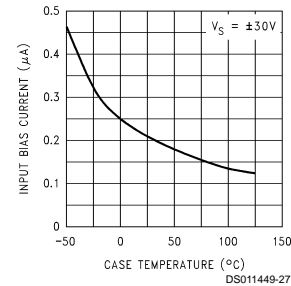
DS011449-25

Clipping Voltage vs Supply Voltage



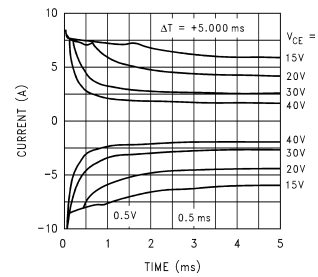
DS011449-26

Input Bias Current vs Case Temperature



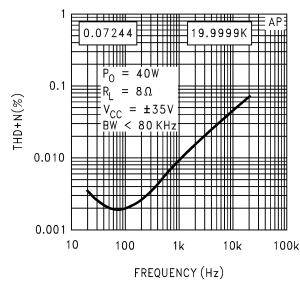
DS011449-27

Peak Output Current



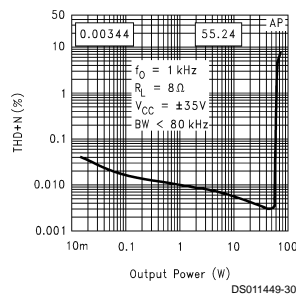
DS011449-28

THD + N vs Frequency



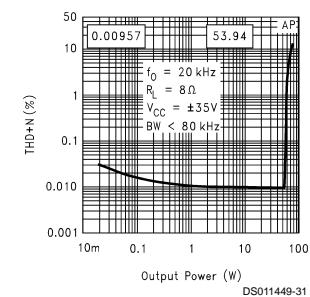
DS011449-29

THD + N vs Output Power



DS011449-30

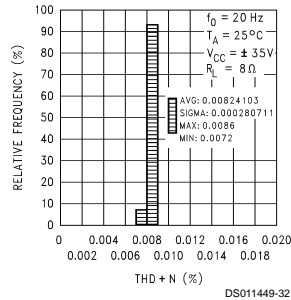
THD + N vs Output Power



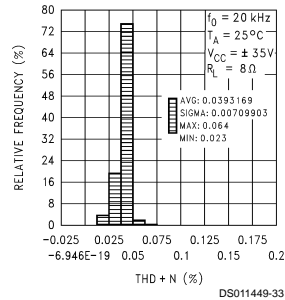
DS011449-31

Typical Performance Characteristics (Continued)

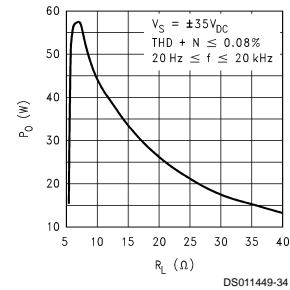
THD Distribution



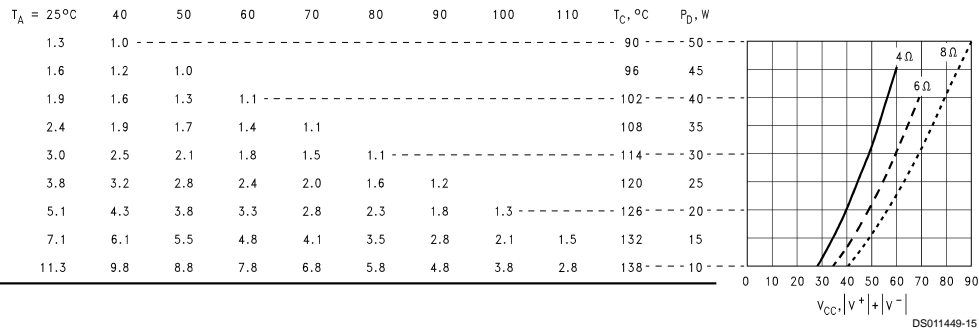
THD Distribution



Output Power vs Load Resistance

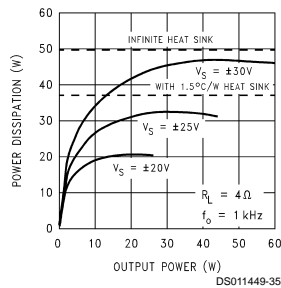


Max Heatsink Thermal Resistance (°C/W) at the Specified Ambient Temperature (°C) and Maximum Power Dissipation vs Supply Voltage

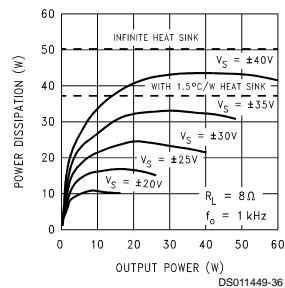


Note: The maximum heat sink thermal resistance values, θ_{SA} , in the table above were calculated using a $\theta_{CS} = 0.2^\circ\text{C/W}$ due to thermal compound.

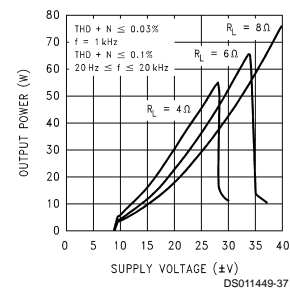
Power Dissipation vs Output Power



Power Dissipation vs Output Power

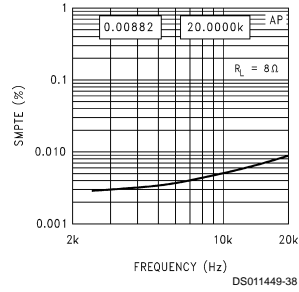


Output Power vs Supply Voltage

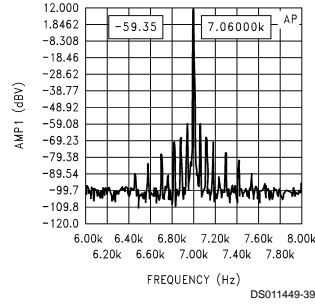


Typical Performance Characteristics (Continued)

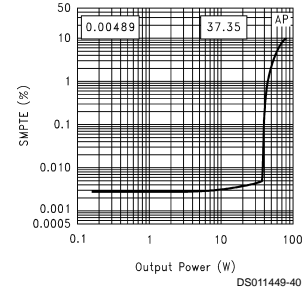
IMD 60 Hz, 4:1



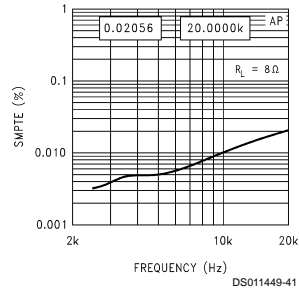
IMD 60 Hz, 7 kHz, 4:1



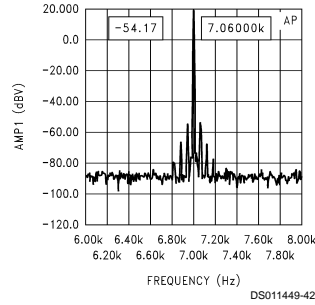
IMD 60 Hz, 7 kHz, 4:1



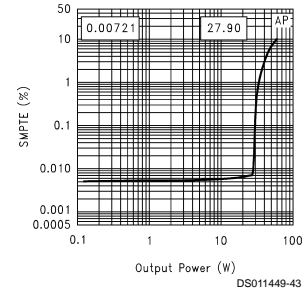
IMD 60 Hz, 1:1



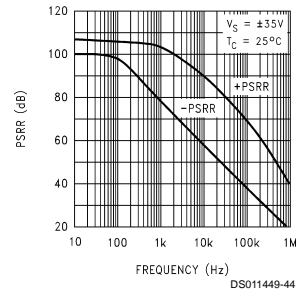
IMD 60 Hz, 7 kHz, 1:1



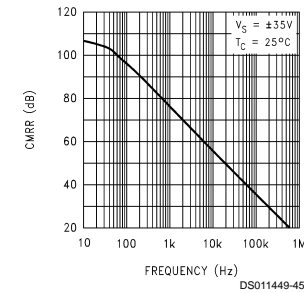
IMD 60 Hz, 7 kHz, 1:1



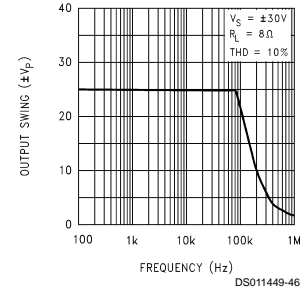
Power Supply Rejection Ratio



Common-Mode Rejection Ratio

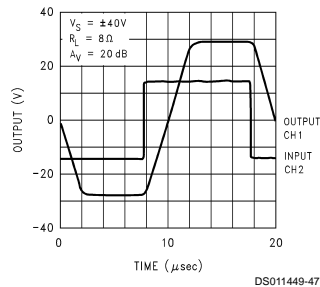


Large Signal Response

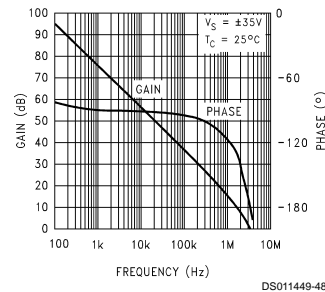


Typical Performance Characteristics (Continued)

Pulse Response



Open Loop Frequency Response



Application Information

GENERAL FEATURES

Under-Voltage Protection: Upon system power-up the under-voltage Protection Circuitry allows the power supplies and their corresponding caps to come up close to their full values before turning on the LM3875 such that no DC output spikes occur. Upon turn-off, the output of the LM3875 is brought to ground before the power supplies such that no transients occur at power-down.

Over-Voltage Protection: The LM3875 contains overvoltage protection circuitry that limits the output current to approximately 4A peak while also providing voltage clamping, though not through internal clamping diodes. The clamping effect is quite the same, however, the output transistors are designed to work alternately by sinking large current spikes.

SPiKe Protection: The LM3875 is protected from instantaneous peak-temperature stressing by the power transistor array. The Safe Operating Area graph in the **Typical Performance Characteristics** section shows the area of device operation where the SPiKe Protection Circuitry is not enabled. The waveform to the right of the SOA graph exemplifies how the dynamic protection will cause waveform distortion when enabled.

Thermal Protection: The LM3875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 165°C , the LM3875 shuts down. It starts operating again when the die temperature drops to about 155°C , but if the temperature again begins to rise, shutdown will occur again at 165°C . Therefore the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 165°C and 155°C . This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen as discussed in the **Thermal Considerations** section, such that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

THERMAL CONSIDERATIONS

Heat Sinking

The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry does not operate under normal circumstances. The heat sink should be chosen to dissipate the maximum IC power for a given supply voltage and rated load.

With high-power pulses of longer duration than 100 ms, the case temperature will heat up drastically without the use of a heat sink. Therefore the case temperature, as measured at the center of the package bottom, is entirely dependent on heat sink design and the mounting of the IC to the heat sink. For the design of a heat sink for your audio amplifier application refer to the **Determining the Correct Heat Sink** section.

Since a semiconductor manufacturer has no control over which heat sink is used in a particular amplifier design, we can only inform the system designer of the parameters and the method needed in the determination of a heat sink. With this in mind, the system designer must choose his supply voltages, a rated load, a desired output power level, and know the ambient temperature surrounding the device. These parameters are in addition to knowing the maximum junction temperature and the thermal resistance of the IC, both of which are provided by National Semiconductor.

As a benefit to the system designer we have provided Maximum Power Dissipation vs Supply Voltages curves for various loads in the **Typical Performance Characteristics** section, giving an accurate figure for the maximum thermal resistance required for a particular amplifier design. This data was based on $\theta_{JC} = 1^{\circ}\text{C/W}$ and $\theta_{CS} = 0.2^{\circ}\text{C/W}$. We also provide a section regarding heat sink determination for any audio amplifier design where θ_{CS} may be a different value. It should be noted that the idea behind dissipating the maximum power within the IC is to provide the device with a low resistance to convection heat transfer such as a heat sink. Therefore, it is necessary for the system designer to be conservative in his heat sink calculations. As a rule, the lower the thermal resistance of the heat sink the higher the amount of power that may be dissipated. This is, of course, guided by the cost and size requirements of the system. Convection cooling heat sinks are available commercially, and their manufacturers should be consulted for ratings.

Application Information (Continued)

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, the thermal resistance will be no better than 0.5°C/W, and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important and can be determined from heat sink manufacturer's specification sheets.

Should it be necessary to isolate V^- from the heat sink, an insulating washer is required. Hard washers like beryllium oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound.

Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

Determining Maximum Power Dissipation

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation (P_D) calculation may result in inadequate heatsinking, causing thermal shutdown circuitry to operate and limit the output power.

The following equations can be used to accurately calculate the maximum and average integrated circuit power dissipation for your amplifier design, given the supply voltage, rated load, and output power. These equations can be directly applied to the Power Dissipation vs Output Power curves in the **Typical Performance Characteristics** section.

Equation (1) exemplifies the maximum power dissipation of the IC and Equations (2), (3) exemplify the average IC power dissipation expressed in different forms.

$$P_{DMAX} = V_{CC}^2 / 2\pi^2 R_L \quad (1)$$

where V_{CC} is the total supply voltage

$$P_{DAVE} = (V_{OPK}/R_L) [V_{CC}/\pi - V_{OPK}/2] \quad (2)$$

where V_{CC} is the total supply voltage and $V_{OPK} = V_{CC}/\pi$

$$P_{DAVE} = V_{CC} V_{OPK} / \pi R_L - V_{OPK}^2 / 2 R_L \quad (3)$$

where V_{CC} is the total supply voltage.

Determining the Correct Heat Sink

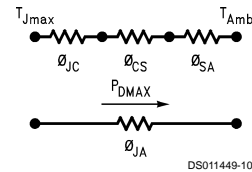
Once the maximum IC power dissipation is known for a given supply voltage, rated load, and the desired rated output power the maximum thermal resistance (in °C/W) of a heat sink can be calculated. This calculation is made using Equation (4) and is based on the fact that thermal heat flow parameters are analogous to electrical current flow properties.

It is also known that typically the thermal resistance, θ_{JC} (junction to case), of the LM3875 is 1°C/W and that using Thermalloy Thermacote thermal compound provides a thermal resistance, θ_{CS} (case to heat sink), of about 0.2°C/W as explained in the **Heat Sinking** section.

Referring to the figure below, it is seen that the thermal resistance from the die (junction) to the outside air (ambient) is a combination of three thermal resistances, two of which are known, θ_{JC} and θ_{CS} . Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM3875 is equal to the following:

$$P_{DMAX} = (T_{Jmax} - T_{Amb}) / \theta_{JA}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$



But since we know P_{DMAX} , θ_{JC} , and θ_{CS} for the application and we are looking for θ_{SA} , we have the following:

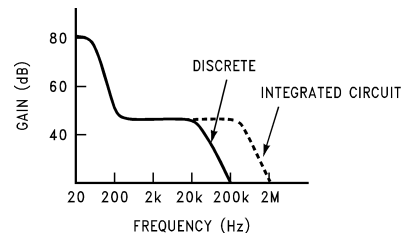
$$\theta_{SA} = [(T_{Jmax} - T_{Amb}) - P_{DMAX} (\theta_{JC} + \theta_{CS})] / P_{DMAX} \quad (4)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier application and its corresponding parameters as described previously. If the ambient temperature that the audio amplifier is to be working under is higher than the normal 25°C, then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

Equations (1), (4) are the only equations needed in the determination of the maximum heat sink thermal resistance. This is, of course, given that the system designer knows the required supply voltages to drive his rated load at a particular power output level and the parameters provided by the semiconductor manufacturer. These parameters are the junction to case thermal resistance, θ_{JC} , $T_{Jmax} = 150^\circ\text{C}$, and the recommended Thermalloy Thermacote thermal compound resistance, θ_{CS} .

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit designs to discrete amplifier designs. Discrete transistor amps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated below.



Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal-to-noise measurements if not considered during the measurement pro-

Application Information (Continued)

cess. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth, (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter (Note 11). A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to the frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

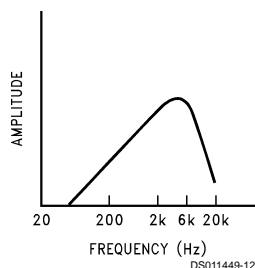
Note 11: CCIR/ARM: A Practical Noise Measurement Method, by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

In addition to noise filtering, differing meter types give different noise readings. Meter responses include:

1. RMS reading,
2. average responding,
3. peak reading, and
4. quasi peak reading.

Although theoretical noise analysis is derived using true RMS based calculations, most actual measurements are taken with ARM (Average Responding Meter) test equipment.

Typical signal-to-noise figures are listed for an A-weighted filter which is commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown below.



SUPPLY BYPASSING

The LM3875 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as "motorboating" or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10 μ F or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1 μ F) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes low distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470 μ F or more.

LEAD INDUCTANCE

Power op amps are sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load.

Lead inductance can also cause voltage surges on the supplies. With long leads to the power supply, energy is stored in the lead inductance when the output is shorted. This energy can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With at least a 20 μ F local bypass, these voltage surges are important only if the lead length exceeds a couple feet (>1 μ H lead inductance). Twisting together the supply and ground leads minimizes the effect.

LAYOUT, GROUND LOOPS AND STABILITY

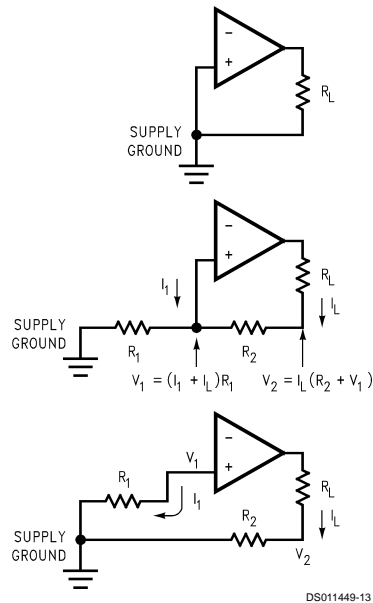
The LM3875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but as with any other high-current amplifier, the LM3875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μ F supply decoupling capacitors as close as possible to the LM3875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths should be as short as possible.

In general, with fast, high-current circuitry, all sorts of problems can arise from improper grounding which again can be avoided by returning all grounds separately to a common point. Without isolating the ground signals and returning the grounds to a common point, ground loops may occur.

"Ground Loop" is the term used to describe situations occurring in ground systems where a difference in potential exists between two ground points. Ideally a ground is a ground, but unfortunately, in order for this to be true, ground conductors with zero resistance are necessary. Since real world ground leads possess finite resistance, currents running through them will cause finite voltage drops to exist. If two ground return lines tie into the same path at different points there will be a voltage drop between them. The first figure below shows a common ground example where the positive input ground and the load ground are returned to the supply ground point via the same wire. The addition of the finite wire resistance, R_2 , results in a voltage difference between the two points as shown below.

Application Information (Continued)



The load current I_L will be much larger than input bias current I_1 , thus V_1 will follow the output voltage directly, i.e., in phase. Therefore the voltage appearing at the non-inverting input is effectively positive feedback and the circuit may oscillate. If there were only one device to worry about then the values of R_1 and R_2 would probably be small enough to be ignored; however, several devices normally comprise a total system. Any ground return of a separate device, whose output is in phase, can feedback in a similar manner and cause instabilities. Out of phase ground loops also are troublesome, causing unexpected gain and phase errors.

The solution to most ground loop problems is to always use a single-point ground system, although this is sometimes impractical. The third figure above is an example of a single-point ground system.

The single-point ground concept should be applied rigorously to all components and all circuits when possible. Violations of single-point grounding are most common among printed circuit board designs, since the circuit is surrounded by large ground areas which invite the temptation to run a device to the closest ground spot. As a final rule, make all ground returns low resistance and low inductance by using large wire and wide traces.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor, C_C , (on the order of 50 pF–500 pF) across the LM3875 input terminals. Refer to the **External Components Description** section relating to component interaction with C_T .

REACTIVE LOADING

It is hard for most power amplifiers to drive highly capacitive loads very effectively and normally results in oscillations or ringing on the square wave response. If the output of the LM3875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.2 μ F. If highly capacitive loads are expected due to long speaker cables, a method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10 Ω resistor in parallel with a 0.7 μ H inductor. The inductor-resistor combination as shown in the **Typical Application Circuit** isolates the feedback amplifier from the load by providing high output impedance at high frequencies thus allowing the 10 Ω resistor to decouple the capacitive load and reduce the Q of the series resonant circuit. The LR combination also provides low output impedance at low frequencies thus shorting out the 10 Ω resistor and allowing the amplifier to drive the series RC load (large capacitive load due to long speaker cables) directly.

GENERALIZED AUDIO POWER AMPLIFIER DESIGN

The system designer usually knows some of the following parameters when starting an audio amplifier design:

Desired Power Output	Input Level
Input Impedance	Load Impedance
Maximum Supply Voltage	Bandwidth

The power output and load impedance determine the power supply requirements, however, depending upon the application some system designers may be limited to certain maximum supply voltages. If the designer does have a power supply limitation, he should choose a practical load impedance which would allow the amplifier to provide the desired output power, keeping in mind the current limiting capabilities of the device. In any case, the output signal swing and current are found from (where P_O is the average output power):

$$V_{\text{Opeak}} = \sqrt{2 R_L P_O} \quad (5)$$

$$I_{\text{Opeak}} = \sqrt{(2 P_O)/R_L} \quad (6)$$

To determine the maximum supply voltage the following parameters must be considered. Add the dropout voltage (5 volts for LM3875) to the peak output swing, V_{Opeak} , to get the supply rail value, (i.e. + $V_{\text{Opeak}} + V_{\text{od}}$) at a current of I_{Opeak} . The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions. Therefore, the maximum supply voltage is obtained from the following equation:

$$\text{max. supplies} \approx \pm (V_{\text{Opeak}} + V_{\text{od}}(1 + \text{regulation}))(1.1) \quad (7)$$

The input sensitivity and the output power specs determine the minimum required gain as depicted below:

$$A_V \geq (\sqrt{P_O R_L})/(V_{\text{IN}}) = V_{\text{orms}}/V_{\text{inrms}} \quad (8)$$

Normally the gain is set between 20 and 200; for a 40W, 8 Ω audio amplifier this results in a sensitivity of 894 mV and 89 mV, respectively. Although higher gain amplifiers provide greater output power and dynamic headroom capabilities, there are certain shortcomings that go along with the so called "gain". The input referred noise floor is increased and hence the SNR is worse. With the increase in gain, there is also a reduction of the power bandwidth which results in a

Application Information (Continued)

decrease in feedback thus not allowing the amplifier to respond as quickly to nonlinearities. This decreased ability to respond to nonlinearities increases the THD + N specification.

The desired input impedance is set by R_{IN} . Very high values can cause board layout problems and DC offsets at the output. The value for the feedback resistance, R_{f1} , should be chosen to be a relatively large value (10 k Ω –100 k Ω), and the other feedback resistance, R_i , is calculated using standard op amp configuration gain equations. Most audio amplifiers are designed from the non-inverting amplifier configuration.

DESIGN A 40W/8 Ω AUDIO AMPLIFIER

Given:

Power Output	40W
Load Impedance	8 Ω
Input Level	1V _(max)
Input Impedance	100 k Ω
Bandwidth	20 Hz–20 kHz \pm 0.25 dB

Equations (5), (6) give:

$$40W/8\Omega \quad V_{opeak} = 25.3V \quad I_{opeak} = 3.16A$$

Therefore the supply required is: $\pm 30.3V$ @3.16A

With 15% regulation and high line the final supply voltage is $\pm 38.3V$ using Equation (7). At this point it is a good idea to check the Power Output vs Supply Voltage to ensure that the required output power is obtainable from the device while maintaining low THD + N. It is also good to check the Power Dissipation vs Supply Voltage to ensure that the device can handle the internal power dissipation. At the same time designing in a relatively practical sized heat sink with a low thermal resistance is also important. Refer to **Typical Performance Characteristics** graphs and the **Thermal Considerations** section for more information.

The minimum gain from Equation (8) is: $A_v \geq 18$

We select a gain of 21 (Non-Inverting Amplifier); resulting in a sensitivity of 894 mV.

Letting R_{IN} equal 100 k Ω gives the required input impedance, however, this would eliminate the "volume control" unless an additional input impedance was placed in series with the 10 k Ω potentiometer that is depicted in Figure 1. Adding the additional 100 k Ω resistor would ensure the minimum required input impedance.

For low DC offsets at the output we let $R_{f1} = 100$ k Ω . Solving for R_i (Non-Inverting Amplifier) gives the following:

$$R_i = R_{f1}/(A_v - 1) = 100k/(21 - 1) = 5 \text{ k}\Omega; \text{ use } 5.1 \text{ k}\Omega$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole give 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = 20 \text{ Hz}/5 = 4 \text{ Hz}$$

$$f_H = 20 \text{ kHz} \times 5 = 100 \text{ kHz}$$

At this point, it is a good idea to ensure that the Gain Bandwidth Product for the part will provide the designed gain out to the upper 3 dB point of 100 kHz. This is why the minimum GBWP of the LM3875 is important.

$$GBWP = A_v \times f_3 \text{ dB} = 21 \times 100 \text{ kHz} = 2.1 \text{ MHz}$$

$$GBWP = 2.0 \text{ MHz (min) for LM3875}$$

Solving for the low frequency roll-off capacitor, C_i , we have:

$$C_i > 1/(2\pi R_i f_L) = 7.8 \mu\text{F}; \text{ use } 10 \mu\text{F}.$$

Definition of Terms

Input Offset Voltage: The absolute value of the voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage and current.

Input Bias Current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input Offset Current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Quiescent Supply Current: The current required from the power supply to operate the amplifier with no load and the output voltage and current at zero.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Class B Amplifier: The most common type of audio power amplifier that consists of two output devices each of which conducts for 180° of the input cycle. The LM3875 is a Quasi-AB type amplifier.

Crossover Distortion: Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current providing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for ICs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion on the negative going transition through zero crossing at the higher audio frequencies.

THD + N: Total Harmonic Distortion plus Noise refers to the measurement technique in which the fundamental component is removed by a bandreject (notch) filter and all remaining energy is measured including harmonics and noise.

Signal-to-Noise Ratio: The ratio of a system's output signal level to the system's output noise level obtained in the absence of a signal. The output reference signal is either specified or measured at a specified distortion level.

Continuous Average Output Power: The minimum sine wave continuous average power output in watts (or dBW) that can be delivered into the rated load, over the rated bandwidth, at the rated maximum total harmonic distortion.

Music Power: A measurement of the peak output power capability of an amplifier with either a signal duration sufficiently short that the amplifier power supply does not sag during the measurement, or when high quality external power supplies are used. This measurement (an IHF standard) assumes that with normal music program material the amplifier power supplies will sag insignificantly.

Definition of Terms (Continued)

Peak Power: Most commonly referred to as the power output capability of an amplifier that can be delivered to the load; specified by the part's maximum voltage swing.

Headroom: The margin between an actual signal operating level (usually the power rating of the amplifier with particular supply voltages, a rated load value, and a rated THD + N figure) and the level just before clipping distortion occurs, expressed in decibels.

Large Signal Voltage Gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Output-Current Limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once SPIke protection circuitry is activated.

Output Saturation Threshold (Clipping Point): The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Power Dissipation Rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

Thermal Resistance: The peak, junction-temperature rise, per unit of internal power dissipation (units in °C/W), above the case temperature as measured at the center of the package bottom.

The DC thermal resistance applies when one output transistor is operating continuously. The AC thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 3 dB below the rated output. For example, an amplifier rated at 60W with ≤0.25% THD + N, would make its power bandwidth measured as the

difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Gain-Bandwidth Product: The Gain-Bandwidth Product is a way of predicting the high-frequency usefulness of an op amp. The Gain-Bandwidth Product is sometimes called the unity-gain frequency or unity-gain cross frequency because the open-loop gain characteristic passes through or crosses unity gain at this frequency. Simply, we have the following relationship:

$$A_{CL1} \times f_1 = A_{CL2} \times f_2$$

Assuming that at unity-gain

$$(A_{CL1} = 1 \text{ or } 0 \text{ dB}) f_u = f_1 = \text{GBWP},$$

then we have the following:

$$\text{GBWP} = A_{CL2} \times f_2$$

This says that once f_u (GBWP) is known for an amplifier, then the open-loop gain can be found at any frequency. This is also an excellent equation to determine the 3 dB point of a closed-loop gain, assuming that you know the GBWP of the device. Refer to the diagram below.

Bi-amplification: The technique of splitting the audio frequency spectrum into two sections and using individual power amplifiers to drive a separate woofer and tweeter. Crossover frequencies for the amplifiers usually vary between 500 Hz and 1600 Hz. "Biamping" has the advantages of allowing smaller power amps to produce a given sound pressure level and reducing distortion effects produced by overdrive in one part of the frequency spectrum affecting the other part.

C.C.I.R./A.R.M.:

Literally: International Radio Consultative Committee Average Responding Meter

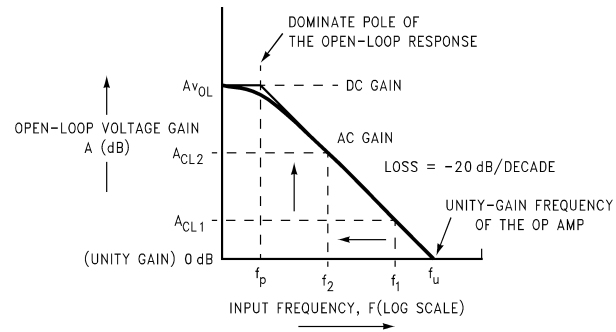
This refers to a weighted noise measurement for a Dolby B type noise reduction system. A filter characteristic is used that gives a closer correlation of the measurement with the subjective annoyance of noise to the ear. Measurements made with this filter cannot necessarily be related to unweighted noise measurements by some fixed conversion factor since the answers obtained will depend on the spectrum of the noise source.

S.P.L.: Sound Pressure Level—usually measured with a microphone/meter combination calibrated to a pressure level of 0.0002 μBars (approximately the threshold hearing level).

$$\text{S.P.L.} = 20 \log 10P/0.0002 \text{ dB}$$

Where P is the R.M.S sound pressure in microbars. (1 Bar = 1 atmosphere = 14.5 lb./in² = 194 dB S.P.L.).

Definition of Terms (Continued)



DS011449-14

The drawing shows the mechanical specifications for the TA11B package. The top view includes dimensions for the overall width, pin pitch, and mounting hole locations. The side view shows the package height, lead dimensions, and the 7° lead angle.

Top View Dimensions:

- Overall Width: 0.788 ± 0.010 (20.01 \pm 0.254)
- Pin Pitch: 0.150 ± 0.002 (3.810 \pm 0.051)
- Mounting Hole Diameter: 0.110 (2.794)
- Pin 1 Indicator: 0.120 ± 0.010 (3.048 \pm 0.254)
- Pin 1 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 10 Position: 0.169 ± 0.010 (4.293 \pm 0.254)
- Pin 11 Position: 0.038 (0.965)
- Pin 12 Position: 0.067 (1.702)
- Pin 13 Position: 0.200 ± 0.010 (5.080 \pm 0.254)
- Pin 14 Position: 0.016 ± 0.002 (0.406 \pm 0.051)
- Pin 15 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 16 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 17 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 18 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 19 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 20 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 21 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 22 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 23 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 24 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 25 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 26 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 27 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 28 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 29 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 30 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 31 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 32 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 33 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 34 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 35 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 36 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 37 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 38 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 39 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 40 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 41 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 42 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 43 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 44 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 45 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 46 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 47 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 48 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 49 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 50 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 51 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 52 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 53 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 54 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 55 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 56 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 57 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 58 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 59 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 60 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 61 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 62 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 63 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 64 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 65 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 66 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 67 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 68 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 69 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 70 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 71 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 72 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 73 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 74 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 75 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 76 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 77 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 78 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 79 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 80 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 81 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 82 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 83 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 84 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 85 Position: 0.061 ± 0.002 (1.549 \pm 0.051)
- Pin 86 Position: $0.061 \pm$

[illegible]

18

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507