

ZXMN3F30FH

30V SOT23 N-channel enhancement mode MOSFET

Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
30	0.047 @ $V_{GS} = 10V$	4.6
	0.065 @ $V_{GS} = 4.5V$	4.0



Description

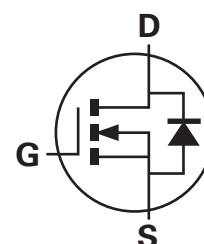
This new generation Trench MOSFET from Zetex features low on-resistance achievable with 4.5V gate drive.

Features

- Low on-resistance
- 4.5V gate drive capability
- SOT23

Applications

- DC-DC Converters
- Power management functions
- Motor Control

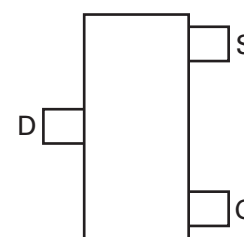


Ordering information

DEVICE	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN3F30FHTA	7	8	3000

Device marking

KNA



Top view

ZXMN3F30FH

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain source voltage	V_{DSS}	30	V
Gate source voltage	V_{GS}	± 20	V
Continuous Drain Current @ $V_{GS}=4.5$; $T_A=25^{\circ}\text{C}^{(b)}$ @ $V_{GS}=4.5$; $T_A=70^{\circ}\text{C}^{(b)}$ @ $V_{GS}=4.5$; $T_A=25^{\circ}\text{C}^{(a)}$	I_D	4.6 3.7 3.8	A A A
Pulsed drain current ^(c)	I_{DM}	21	A
Continuous source current (body diode) ^(b)	I_S	1.5	A
Pulsed source current (body diode) ^(c)	I_{SM}	21	A
Power dissipation at $T_A=25^{\circ}\text{C}^{(a)}$ Linear derating factor	P_D	0.95 7.6	W mW/ $^{\circ}\text{C}$
Power dissipation at $T_A=25^{\circ}\text{C}^{(b)}$ Linear derating factor	P_D	1.4 11.2	W mW/ $^{\circ}\text{C}$
Operating and storage temperature range	T_j, T_{stg}	-55 to 150	$^{\circ}\text{C}$

Thermal resistance

Parameter	Symbol	Limit	Unit
Junction to ambient ^(a)	$R_{\theta JA}$	131	$^{\circ}\text{C/W}$
Junction to ambient ^(b)	$R_{\theta JA}$	89	$^{\circ}\text{C/W}$
Junction to lead ^(d)	$R_{\theta JL}$	68	$^{\circ}\text{C/W}$

NOTES:

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

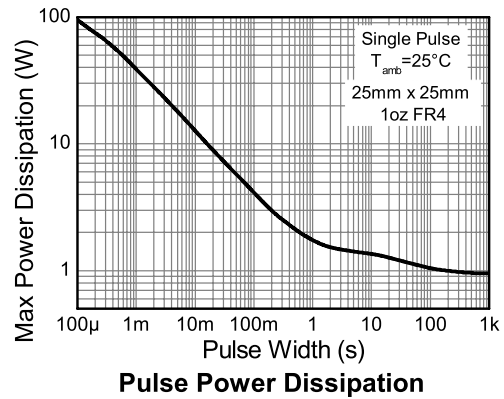
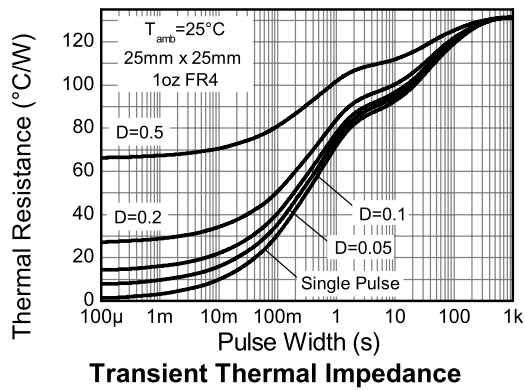
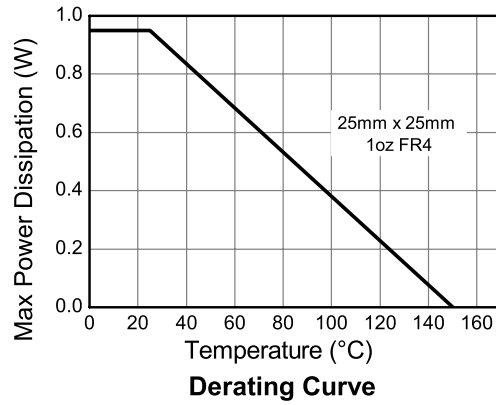
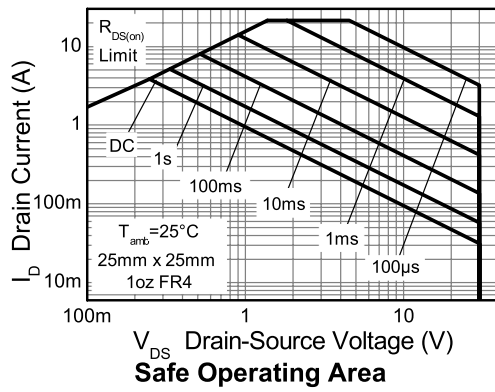
(b) For a device surface mounted on FR4 PCB measured at $t \leq 5$ sec.

(c) Repetitive rating - 25mm x 25mm FR4 PCB, $D=0.02$, pulse width 300 μs - pulse width limited by maximum junction temperature.

(d) Thermal resistance from junction to solder-point (at the end of the drain lead).

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Thermal characteristics



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Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	30			V	I _D = 250μA, V _{GS} =0V
Zero Gate Voltage Drain Current	I _{DSS}			0.5	μA	V _{DS} = 30V, V _{GS} =0V
Gate-Body Leakage	I _{GSS}			100	nA	V _{GS} =±20V, V _{DS} =0V
Gate-Source Threshold Voltage	V _{GS(th)}	1.0		3.0	V	I _D = 250μA, V _{DS} =V _{GS}
Static Drain-Source On-State Resistance (*)	R _{DS(on)}			0.047 0.065	Ω Ω	V _{GS} = 10V, I _D = 3.2A V _{GS} = 4.5V, I _D = 2.8A
Forward Transconductance(*) (†)	g _{fs}		5.2		S	V _{DS} = 15V, I _D = 2.5A
Dynamic (†)						
Input Capacitance	C _{iss}		318		pF	V _{DS} = 15V, V _{GS} =0V f=1MHz
Output Capacitance	C _{oss}		75		pF	
Reverse Transfer Capacitance	C _{rss}		45		pF	
Switching (†) (§)						
Turn-On-Delay Time	t _{d(on)}		1.6		ns	V _{DD} = 15V, V _{GS} = 10V I _D = 1A R _G ≈ 6.0Ω
Rise Time	t _r		2.6		ns	
Turn-Off Delay Time	t _{d(off)}		17		ns	
Fall Time	t _f		9.3		ns	
Total Gate Charge	Q _g		7.7		nC	V _{DS} = 15V, V _{GS} = 10V I _D = 2.5A
Gate-Source Charge	Q _{gs}		1		nC	
Gate Drain Charge	Q _{gd}		1.8		nC	
Source-drain diode						
Diode Forward Voltage(*)	V _{SD}		0.73	1.2	V	I _S = 1.25A, V _{GS} =0V

NOTES:

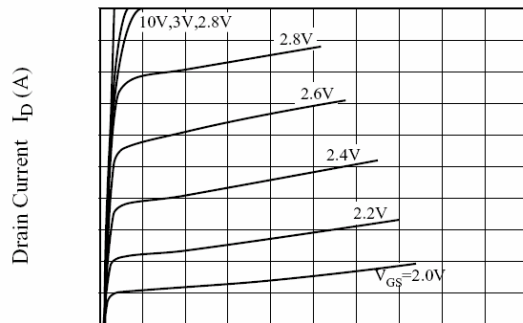
(*) Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

(†) For design aid only, not subject to production testing.

(‡) Switching characteristics are independent of operating junction temperature.

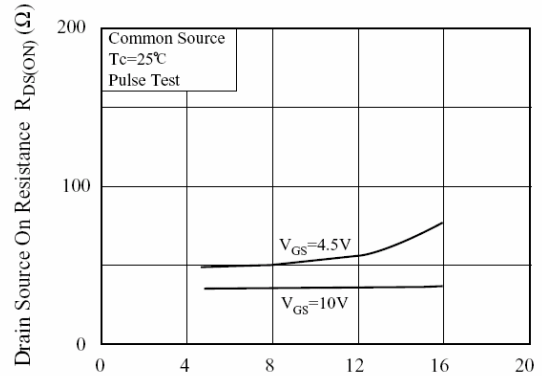
Typical characteristics

Fig1. $V_{DS} - I_D$



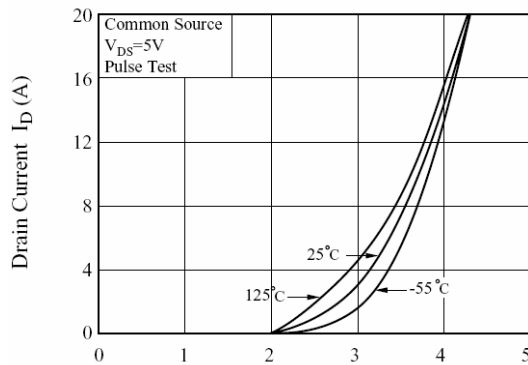
Drain - Source Voltage V_{DS} (V)

Fig2. $R_{DS(ON)} - I_D$



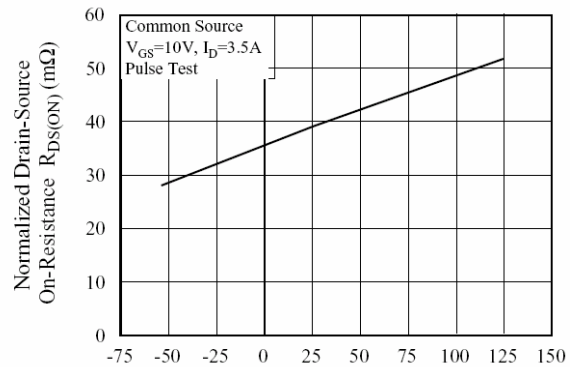
Drain - Current I_D (A)

Fig3. $V_{GS} - I_D$



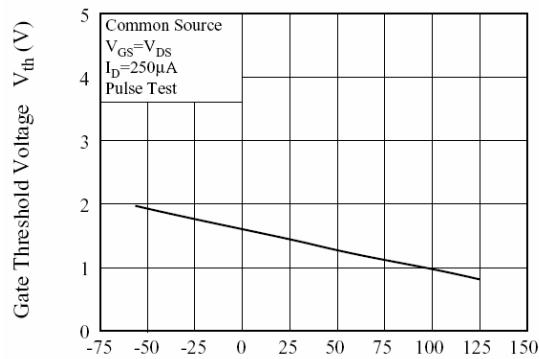
Gate Source Voltage V_{GS} (V)

Fig4. $R_{DS(ON)} - T_j$



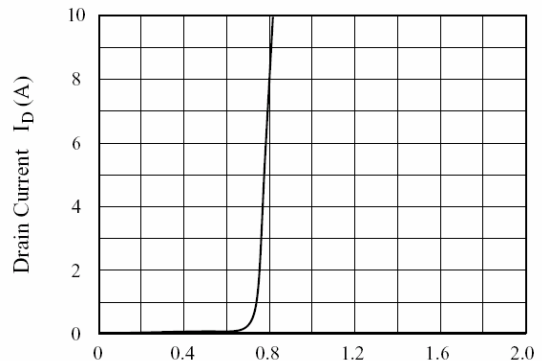
Junction Temperature T_j ($^\circ\text{C}$)

Fig5. $V_{th} - T_j$



Junction Temperature T_j ($^\circ\text{C}$)

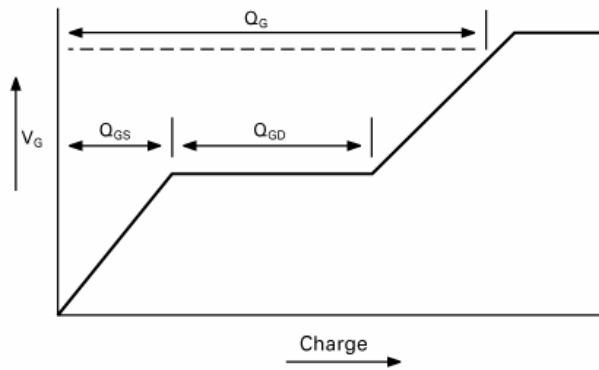
Fig6. $I_S - V_{SDF}$



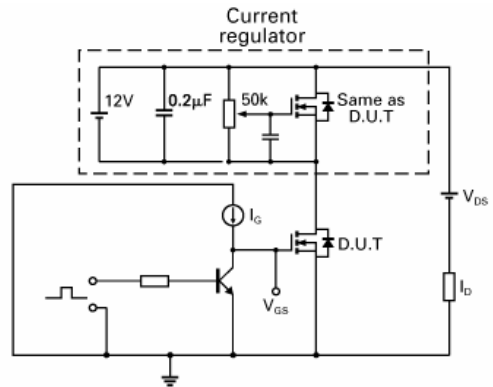
Source - Drain Forward Voltage V_{SDF} (V)

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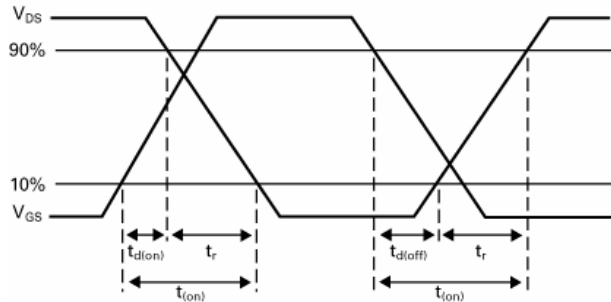
Test circuits



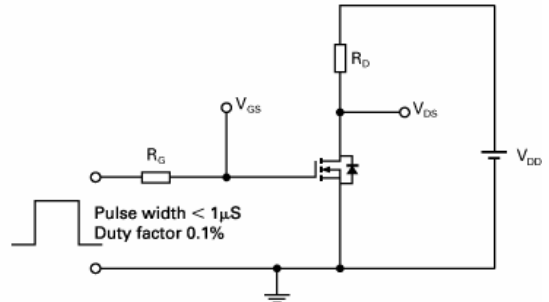
Basic gate charge waveform



Gate charge test circuit



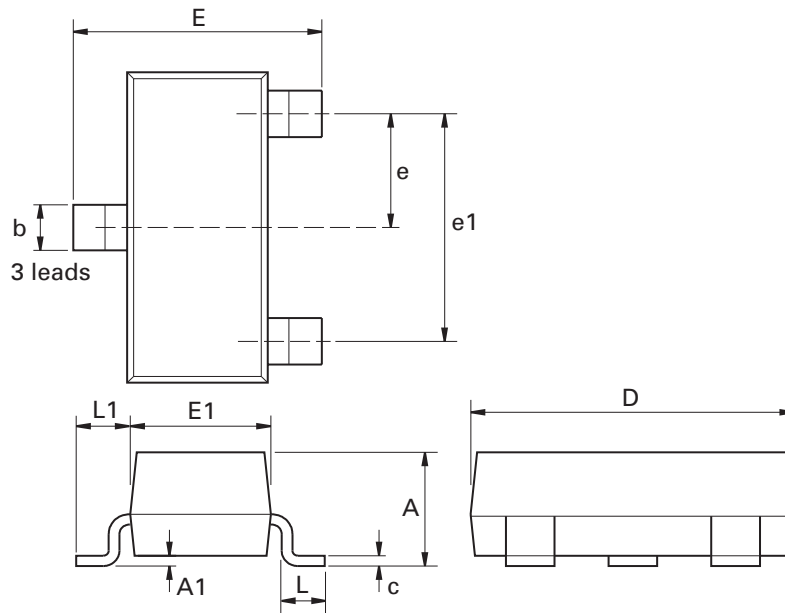
Switching time waveforms



Switching time test circuit

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Package outline - SOT23



Dim.	Millimeters		Inches		Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	-	1.12	-	0.044	e1	1.90 NOM		0.075 NOM	
A1	0.01	0.10	0.0004	0.004	E	2.10	2.64	0.083	0.104
b	0.30	0.50	0.012	0.020	E1	1.20	1.40	0.047	0.055
c	0.085	0.20	0.003	0.008	L	0.25	0.60	0.0098	0.0236
D	2.80	3.04	0.110	0.120	L1	0.45	0.62	0.018	0.024
e	0.95 NOM		0.037 NOM		-	-	-	-	-

Note: Controlling dimensions are in millimeters. Approximate dimensions are provided in inches

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