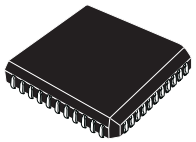
SGS-THOMSON MICROELECTRONICS

L6238S

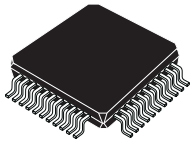
12V SENSORLESS SPINDLE MOTOR CONTROLLER

PRODUCT PREVIEW

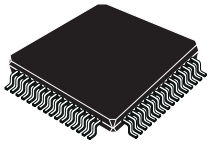
- 12V OPERATION
- 3A, THREE-PHASE DMOS OUTPUT (TOTAL R_{dson} 0.52Ω)
- NO HALL SENSORS REQUIRED
- DIGITAL BEMF PROCESSING
- LINEAR OR PWM CONTROL
- STAND ALONE OR EXT. DRIVER
- SHOOT-THROUGH PROTECTION
- THERMAL SHUTDOWN



PLCC44



PQFP44



TQFP64

ORDERING NUMBERS: L6238S (PLCC44)
L6238SQA (PQFP44)
L6238SQT (TQFP64)

DESCRIPTION

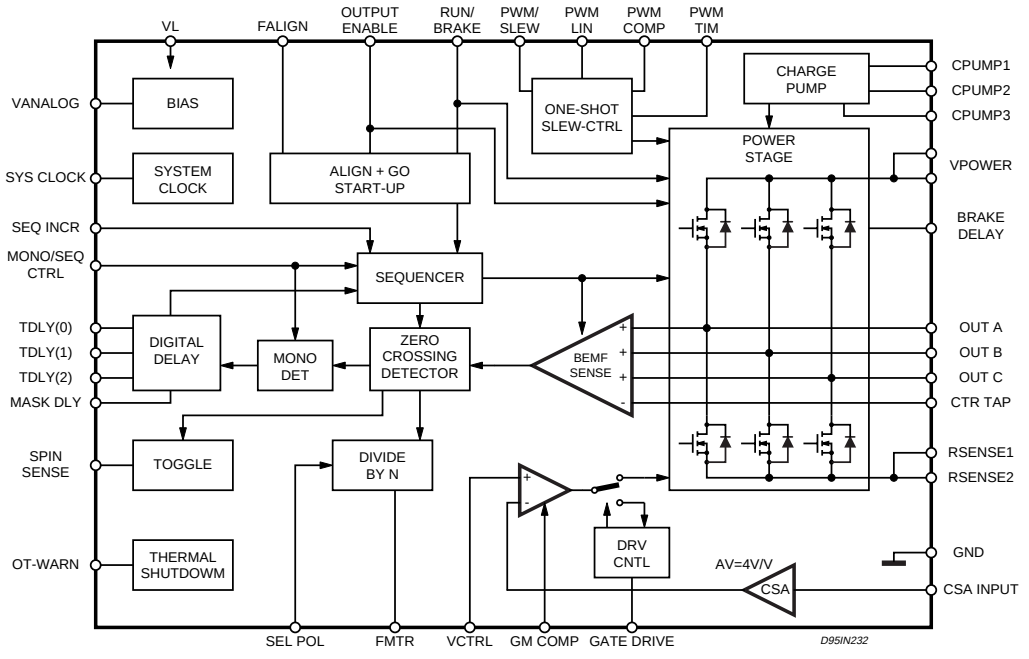
The L6238S is a Three-Phase, D.C. Brushless Spindle Motor Driver system. This device features both the Power and Sequence Sections.

Higher Power Applications can be activied with the addition of an external Linear Driver, or by operating the Internal Drivers in PWM.

Motor Start-Up, without the use of Hall Sensors, can be achieved either by an internal start-up algorithm or by manually sequencing the Output Drivers, using a variety of User-Defined Start-UP Algorithms.

Protection features include Stuck Rotor\Backward Rotation Detection and Automatic Thermal Shutdown.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

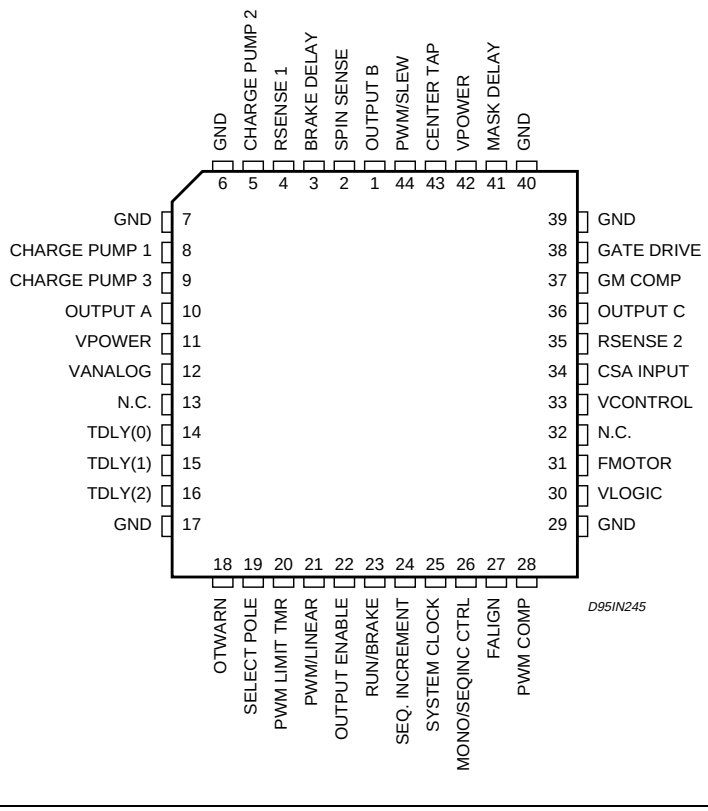
Symbol	Parameter	Value	Unit
BV_{dss}	Output Brakdown Voltage	17	V
V_{Power}	Motor Supply Voltage	15	V
V_{Logic}	Logic Supply Voltage	7	V
V_{Analog}	Analog Supply Voltage	15	V
V_{in}	Input Voltage	-0.3 to 7	V
$C_{storage}$	Charge Pump Storage Capacitor	4.7	µF
I_{mdc}	Motor Current (DC) (TQFP64 only) (PLCC44 and PQFP44)	3 2.5	A A
I_{mpk}	Peak Motor Current (Pulsed: T_{on} = 5ms, d.c. = 10%)	5	A
P_{tot}	Power Dissipation at Tamb = 50 °C (PLCC44) (TQFP64) (PQFP44)	2.3 1.7 1.3	W W W
Ts	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

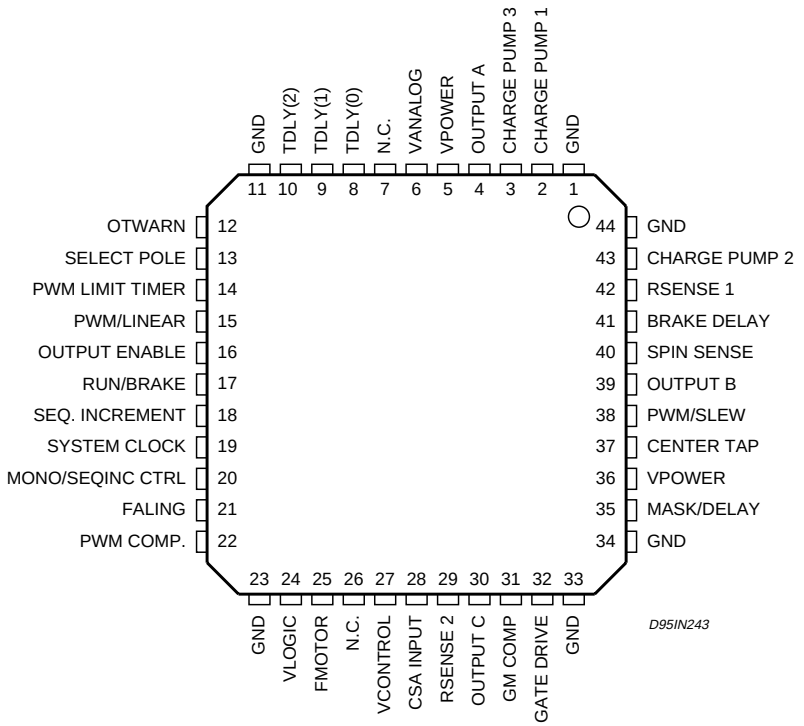
Symbol	Parameter	PLCC44	PQFP44	TQFP64	Unit
$R_{th\ (j\text{-}amb)}$	Thermal Resistance Junction-Ambient	34	45	45	°C/W

Those Thermal Data are valid if the package is mounted on Mlayer board in stillair

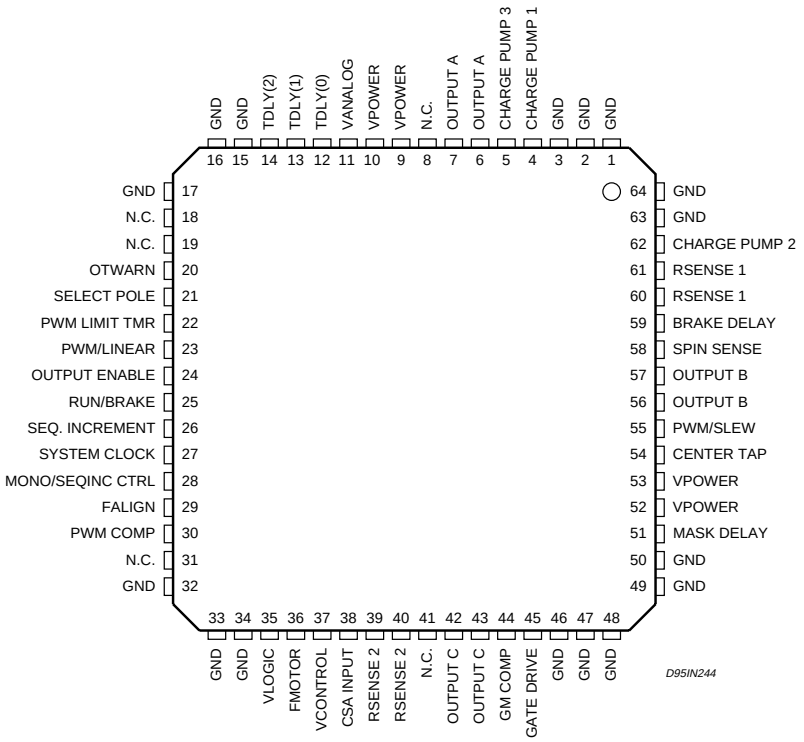
PIN CONNECTION PLCC44 (Top view)



PIN CONNECTION PQFP44 (10x10) (Top view)



PIN CONNECTION TQFP64 (Top view)



PIN FUNCTIONS

PLCC44	PQFP44	TQFP64	Name	I/O	Function
1	39	56, 57	OUTPUT B	I/O	DMOS Half Bridge Output and Input B for Bemf sensing.
2	40	58	SPIN SENSE	O	Toggless at each Zero Crossing of the Bemf.
3	41	59	BRAKE DELAY	I	Energy Recovery time constant, defined by external R-C to ground.
4	42	60, 61	$R_{sense\ 1}$	O	Outputs A+B connections for the Motor Current Sense Resistor to ground
5	43	62	CHARGE PUMP 2	I	Negative Terminal of Pump Capacitor.
6, 7, 17, 29, 39, 40	1, 11, 23, 33, 34, 44	*	GROUND	S	Ground terminals.
8	2	4	CHARGE PUMP 1	I	Positive terminal of Pump Capacitor.
9	3	5	CHARGE PUMP 3	O	Positive terminal of Storage Capacitor.
10	4	6, 7	OUTPUT A	I/O	DMOS Half Bridge Output and Input A for Bemf sensing.
11, 42	5, 36	9, 10, 52, 53	V_{power}	S	Power Section Supply Terminal.
12	6	11	V_{analog}	S	12V supply.
13, 32	7, 26	8, 18, 19, 31, 41	N.C	N.C	Open Terminal
14	8	12	Tdly(0)	I	Three bits that set the Delay between the detection of the Bemf zero crossing, and the commutation of the next Phase.
15	9	13	Tdly(1)	I	
16	10	14	Tdly(2)	I	
18	12	20	OTWARN	O	Overtemperature Warning Output
19	13	21	SELECT POLE	I	Selects # of Motor Poles. A zero selects 8, while a one selects 4 poles.
20	14	22	PWM TIMER	I	Capacitor connected to this pin sets the maximum time allowed for 100% duty cycle during PWM operation
21	15	23	PWM/LINEAR	I	Selects PWM or Linear Output Current Control
22	16	24	OUTPUT ENABLE	I	Tristates Power Output Stage when a logic zero.
23	17	25	SEQUENCE	I	Rising edge will initiate start-up. A Braking rountine is started when this input is brought low.
24	18	26	SEQ INCREMENT	I	A low to high transition on this pin increments the Output State Sequencer.
25	19	27	SYSTEM CLK	I	Clock Frequency for the system timer/counters.
26	20	28	MONO/SEQ. INC. CONTROL	I	A logic one will disable the Monotonicity Detector and Sequence Increment functions.
27	21	29	Falign	I	Reference Frequency for the opt. Auto-Start Algorithm. If int. start up is not used, this pin must be connected to the System Clock.
28	22	30	PWM COMP	O	Output of the PWM Comparator
30	24	35	Vlogic	S	5V Logic Supply Voltage.
31	25	36	Fmotor	O	Motor Once-per-Revolution signal.
33	27	37	Vcontrol	I	Voltage at this input controls he Motor Current
34	28	38	CSA INPUT	I	Input to the Current Sense Amplifier.
35	29	39, 40	Rsense 2	O	Output C connection for the Motor Current Sense Resistor to ground.
36	30	42, 43	OUTPUT C	I/O	DMOS Half Bridge Output and Input C for Bemf sensing.
37	31	44	gm COMP	I	A series RC network to ground that defines the compensation of the Transconductance Loop.

PIN FUNCTIONS

PLCC44	PQFP44	TQFP64	Name	I/O	Function
38	32	45	GATE DRIVER	I/O	Drivers the Ext. PFET Gate Driver for Higher Power applications. This pin must be grounded if an external driver is not used.
41	35	51	MASK/DELAY	O	Internal Logic Signals used for production Testing
43	37	54	CENTER TAP	I	Motor Center Tap used for differential BEMF sensing.
44	38	55	PWM/SLEW	I	R/C at this input set the Linear Slew Rate and PWM OFF-Time

Figure 1: Brake Delay Timeout vs C_{brake} (R_{brake} = 1Meg)

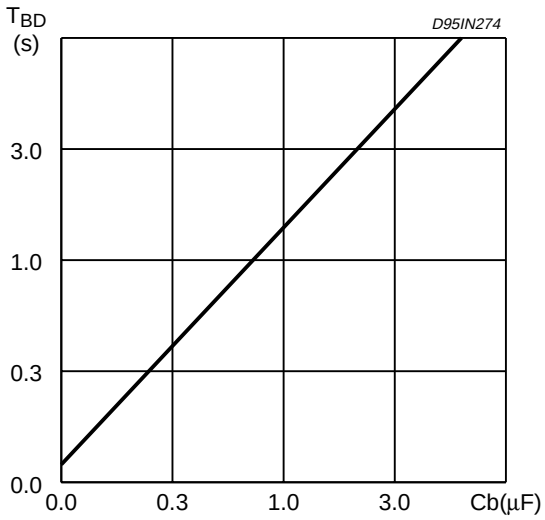


Figure 2: Linear Slew Rate vs R_{slew}

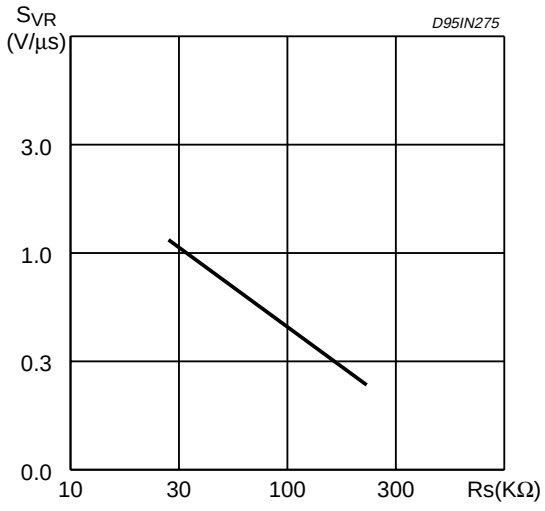


Figure 3: PWM Off - Time vs R_{slew}/C_{off}

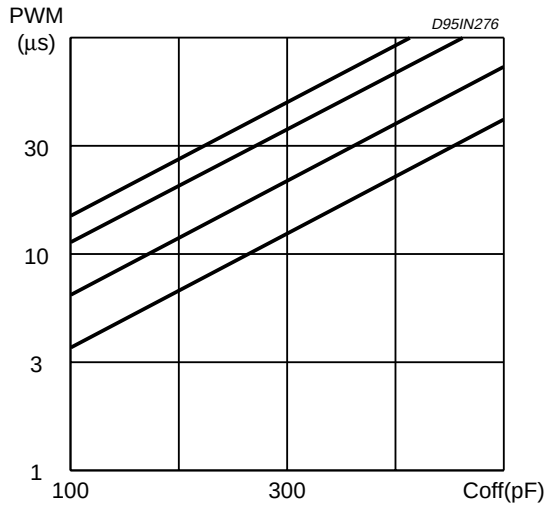
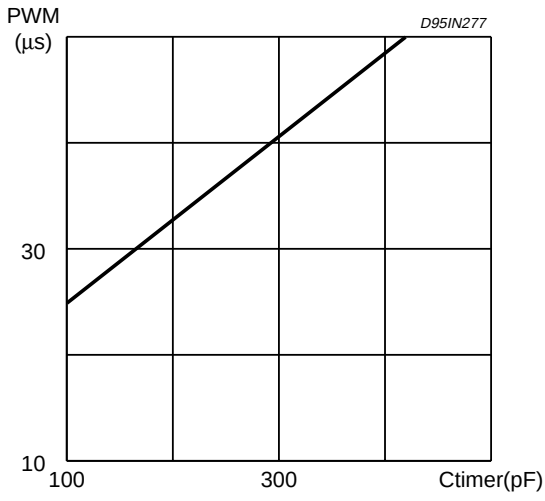


Figure 4: PWM Limit Time - Out vs C_{timer}



ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C; $V_A = V_{Pwr}$ = 12V; V_{logic} = 5V; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
GENERAL						
V_{analog}	Analog Supply Voltage		10.5		13.5	V
I_{analog}	Analog Supply Current	Run Mode V_A = 13.5V	1.5	2.7	4.5	mA
		Brake Mode V_A = 13.5V		280	800	µA
V_{logic}	Logic Supply Voltage		4.5	5.0	5.5	V
I_{logic}	Logic Supply Current	Run Mode V_{logic} = 5.5V	1	2	3.2	mA
		Brake Mode	100	500	1000	µA
THERMAL SHUTDOWN						
* T_{sd}	Shut Down Temperature		150		180	°C
* T_{hys}	Recovery Temperature Hysteresis			30		°C
* T_{ew}	Early Warning Temperature			T_{sd}-25		°C
POWER STAGE						
$R_{DS(on)}$	Output ON Resistance per FET	T_j = 25°C; V_A = 10.5V T_j = 125°C; V_A = 10.5V		0.20	0.26 0.40	Ω Ω
$I_{o(leak)}$	Output Leakage Current	V_{pwr} = 15V			1	mA
V_F	Body Diode Forward Drop	I_m = 2.0A			1.5	V
dVo/dt	Output Slew Rate (Linear)	R_{slew} = 100KΩ	0.15	0.30	0.45	V/µs
	Output Slew Rate (PWM)		10		150	V/µs
I_{gt}	Gate Drive for Ext. Power DMOS	$V_{control}$ = 1V; V_{sns} = 0V; V_A = 10.5V	4.5			mA
$V_{Gate\text{-}Drive}$	Ext Driver Disable Voltage			0.7		V
$V_{Ctrl\text{-}Range}$	Voltage Control Input Range		0		5.0	V
$I_{in(VCtrl)}$	Voltage Control Input Current				10	µA
PWM OFF-TIME CONTROLLER (R_{slew} = 100KΩ, C_{off} = 120pF)						
T_{off}	OFF Time		9	11	14	µs
V_{chrg}	Capacitor Charge Voltage	V_A = 10.5V	2.31	2.65	3.1	V
V_{trip}	Lower Trip Threshold			1.25		V
PWM LIMIT TIMER						
I_{chrg}	Capacitor Charge Current	$V_{PWM\ Timer}$ = 0V; V_A = 10.5V	10.0	20.0	30	µA
V_{chrg}	Capacitor Charge Voltage	V_A = 10.5V	3.0	3.5	4.0	mV
V_{trip}	Lower Trip Threshold			100	400	V
BEMF AMPLIFIER						
Z_{inCT}	Center Tap Imput Impedance		20	30	40	KΩ
V_{Bemf}	Minimum Bemf (Pk-Pk)		60			mV
CURRENT SENSE AMPLIFIER						
I_{snsin}	Input Bias Current	V_A = 13.5V			10	µA
G_v	Voltage Gain		3.8	4.0	4.2	V/V
SR	Slew Rate		0.33	0.8		V/µs

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BRAKE DELAY						
V_{chrg}	Capacitor Charge Voltage	R_T = 50K	8.8	9.6	10.5	V
I_{in}	Input Current	V_{in} = 5.0V			500	nA
I_{out3}	Source Current	V_A = 10.5V	0.5			mA
V_{Thres}	Delay Timer Low Trip Threshold		1.2	1.8	2.8	V
CHARGE PUMP						
V_{out}	Storage Capacitor Output Voltage	V_A = 10.5V; I_{out} = 500µA	17			V
F_{cp}	Charge Pump Frequency		140		450	KHz
I_{in}	Vstorage Input Current (Run Mode)	$V_{storage}$ = 12V; V_A = V_{logic} = 0			25	µA
I_{brkdly}	Vstorage Leakage Current (Brake Delay Mode)	$V_{storage}$ = 12V; V_A = V_{logic} = 0		0.4	1	µA
I_{brake}	Vstorage Leakage Current (Brake Mode)	$V_{storage}$ = 12V; V_A = V_{logic} = 0		0.1	1	µA
SEQUENCE INCREMENT						
t_{seq}	Time Between Rising Edges		1			µs
OUTPUT TRANSCONDUCTANCE AMPLIFIER Note: Measure at OTA Comp. pin.						
V_{oh}	Voltage Output High	V_A = 10.5V	10			V
V_{outL}	Output Voltage				2.0	V
I_{source}	Output Voltage			40.0	0.5	V
I_{sink}	Output Sink Current			40.0		µA
LOGIC SECTION						
V_{inH} V_{inL}	Input Voltage (All Inputs Except Run/Brake	V_{logic} = 4.5 to 5.5V	3.5		 1.5	V V
V_{inH} V_{inL}	Run/Brake Input Voltage	V_{logic} = 4.5 to 5.5V	2.0		 1.0	V V
I_{inH} I_{inL}	Input Current		 -1.0		1.0	µA mA
V_{outL} V_{inL}	Output Voltage	Vsink = 2.0mA V_{source} = 2.0mA	 4.5		0.5	V V
F_{sys}	System Clock Frequency		8.0		12.0	MHz
t_{off}/t_{on}	Clock ON/OFF Time		20			ns

Phase Delay Truth Table

Tdelay (2)	Tdelay (1)	Tdelay (0)	Commutation Phase Delay, in Electrical Degrees
1	0	1	2.0
1	0	0	9.4
1	1	1	18.80
1	1	0	20.68
0	0	1	22.56
0	0	0	24,44 (*)
0	1	1	26.32
0	1	0	28.20

(*) Input Default

FUNCTIONAL DESCRIPTION

1.0 INTRODUCTION

1.1 Typical Application

In a typical application, the L6238S will operate in conjunction with the L6244 Voice Coil Driver as shown in Fig. 1-1.
This configuration requires a minimum amount of external components.

1.2 Input Default States

Figure 1-2 depicts the two possible input structures for the logic inputs. If a particular pin is not

Figure 1-1

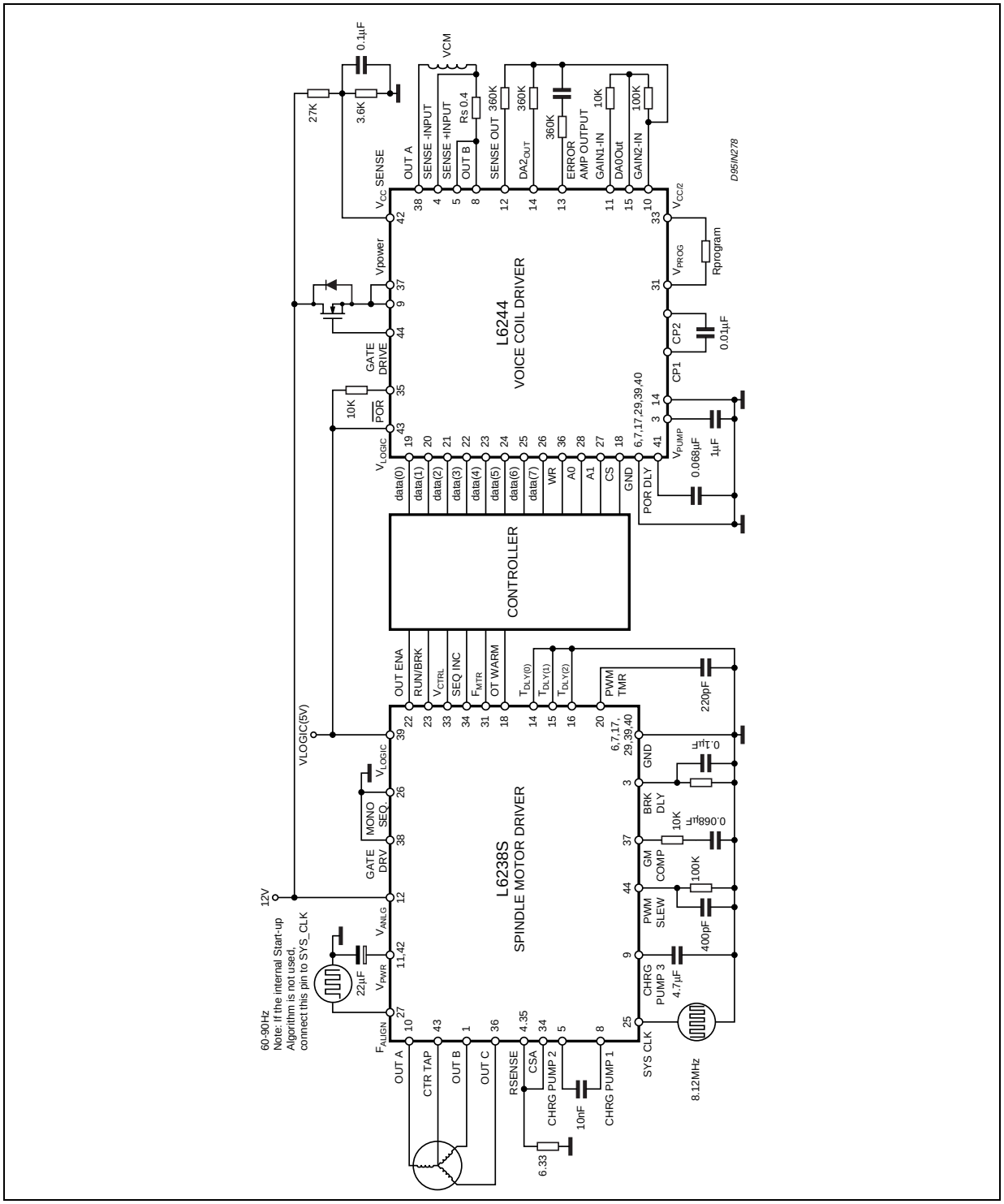
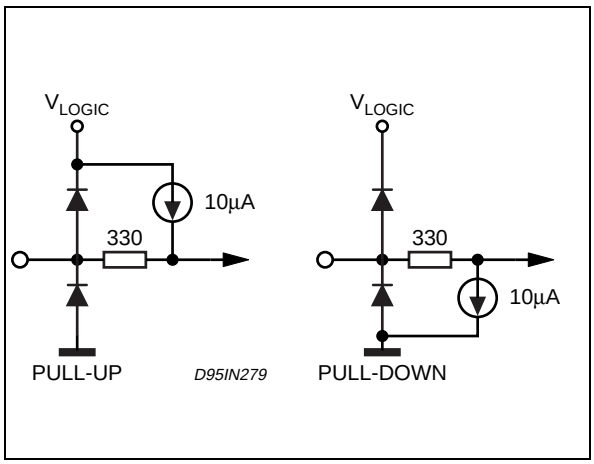


Figure 1-2



used in an application, it may either be connected to ground or VLOGIC as required, It may also be simply left unconnected.

If no connection is made, the pin is either pulled high or low by internal constant current generators as shown above.

A listing of the logic and clock inputs is shown in Table 1 with the corresponding default state.

Table 1

Pin Function	Configuration
Tdly (0,1,2)	Pull-Down
Select Pole	Pull-Down
PWM/Linear	Pull-Down
Output Enable	Pull-Down
Run/Brake	Pull-Up
Sequence Increment	Pull-Down
System Clock	Pull-Up
Faling	Pull-Up

1.3 Modes of Operation

There are 5 basic modes of operation.

1) **Tristate**

When **Output Enable** is low, the output power drivers are tristated.

2) **Start-Up**

With **Output Enable** high, bringing **Run/Brake** from a low to a high will energize the motor and the system will be driven by the Fully-Integrated StartUp Algorithm.
A user-defined Start-Up Algorithm, under control of a MicroProcessor, can also be achieved via the sequence increment input.

3) **Run**

Run mode is achieved when the motor speed (controlled by the external microprocessor) reaches the nominal speed.

4) **Park**

When **Run/Brake** is brought low, energy to park the heads may be derived from the rectified Bemf. The energy recovery time is a function of the Brake Delay Time Constant. In this state, the quiescent current of the device is minimized (sleep mode).

5) **Brake**

After the Energy Recovery Time-Out, the device is in Brake, with all lower Drivers in full conduction.

There are two mutually exclusive conditions which may be present during the Tristate Mode (wake up):

a)the spindle is stopped.
b)the system is still running at a speed that allows for resynchronization.

In order to minimize the ramp up time, the microcontroller has the possibility to:

- check the SPIN SENSE pin, (which toggles at the Bemf zero crossing frequency)
- enable the power to the motor based on the previous information. Otherwise the µP may issue a Brake command, followed by the start-up procedure after the motor has stopped spinning.

2.0 STATE DIAGRAMS

2.1 State Diagram

Figure 2-1 is a complete State Diagram of the controller depicting the operational flow as a function of the control pins and motor status. The flow can be separated into four distinct operations.

2.2 Align + Go

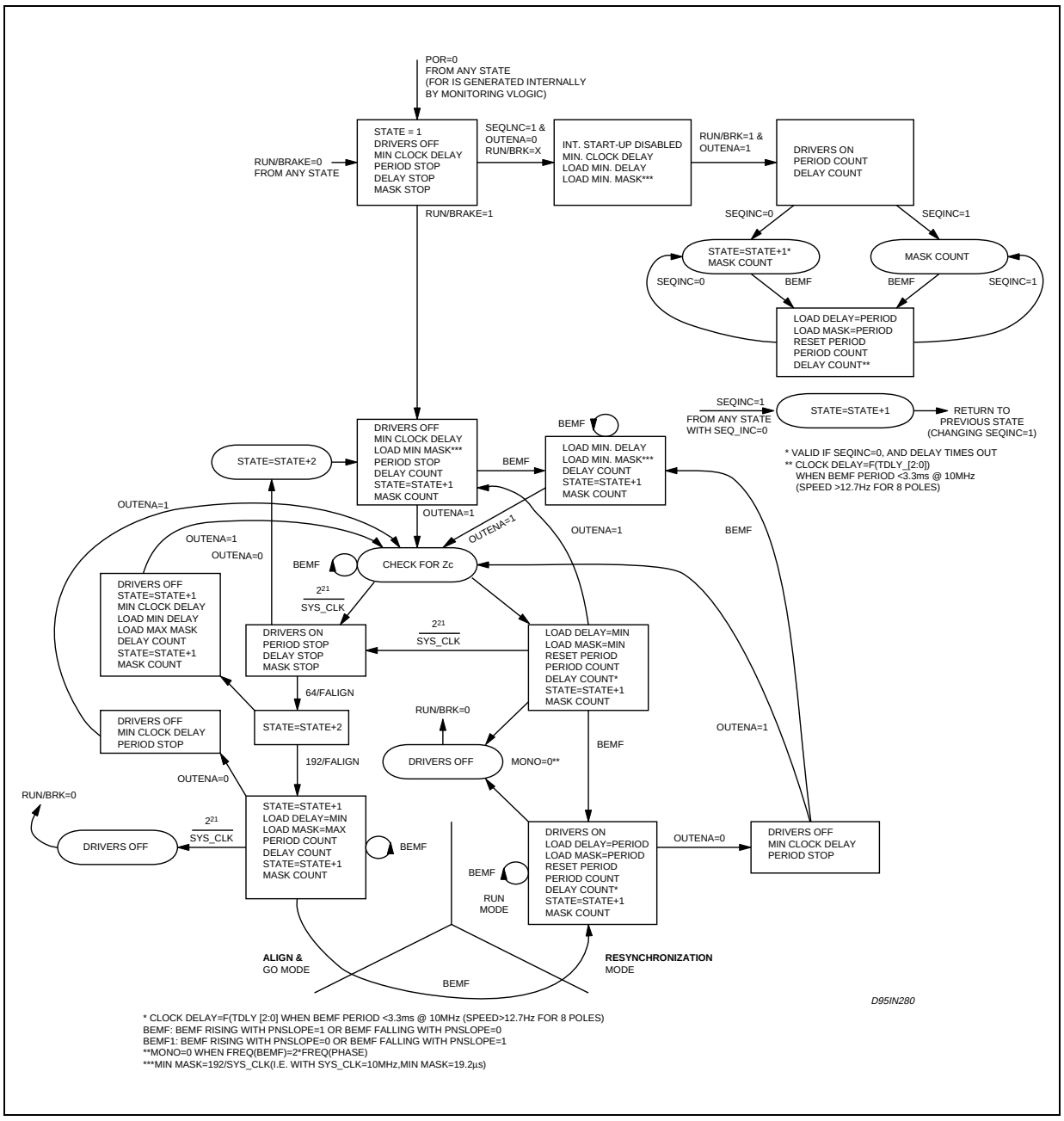
Figure 2-2 represent the normal flow that will achieve a spin-up of the spindle motor using the internally generated start up algorithm.

Upon power up, or from any state with **Run/Brake** low the controller first sets the state machine for State=1 with the Outputs Tristated.

The period counter that monitors the time between zero crossing is stopped, analog with the phase and mask delay counters.

When **Run/Brake** is brought high, the motor is in the first part of the align mode at State 2 **(Output A** high and **Output C** low). If **Output Enable** is high, the controller first checks to determine if the motor is still spinning for a time of 21Ω (with Sys_Clk = 10MHz). The drivers are now enabled and after the align time-out, (64/Falign), the sequencer double increments the outputs to State 4 **(Output** B high and **Output** A low). The first part of this align mode is used to reduce the effects of stiction

Figure 2-1



After the next align time-out 192/Falign), the controller enters the Go mode, were the sequencer again double increments the output phase upon detection of the motor's Bemf.

The align time-out may be optimized for the application by changing the Faling reference frequency.

A Watch-Dog Timer protection feature is built into the control logic to monitor the Falign pin for a clocking signal. This circuitry, shown in Figure 2-3 will prevent start up the device if the Falign clock is not present.

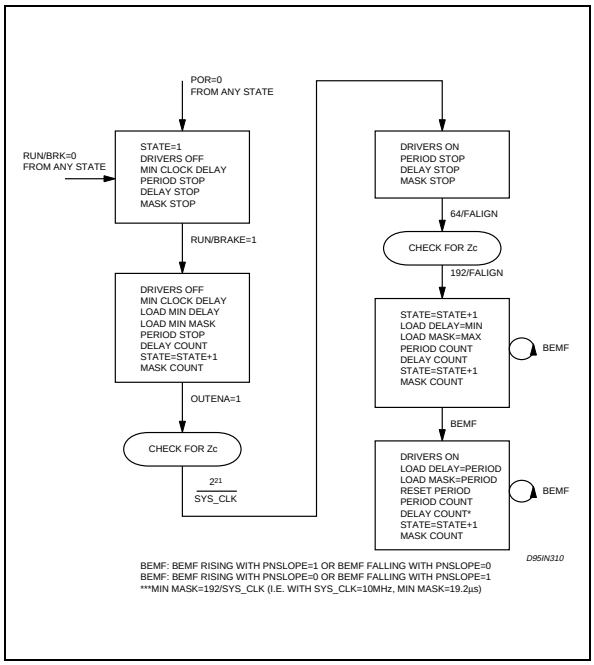
Without this feature, the output would remain in the first phase under high current conditions, if the clock were not present.

If the external sequencer is used to provide start up, the system clock may be tied to the Falign pin to satisfy the requirements of the Watch-Dog Timer.

2.3 Resynchronization

If power is momentarily lost, the sequencer can automatically resynchronize to the monitored

Figure 2.2



Bemf. This resychronization can either occur whenever **Output Enable** or **Run/Brake** is first brought low then high.

Referring to figure 2-4, the "Hold for Resync" state is brought low. The controller leaves this state and enters "Start Resync" when **Output Enable** is high.

Figure 2.3: Watch-Dog Timer

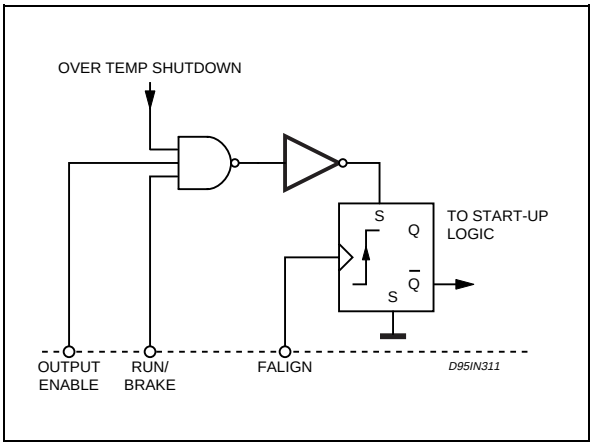


Figure 2-4

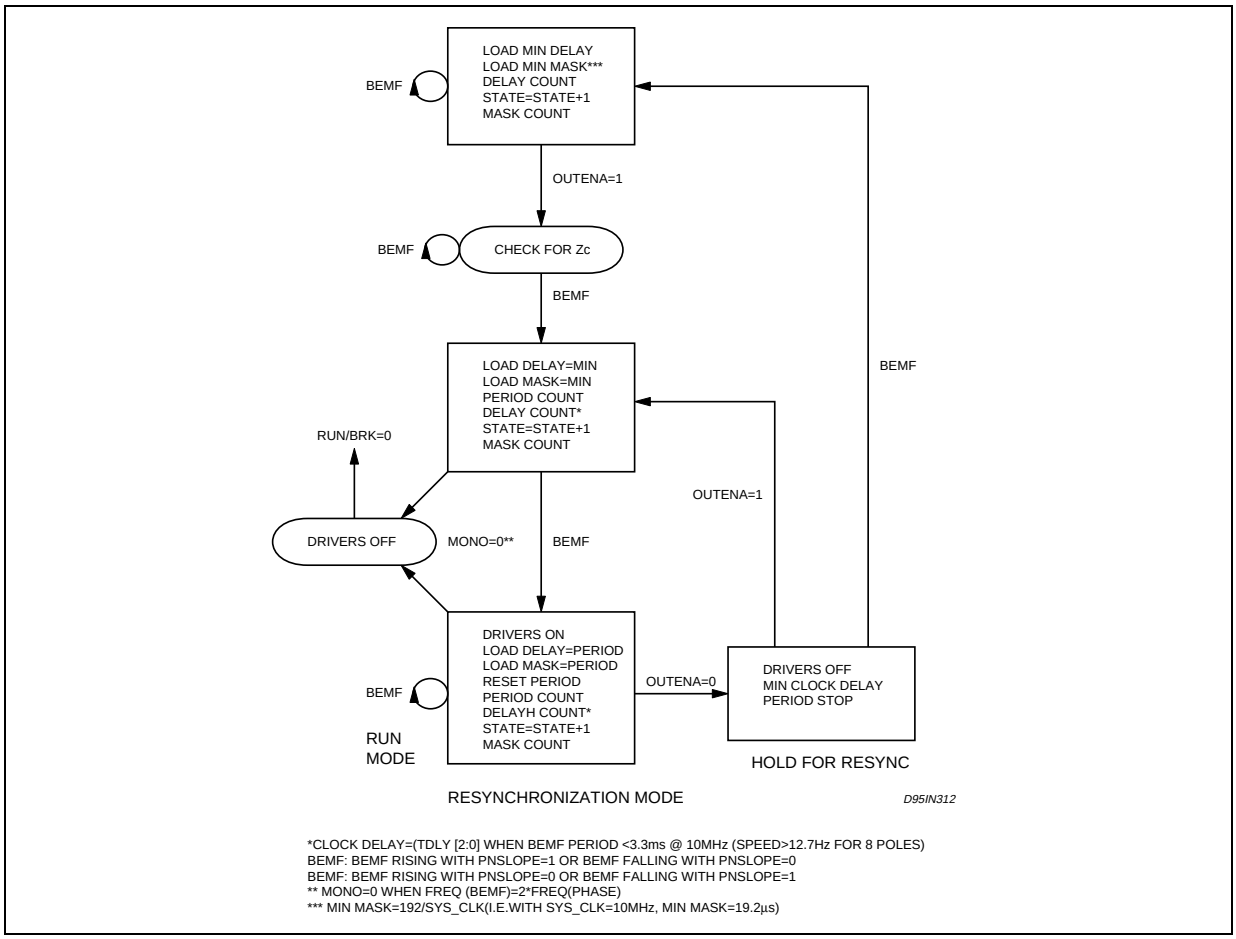
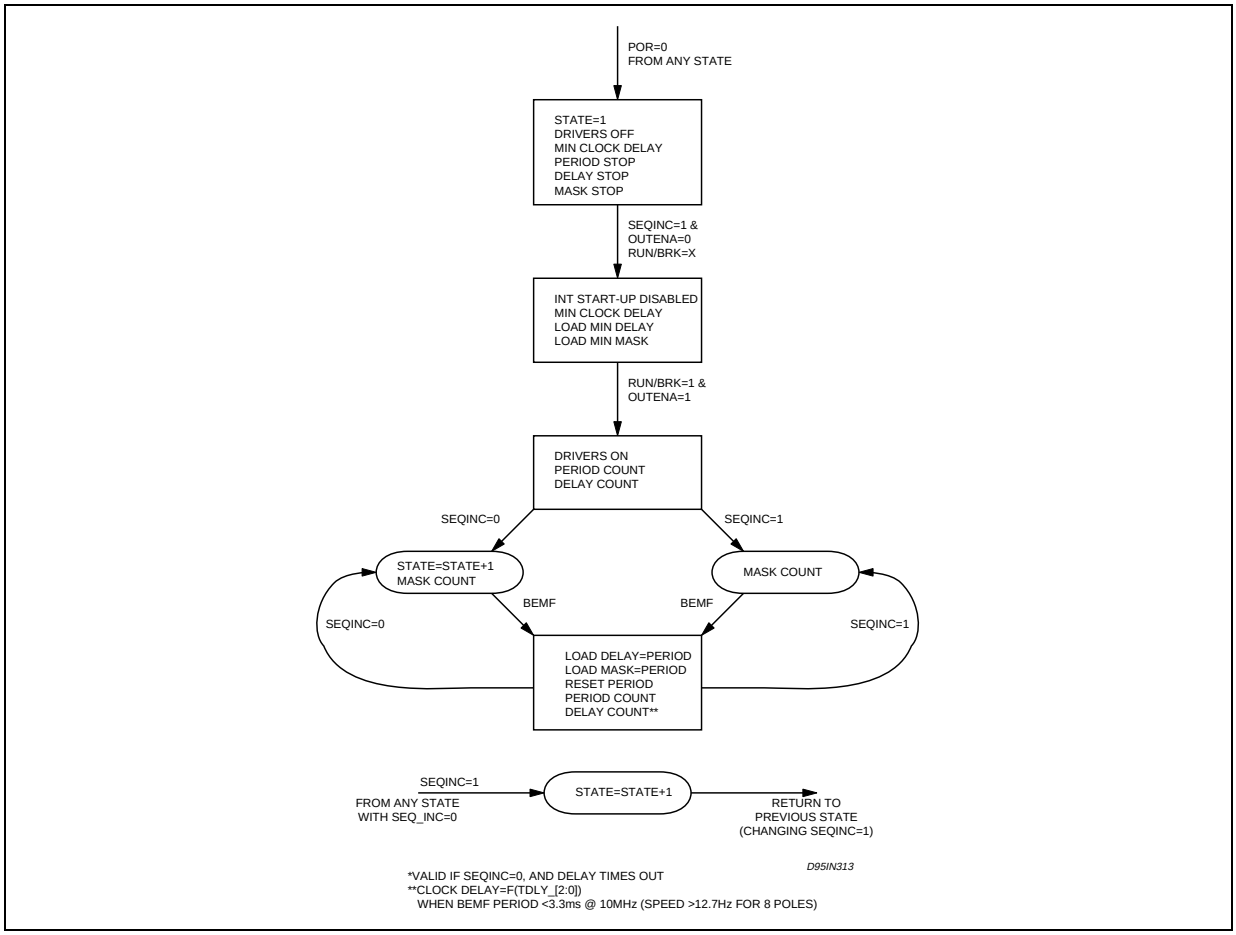


Figure 2-5



If zero crossings are detected, the sequencer will automatically lock on to the proper phase.

This resynchronization will take effect with the motor speed running as low as typically 30% of it's nominal value.

2.5 External Sequencing

Although the user-defined Start-Up Algorithm is flexible and will consistently spin up a motor with no external interaction, the possibility exists where certain applications might require complete microprocessor control of start-up.

The L6238S offers this capability via the **SEQUENCE INCREMENT** input. Referring to figure 2-5, during initial power-up with **Output Enable** low, the controller is in the "Hold and Wait for Decision" state. If the **SEQUENCE INCREMENT** pin is brought high during this state, the Auto StartUp Algorithm is disabled and the sequencer can be controlled externally.

When **Output Enable and Run/Brake** are brought high, the sequencer is incremented on each positive transition o the **SEQUENCER INCREMENT** pin. During the time that this pin is high, all Bemf information is masked out. When it is low, the Bemf information can be detected normally after the internal mask time. The minimum mask time is 192/Sys_Clk (i.e. with Sys_Clk = 10MHz, min. mask = 19.2µs) Therefore to insure that the sequencer is under complete control of the state machine, the time that the **SEQUENCE INCREMENT** pin is held low should be much less then the min. mask time, but greater then 1µs.

When the motor has reached a predetermined speed, the **SEQUENCE INCREMENT** pin can be left low and the L6238S Motor Control logic will take over and automatically spin up the motor to the desired speed

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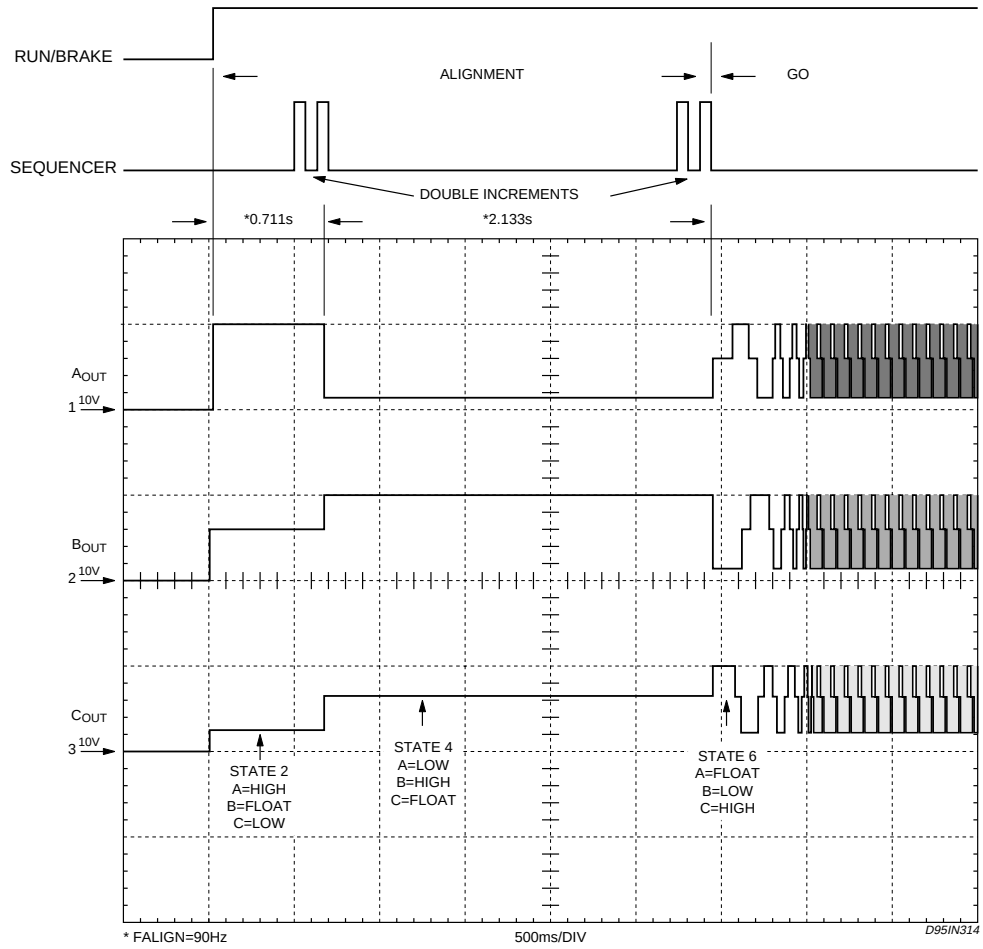
3.0 START-UP ALGORITHMS

3.1 Spin-Up Operation

The spin operation can be separated into 3 parts:

1) **Open Loop Start-Up** - The object is to create motion in the desired direction so that the Bemf voltages at the 3 motor terminals can provide reliable information enabling a transition to closed loop operation.

Figure 3-1: Align+Go



2) **Closed Loop Start-Up** - The Bemf voltage zerocrossings provide timing information so that the motor can be accelerated to steady state speed.

3) **Steady-State Operation** - The Bemf voltage zero-crossings provide timing information for precision speed control.

The L6238S contains features that offer flexible control over the start-up procedure. Either the onboard Auto-Start Algorithm can be used to control the start-up sequence or more sophisticated extenal start-up algorithms can be developed using the Serial Port and key control/sense functions brought out to pins.

3.2 Auto-Start Algorithm

When initially powered up, the controller defaults to the internal AutoStart Mode. When **Run/Brake** is low, the L6238S is in brake mode, and the Auto-Start Algorithm is reset. In the brake mode, all of the lower DMOS drivers are ON, and the upper drivers are OFF.

The Auto-Start Algorithm is based on an Align & Go approach and can be visualized by referring to Figure 3-1. Shown are the **Run/Brake** control signals, sequencer function, and the three output voltage waveforms.

Referring to figure 3-1, the following is the sequence of events during Auto-Start:

With **Output Enable** = 1, **Run/Brake** = 0

- State Machine is set to State 1 with the drivers **Trisatted**.

■ Alignment Phase (1)
Run/Brake = 1

- Output Stage is sequenced to State 2 and the drivers energized with **OUTPUT A** high and **OUTPUT C** low for 64/Falign seconds.

■ Alignment Phase (2)

- Output Stage is double sequenced to State 4 with **OUTPUT B** high and **OUTPUT A** low for

192/Falign seconds.

- During the alignment phase, the **SEQ INCREMENT** signal is ignored.

- Go Phase
  - The internal sequencer double increments the output stage to State 6, which should produce torque in the desired direction.
  - with **SEQ INCREMENT** held low, the sequencer is now controlled by the Bemf zero crossings, and the motor should ramp up to speed.

3.3 Externally Controlled Start-Up Algorithms

Enhanced Start-Up Algorithms can be achieved by using a µProcessor to interact with the L6238S.' The L6238S has the ability to transition to Closed Loop Start-Up at very low speeds, reducing the uProcessor task to monitoring status rather than real time interaction. Thus, it is a perfect application for an existing µProcessor.

The following control and status signals allow for very flexible algorithm development:

- **SEQ_INCR** A low to high transition at this input is used to increment the state of the power output stage. It is useful during start-up, because the µProcessor can cycle to any desired state, or cycle through the states at any desired rate. When held high, it inhibits the BEMF zero crossings from incrementing the internal sequencer.

- **SPIN SENSE** This output is low until the first detected Bemf zero crossing occurs. It then toggles at each successive zero crossing. This signal serves as a motion detector and gives useful timing information as well as the slope of the Bemf.

3.4 Start Up Approaches

Align & Go Approach The Align & Go approach provides a very time efficient algorithm by energizing the coils to align the rotor and stator to a known phase. This approach can be achieved via the sequencing **SEQ INCR. SPIN SENSE** can be monitored to assure that motion occurred. Once ample time is given for alignment to occur, **SEQ INCR** can be double incremented, and the **SPIN SENSE** pin can be monitored to detect motion.

When **SEQ INCR** is pulled low, control is transferred to the internal sequencer, and the L6238S finishes the spinup operation. If no motion is detected, **SEQ INCR** can be incremented to a different phase and the process can be repeated. The alignment phase may cause backward rotation, which on the average will be greater than the Stepper Motor approach.

The **Auto-Start** algorithm described earlier is an Align & Go approach. The main advantages of the integrated Auto-Start are that the µP is not involved real-time, and there are a minimum of interface pins required to the spindle control system.

Stepper Motor Approach This approach minimizes backward rotation by sequencing **SEQ INCR** at an initial rate that the rotor can follow. Thus, it is driven in a similar fashion to a stepper motor. The rate is continually increased until the Bemf voltage is large enough to reliably use the zero-crossings for commutation timing. **SEQ INCR** is held low, causing control to be passed to the L6238S's internal sequencer as in the Align & Go approach.

The Stepper Motor approach takes longer than the Align & Go approach because the initial commutation frequency and subsequent ramp rate must be low enough so that the motor can follow without slipping. This implies that to have a reliable algorithm, the initial frequency and ramp rate must be chosen for the worst case motor under worst case conditions.

4.0 MOTOR DRIVER

4.1 Output Stage

The output stage forms a 3-Phasefull wave bridge consisting of six Power DMOS FET High output currents are allowed for bbrief periods. High output currents are allowed for brief periods. Output Power exceeding the stand-alone power dissipation capabilities of the L6238S can be increased with the addition of an external P-FET or by the use of Pulse-Width-Modulation.

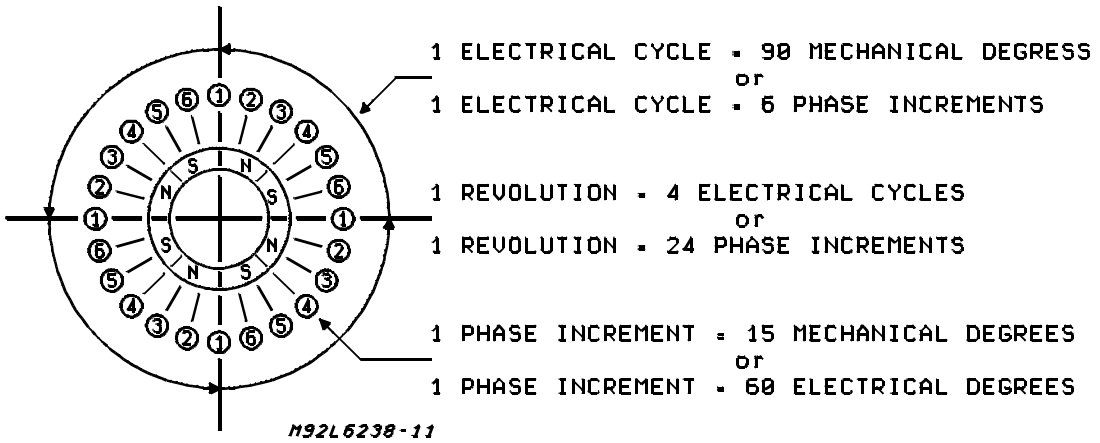
Table 4-1 is a reference diagram that lists the parameters associated with 8-pole motors operating at 3600 and 5400 RPM.

Figure 4-1 represents the waveforms associated with the output stage. The upper portion of figure 4-1 shows the flow of current in the motor windings for each of the 24 phase increments. A rotational degree index is shown as a reference along with a base line to indicate the occurrence of a zero crosing. The output waveforms are a digitally reproduced voltage signals as measured on samples.The feedback Input is multiplexed between the internal Bemf Zero Crossing Detector and an externally provided sync pulse **(EXT INDEX)**

Shown in figure 10 is the classical state diagram for a phase detector along with waveform examples.

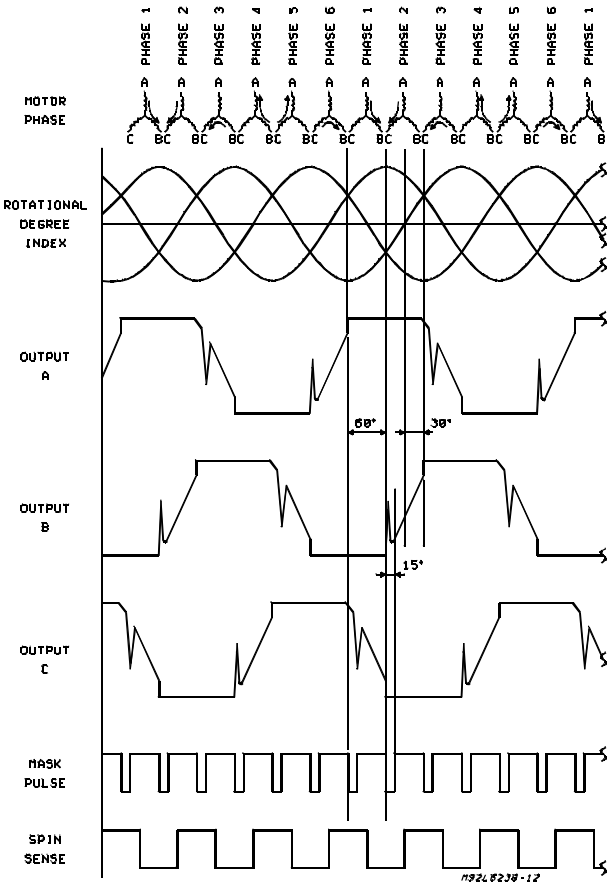
A typical sequence starts when the outputs switch states. Referring to figure 4-1, during phase 1, output A goes high, while outputB is low. During this phase, output C is floating, and the Bemf is monitored. The outputs remain in this state for 60 electrical degrees as indicated by the first set of dashed lines. After this period the out-

Table 4-1



Rotational Speed	3600rpm	5400rpm
Rotational Frequency	60Hz	90Hz
Rotational Period	16.667ms	11.111ms
Electrical Period	4.167ms	2.778ms
Phase Period	694.5µs	463.0

Figure 4-1: Waveforms



put switched to phase 2 with output A high and C low with the Bemf amplifier monitoring output B.

In order to prevent commutation current noise being detectedm as a false zero crossing, a masking circuit automatically blanks out all incoming signals as soon as a zero crossing is detected. When the next commutation occurs an internal counter starts counting down to set the time that the masking pulse remains.
The counter is initially loaded with a number that is equal to time that is always 25% of the previous phase period or 15 electrical degrees. The time-out of the masking pulse shown for reference at the bottom of figure 4-1. Thus the actual masking period is the total of the time from the detected zero crossing to the phase commutation, plus 25% of the previous period. The mask pulse operation is further discussed in section 4.6, Slew Rate Control and PWM operation.

After the masking period, the Bemf voltage at output B is monitored for a zero crossing. Upon detection of the crossing, the output is commutated after the selected phase delay insuring maximum torque. The spin sense waveform at the bottom of the figure indicates that this output signal toggles with each zero crossing.

4.2 Brake Delay

When Run/Brake is brought low, a brake is initiated. Referring to figure 4-2, SW1 is opened and the brake delay capacitor, C_{brake}, is allowed to discharge towards groun via R_{brake}.

At the same time, switches SW2 through SW7 bring the gates of the output FETs to ground halting conduction, causing the motor to coast. While the motor is coasting, the Bemf is used to park the heads. When Cbrake reaches a voltage that is below the turn ON threshold of Q1, Switches SW8, 9, and 10 bring the gates of the lower drivers to V_{brake} potential. This enables the lower FETs causing a braking action.

The analog and logic supplies are not monitored in the L6238S, since the L6244 already monitors this voltage and initiates a Park function when either supply drops to a predeterminated level.

Figure 4-2

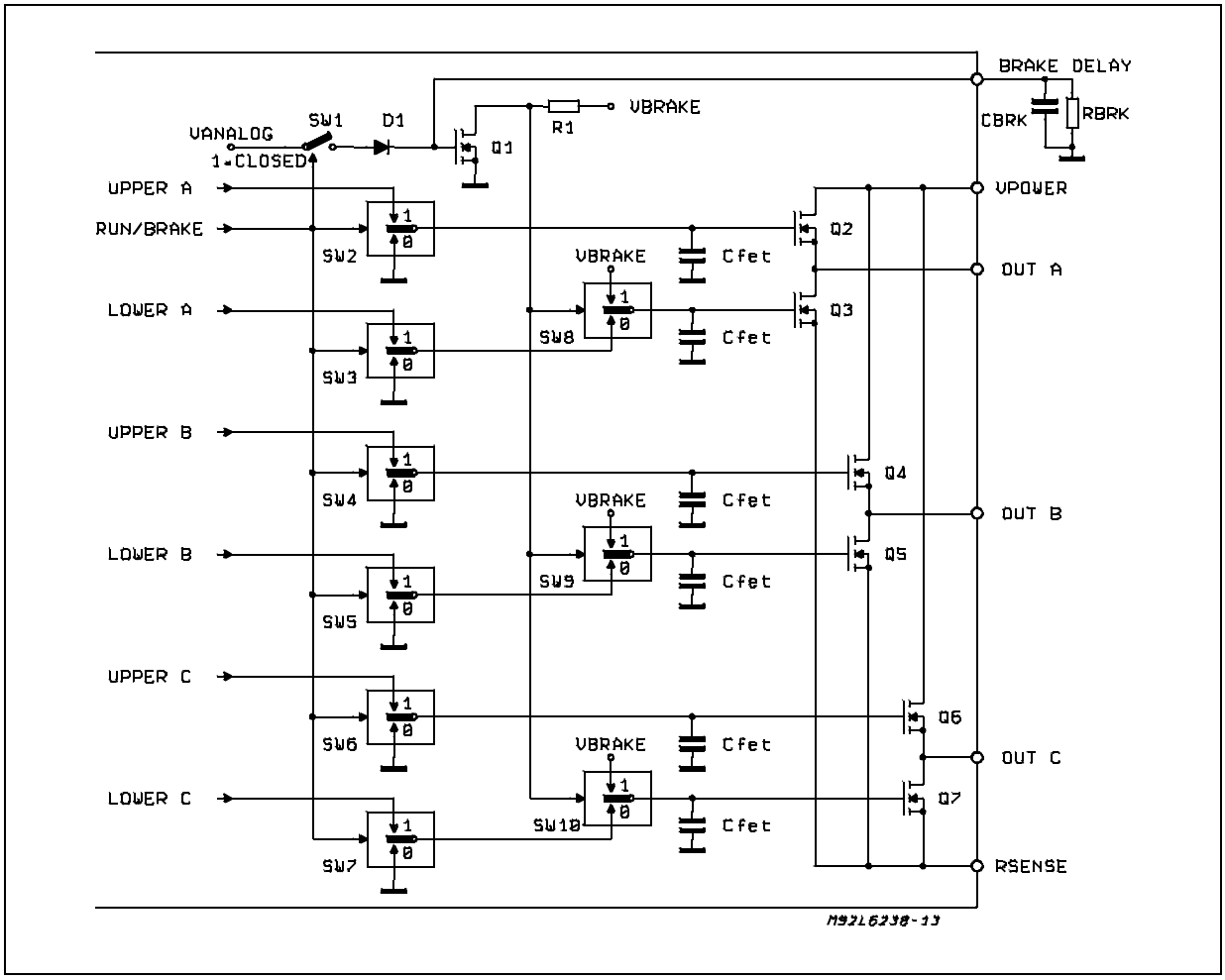
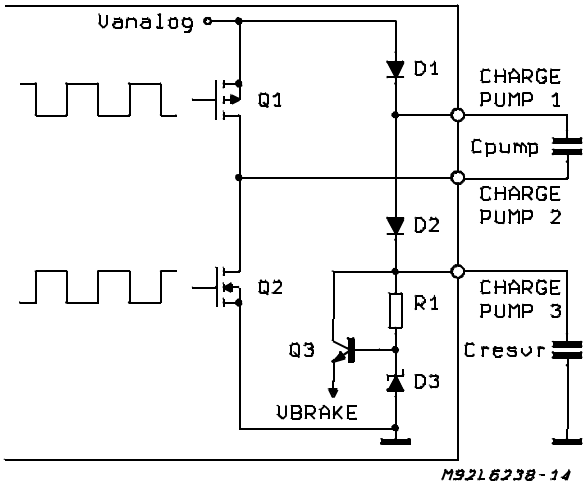


Figure 4-3



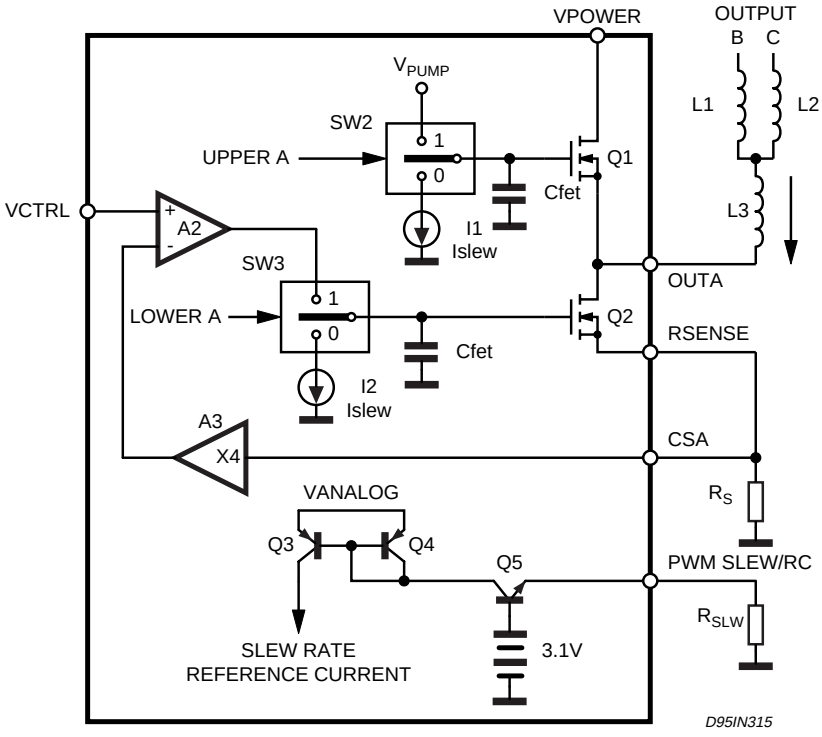
4.3 Charge Pump

The charge pump circuitry is used as a means of doubling the analog supply voltage in order to allow the upper N-channel DMOS transistors to be driven like P-channel devices. The energy stored in the reservoir capacitor is also used to drive the lower drivers in a brake mode if the analog supply is lost. Figure 4-3 is a simplified schematioc of the charge pump circuitry.

A capacitor, C_{pump}, is used to retrieve energy from the analog supply and then "pumps" it into the storage capacitor, C_{resvr}.
An internal 300KHz oscillator first turns ON Q2 to quickly charge C_{pump} to approximately the rail voltage. The oscillator then turns ON Q1 while turning OFF Q2. Since the bottom plate of C_{pump}, is now effectively at the rail voltage via D2.

A zener-referenced series-pass regulator supplies

Figure 4-4



a voltage, V_{brake}, during brake mode.

The maximum capacitance specified for the Storage Capacitor is 4.7µF.For applications requiring a larger value, an external diode should be connected between Vanalog and the Storage Capacitor to prevent excessive inrush current from damaging the charge pump circuitry. A small value resistor (i.e. 50W) may instead be inserted in series with the Storage Capacitor to limit the inrush current.

4.4 Linear Motor Current Control

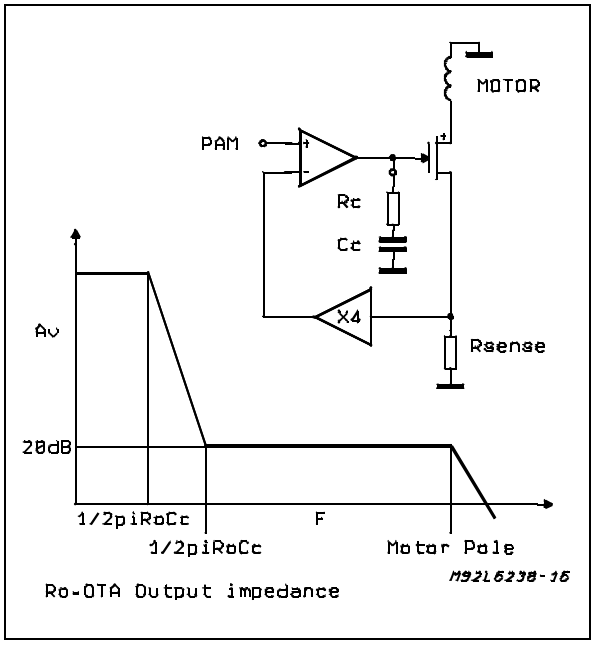
The output current is controlled in a linear fashion via a transconductance loop. Referring to Figure 4-4 the sourcing FET of one phase is forced into full conduction by connecting the gate to V_{pump}, while the sinking transistor of an appropriate phase operates as a transconductance element. To understand the current control loop, it will be assumed that Q2 in figure 4-4 is enabled via SW3 by the sequencer. During a run condition, the current in Q2 is monitored by a resistor R_S connected to the R_{sense} input.

The resulting voltage that appears across R_S is amplified by a factor of four by A3 and is sent to A2 where it is compared to the Current Command Signal. A2 provides sufficient drive to Q2 in order to maintain the motor speed at the proper level as commanded by the Speed Controller.

4.5 Transconductance Loop Stability

The RC network connected to the Compensation pin provides for a single pole/zero compensation scheme. The pole/zero compensation scheme.

Figure 4-5



The pole/zero locations are adjusted such that a few dB of gain (typ. 20dB) remains in the transconductance loop at frequencies higher than the zero.

The inductive characteristic of the load provides the pole necessary for loop stability. Thus the loop bandwidth is actually limited by the motor itself.

Figure 4-5 shows the complete transconductance loop including compensation, plus the response. The Bode plot depicts the normal way to achieve stability in the loop. The pole andzero are used to set a gain of 20dB at a higher frequency and the pole of the motor cuts the gain to achieve stability.

Loop instability may be caused by two factors:

1)The motor pole is too close to the zero. Referring to figure 4.6, the zero is not able to decrement the shift of phase, and when the effect of the pole is present, the phase shift may reach 180° and the loop will oscillate. To rectify this situation, the pole/zero must be shifted at lower frequencies by increasing the compensation capacitor.

Figure 4-6

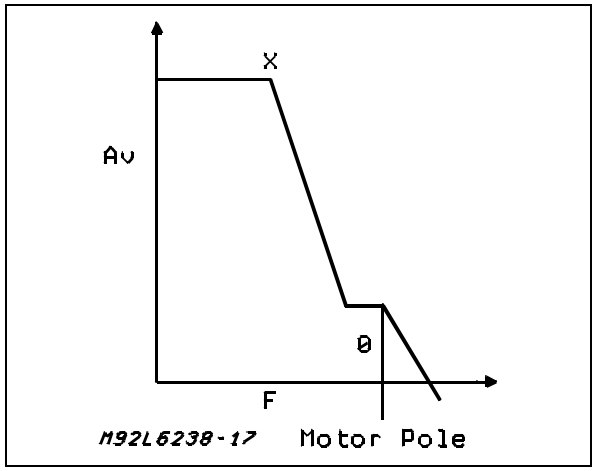


Figure 4-7

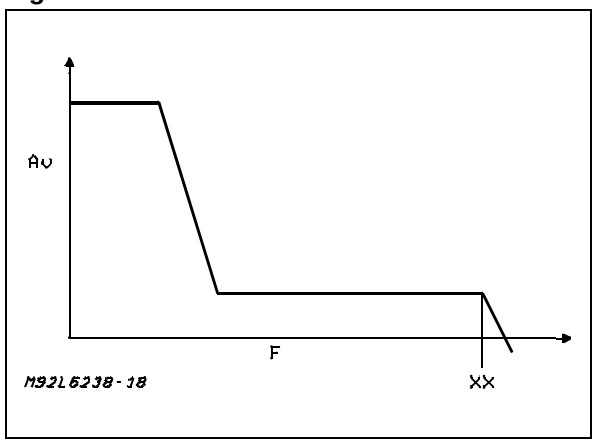
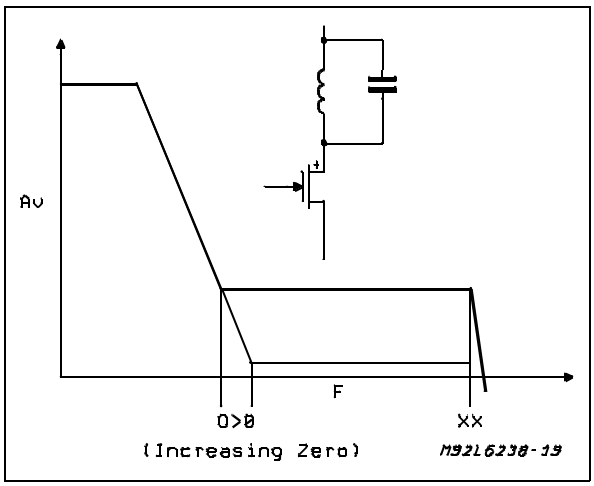


Figure 4-8



2)The motor capacitance, CM, itself can interfere with the loop, creating double poles. If the gain at higher frequencies is sufficiently high, the double pole slope of 40dB/decade can cause the phase shift to reach 180°, re sulting in oscillation.

Figure 4-8 is a Bode plot showing how to correct this situation. The bold line indicates the response with relatively high gain at the higher frequencies. By leaving the pole unchanged and increasing the zero, the response indicated by the dashed lines can be achieved.

4.6 Slew Rate Control

A 3-phase motor appears as an inductive load to the power supply. The power supply sees a disturbance when one motor phase turns OFF and another turns ON because the FET turn-OFF time is much shorter than the L/R rise time. Abrupt FET turn-OFF without a proper snubbing circuit can even cause current recirculation back into the supply.
However, the need for a snubber circuit can be eliminated by controlling the turn-OFF time of the FETs.

The rate at which the upper and lower drivers turn OFF is programmable via an external resistor, S_{slew} connected to the **SLEW RATE** pin. This resistor defines an internal current source that is utilized to limit the voltage slew rate at the outputs during transition, thus minimizing the load change that the power supply sees.

To insure proper operation the range of resistor values indicated should not be exceeded and in some applications values near the end points should be avoided as discussed below.

Low Values of Rslew - If a relatively low value of Rslew is selected, the resultant fast slew rate will result in increased commutation cross-over current, higher EMI, and large amount of commutation current.

This last case can cause voltage spikes at the output that can go as much as IV below ground level. This situation must be avoided in this integrated circuit (as in most) since it causes unpredictable operation.

High Values of Rslew - Higher values of Rslew result of course in slow slew rates at the outputs which is, under most conditions, the desired case since the problems associated with fast rates are reduced. The additional advantage is lower acoustical noise.

Problems can occur though if the slew rate for a

Figure 4-9: Effect of Slow Slew Rate.

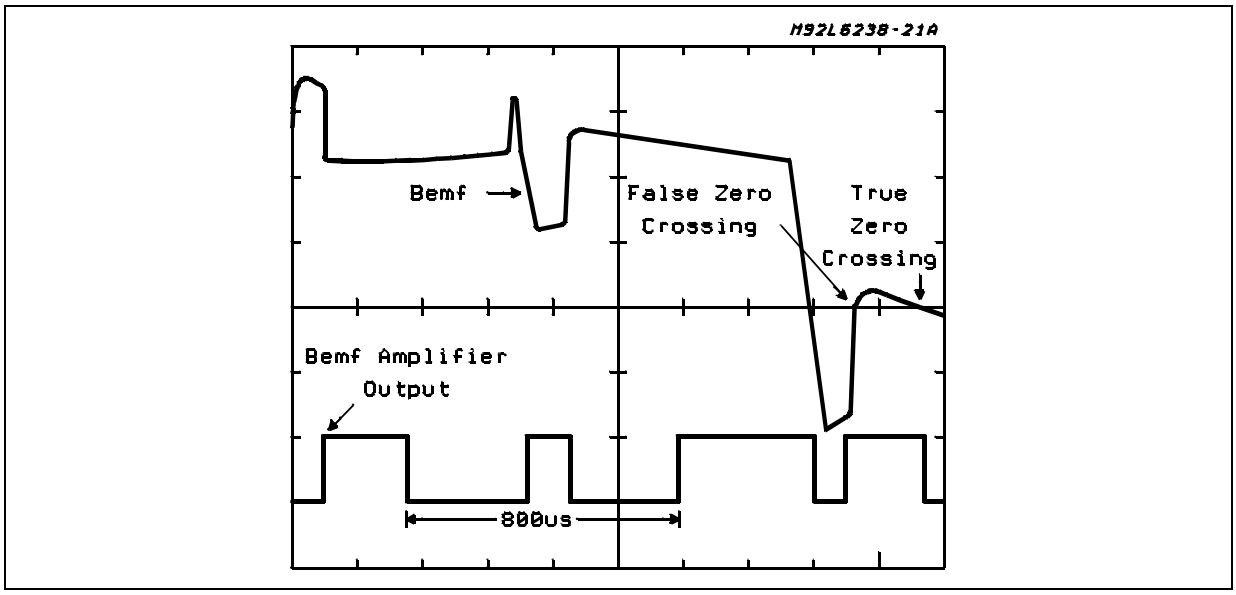
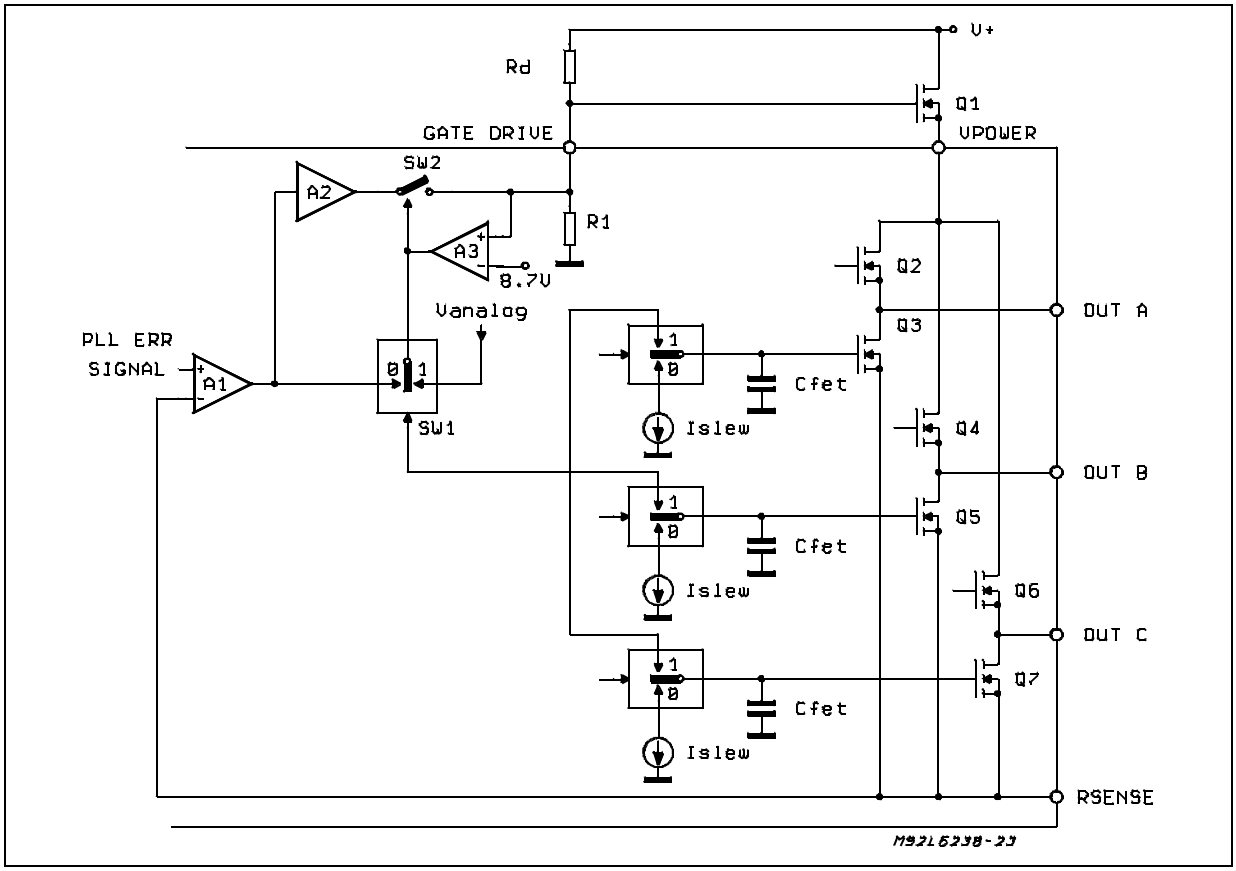


Figure 4-10: External P-Fet.



given application is too slow. Figure 4-9 is an oscillograph taken on a device that had a fairly large value for Rslew and failed to spin up and phase lock a motor.

The problem manifests itself as the motor begins to spin up. At lower RPMs, the Bemf of the motor is relatively small resulting in higher amounts of commutation current. In figure 4-9, the upper waveform is the voltage appearing at **OUTPUT** relative to the **CENTER TAP** input. The lower waveform is the actual output of the Bemf amplifier available on special engineering prototypes.

The oscillograph was taken just as the problem occured. The period between zero crossings was ~800µs resulting in a mask time period of 200µs.

As can be seen, the excessively long slew rate actually exceeded the mask period and was detected as a zero crossing.
This resulted in improper sequencing of the outputs relative to the proper phases and caused the motor to spin down.

4.7 Ext PFET Driver

The power handling capabilities of the 3 phase output stage can be extended with the addition of a single P-Channel FET.

Figure 4-10 shows the Ext FET connection and demonstrates how the L6238S automatically senses the FETs presence. When the voltage at the **Gate Drive** pin is ≥ 0.7V, the output of comparator A3 goes high, removing the variable drive A1 from the internal FETs and connects them instead to Vanalog via the commutation switches to facilitate full conduction.

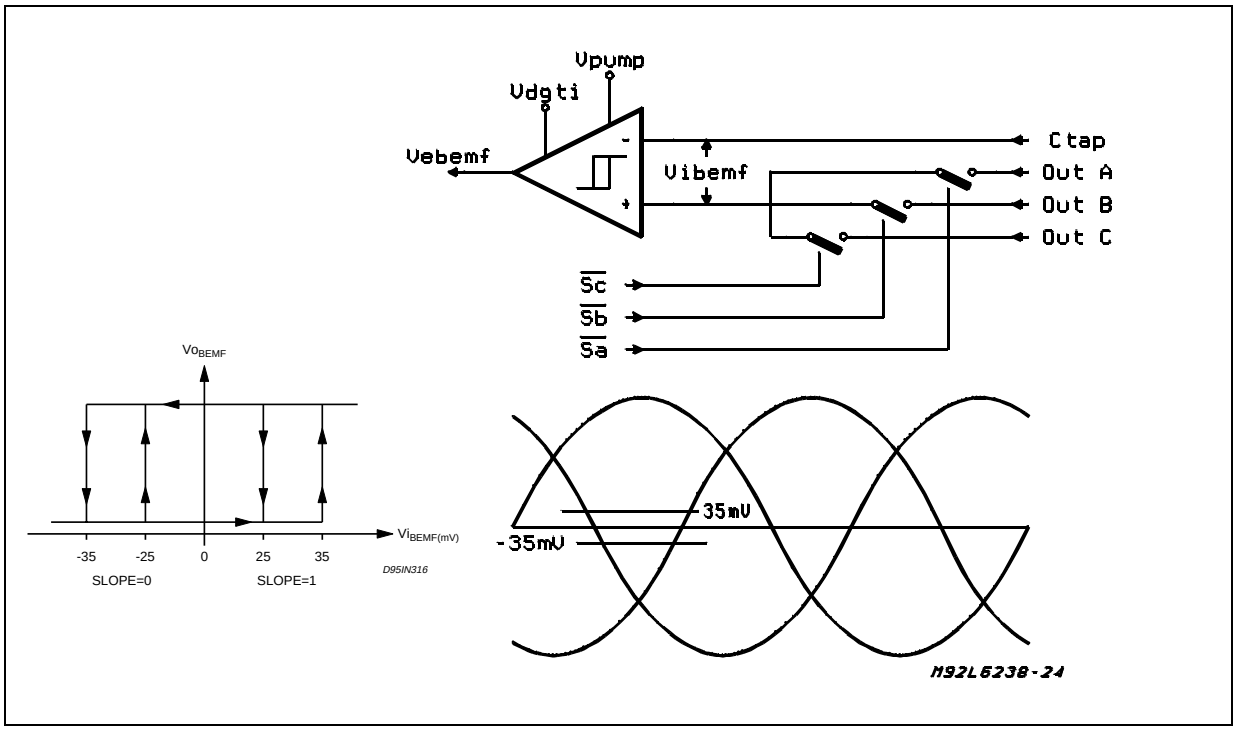
The upper FETs drive paths are not shown for clarity. A3 also closes SW2 allowing A1 to linearly drive the external P-Channel FET Q1 via inverter A2.

4.8 Bemf Ampolifier

Since no Hall Effect Sensors are required, the commutation information is derived from the Bemf voltage zero-crossings of the undriven phase with respect to the center tap. The Bemf comparator and associated signal levels are depicted in figure 4-11. For reliable operation, the Bemf signal amplitude should be a minimum of ± 60 mV to be properly detected. In order to provide for noise immunity, internal hysteresis is incorporated in the detection circuitry to prevent false zero crossing detection.

For laboratory evaluation purposes, a simple re-

Figure 4-11: Bemf Amplifier.



sistive network as shown in figure 4.12 can be used to emulate the Bemf of the motor.

The actual Bemf zero-crossing is 30 electrical degrees (50% of a commutation interval) away from the optimal switch point. A digital counter circuit measures 50% of the previous interval to determine the next interval's commutation delay from the zero crossing. During the low RPM stages of start up the long commutation intervals may cause the counter to overflow, in which case 50% of the max count will be less than 50% of the ideal commutation interval. Therefore, the torque will not be optimal until the desired commutation interval is less than the dynamic range of the counter.

4.9 Center Tap Protection

Spindle Motors with a high number of windings exhibit a transformer coupling effect that in some cases can cause relatively high currents to flow through the center tap input.

Current flowing out of the center tap pin as high as 25mA has been observed with certain motors.

Figure 4-12: Bemf Emulator

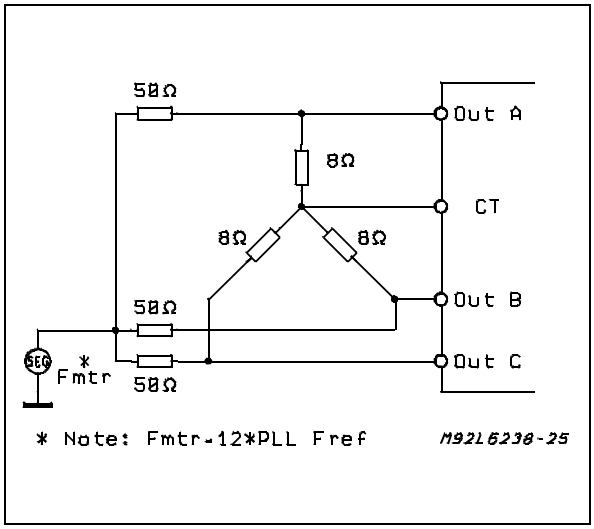
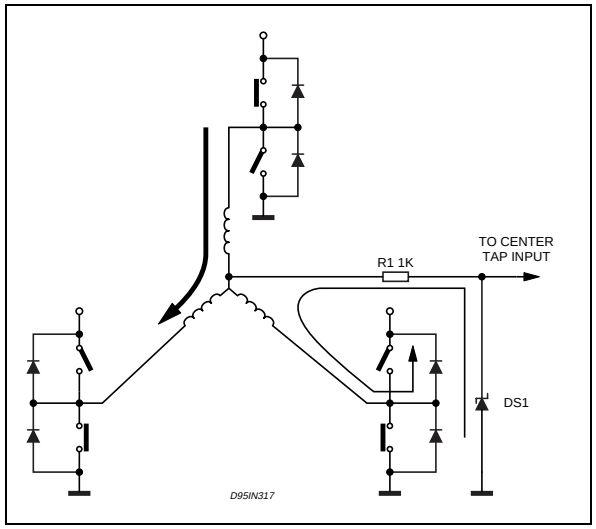


Figure 4-13



The high current flows from the grounded substrate of the integrated circuit (p-type material), through one or more epitaxial pockets (n-type material) and out the center par pin.

This current can cause adverse operation of the controllet due to substrate injection and might possibility damage the internal metalization runs. The normal current for this input is in the 200µA range.

Referring to figure 4-13, a simple protection scheme consisting of a 1K resistor and a low current Schottky diode should be added if the application causes excessive current (i.e. >1mA) to flow through the center tap pin.

5.0 PWM MOTOR CURRENT CONTROL

A unique feature of the L6238S in the optional Pulse Width Modulation (PWM) control of motor current.
Using Variable-frequency, Constant-OFF time Current-Mode control, the L6238S can drive higher power motors without the need for external drivers, while minimizing internal power dissipation.

Additional benefits include reduced power supply consumption (up to 50% savings) and lower wattage requirements for the current sensing resistor.

Constant-OFF time Current-Mode control, operates on the principle of monitoring the motor current and comparison it to a reference or control level.

When the motor current reaches this commanded level, the output drivers turn OFF and remain OFF for a Constant-OFF time. After this OFF time the drivers turn back ON to repeat the cycle.

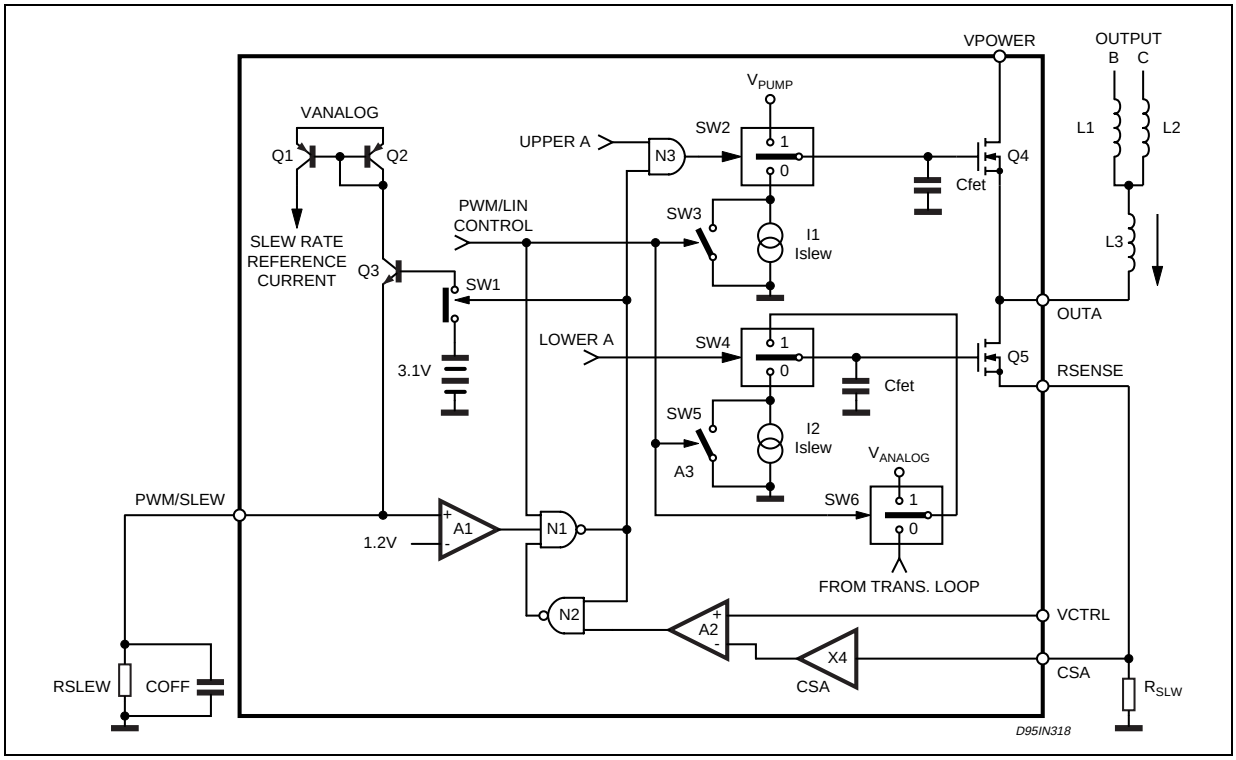
Figure 5.1 is a block diagram of the PWM control circuitry. When using PWM as opposed to linear control, two changes are made to the control loop:

1. The slew rate control is disabled, allowing the outputs to slew at a minimum rate of 10V/µs. This is accomplished by closing SW3 and SW5.
2. The OTA amplifier is taken out of the control loop via SW6. The lower drivers are now driven into hard conduction by tying the gates to the analog supply during the On time of the PWM cycle.

The current in the motor windings is monitored via the voltage dropped in the sensing resistor, R_{sense}.
This voltage is multiplied by a factor of 4 in the Current Sense Amplifier (CSA) and sent to negative input of the PWM Comparator (A2).

The control voltage, $V_{control}$, is applied to the positive input of A2. When the output of the CSA reaches a level that is equal to the commanded level, the output of A2 switches low, toggling the latch comprised of N1 and N2. This causes the upper drivers to turn off and opens SW1. Q3 turns OFF allowing the Constant-OFF time capacitors,

Figure 5-1



C_{off} to discharge to dischargte through R_{slew}, initiating the Constant-OFF time-out. When the voltage on C_{off} reaches 1.2V, comparator A1switches state toggling the latch in the opposite state, turning the upper driver back ON. SW1 also closed quickly charging up C_{off} for the next cycle.

5.1 PWM Design Considerations

In order to select the parameters associated with PWM operation, the following factors must be taken into consideration:

1. PWM Switching Frequency
2. Duty Cycle
3. Motor Currents
4. Minimum ON Time
5. Noise Blanking
6. Bemf Masking/Sampling

5.1.1. PWM Switching Frequency

The PWM switching frequency F_{pwm} is found from:

$$F_{pwm} = \frac{1}{T_{on} + T_{off}} \qquad (5.1.1)$$

where:

T_{on} = The time required for the motor current to reach the commanded level.

T_{off} = The programmed OFF time.

The two main considerations for this parameter are the minimum and maximum switching frequency.

The maximum switching frequency occurs during the Start-up and should be kept below 50KHz due tointentional bandwidth limitations and output switching losses.

5.1.2 Duty Cycle

Besides reducing the power dissipation of the controller output stage, running in PWM offers 2 additional "free" benefits:

A. Reduced Powe Supply Current at Start Up

B. Lower Power Rating for the Motor Current Sense Resistor.

Figure 5-2 is the current path during the ON time of a phase period. The current from the supply passes through the upper sourcing DMOS, Q3 transistor through the two driven winding, the lower DMOS, Q2 and finally through the current sensing resistor R_{sns}. Since both Q3 and Q4 are ON, while Q3 is turned OFF. The voltage, causing the current to continue to flow through Q2, and Q4.

If the duty cycle is nearor at 50%, then for 1/2 the PWM cycle, no current is flowing from the power supply or the sense resistor while current is still flowing in the motor. This lowers the requirement

Figure 5-2

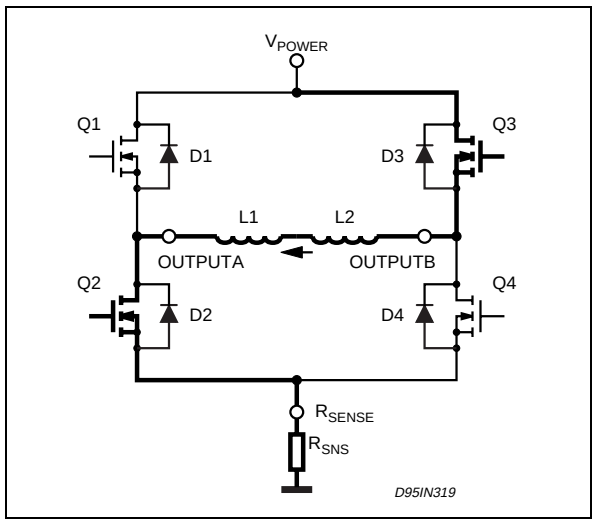
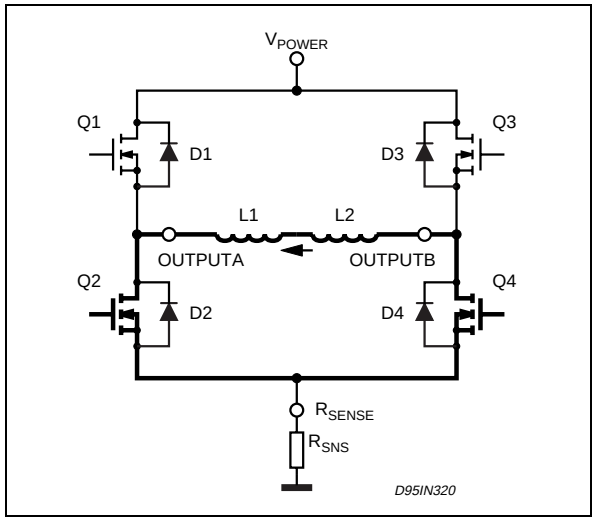


Figure 5-3



for both the Power Supply and the Power Rating for the sensing resistor.

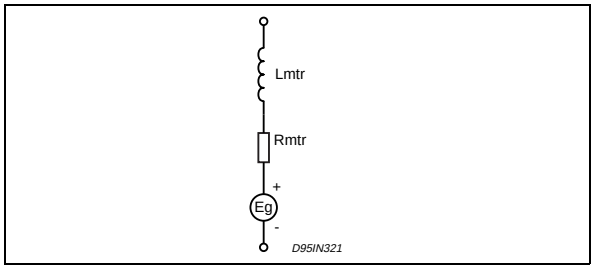
5.1.3 Motor Currents

Note: It is not the objective of this section to describe the principles of brushless DC motor, but to provide sufficient information about the parameters associated with PWM operation in order to optimize an application.

A simplified model of a motor is shown in figure 5-4. For this discussion, lower order effects due to mutual inductance between windings, resistance due to losses in the magnetic circuit, etc. are not shown.

The motor at **stall** is equal to a resistance, **Rmtr**, in series with an inductance, **Lmtr**. When the motor is rotating, there is an induced emf that appears across the armaure terminals and is shown in figure 5-4 as an internally generated voltage Ibemf), **Eg**.

Figure 5-4



The relation between these variables is given by:

$$V = L_{mtr}\frac{di_{mtr}}{dt} R_{mtr}\, i_{mtr} + E_g \qquad (5.1.2)$$

where:

V	=	Applied Voltage
i_{mtr}	=	Motor Current
L_{mtr}	=	Total inductance of the motor windings
R_{mtr}	=	Resistance in series with the motor
E_g	=	The internally generated voltage of the motor, proportional to the motor velocity

Since:

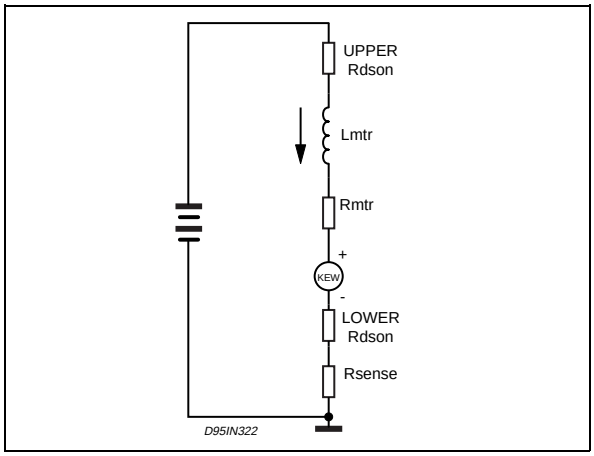
$$E_g = K_E\omega \qquad (5.1.3)$$

The above equations can be combined to form the basic electrical equation for a motor:

$$V = L_{mtr}\frac{di_{mtr}}{dt} R_{mtr}\, i_{mtr} + K_E\omega \qquad (5.1.4)$$

Figure 5.5 is a simplified electrical equivalent of the output stage of the L6238S along with the model of the motor during the time that the Output Drives are conducting.

Figure 5-5



The additional resistance associated with the output stage and sensing resistor are also in series with the motor. If we let R_s equal the total series resistence:

$$R_s = 2*R_{dsON} + R_{mtr} + R_{sense} \qquad (5.1.5)$$

then (5.1.4) becomes:

$$V = L_{mtr}\frac{di_{mtr}}{dt} R_s\, i_{mtr} + E_g \qquad (5.1.6)$$

Figure 5-6

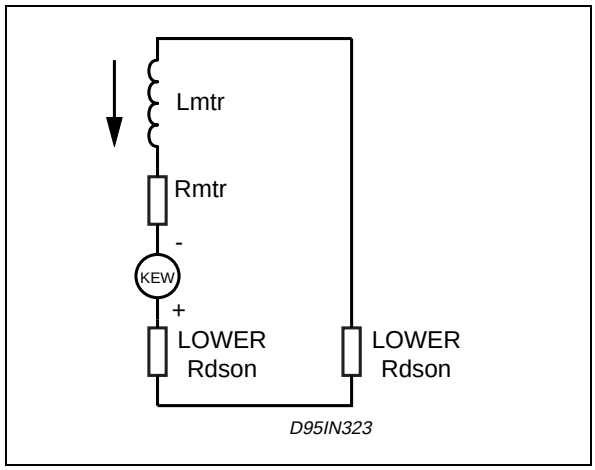


Figure 5-6 is an equivalent circuit of the output stage during the Constant-OFF period. During the OFF time the lower driver for the particular phase beign driven remains ON.

The internally generated voltage forces the path of current though the motor, its series resistance, the RdsON of the Lower Driver and finally through the opposite lower driver.

PWM Example (Refer to Figure 5-7)

The following is an example on how to select the timing parameters.

Given:

DCStart Current	=	1.25A
Ripple Current	=	100mA
Duty Cycle	=	50%
Motor Interface (L)	=	880µH
Total Series Resistance (R_S)	=	4.8Ω

If the worst case start current is 1.25A and the duty cycle is 50%, then the Peak Current, It will be:

$$i_t = 1.25 + \frac{0.1}{2}$$

$$i_t = 1.30A$$

The Valley current, I_b will thereforebe:

i_b = 1.30 - 0.1A

i_b = 1.20A

During the Align and Go Phase (where the power dissipation requirements are highest, Eg is zero. The initial time required to reach the Peak current is:

$$t_{init} = \frac{-L}{R} \ln\left(1 - \frac{I,R}{V}\right) \qquad (5.1.7)$$

Substituting values:

$$t_{init} = \frac{-880e-6}{4.8} \ln\left(1 - \frac{1.3 \cdot 4.8}{12}\right)$$

t_{init} = 134.6µs

The ON time can be calculated from:

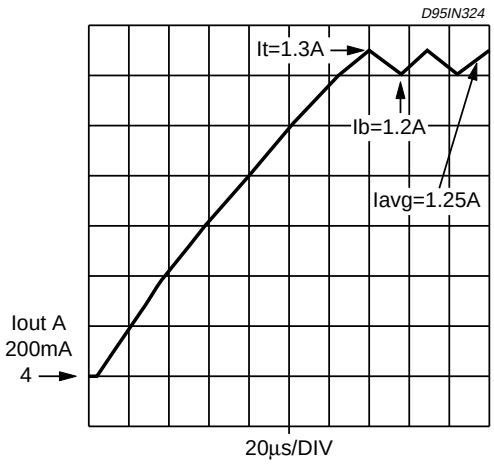
$$t_{on} = \frac{L}{R_s} \ln\left(\frac{\frac{V}{R_s} - i_b}{\frac{V}{R_s} - i_t}\right) \qquad (5.1.8)$$

Substituting values:

$$t_{on} = \frac{880E-6}{4.8} \ln\left(\frac{\frac{12}{4.8} - 1.2}{\frac{12}{4.8} - 1.3}\right)$$

t_{on} = 14.67µs

Figure 5-7



During the OFF time, the motor current continues to flow through the DMOS transistors and threfore the voltage drop remains constant across the windings.

The time required for the inductor current to reach the valley current is given by:

$$t_{off} = \frac{L}{R} \ln\left(\frac{I_t}{I_b}\right) \qquad (5.1.9)$$

Substituting values:

$$t_{off} = \frac{880e^{-6}}{4.8} \ln\left(\frac{1.3}{1.2}\right)$$

t_{off} = 14.67µs

Note: that the parameters for this example were selected to arrive at a 50% duty cycle. This will not always be the case due to factors such as fixed motor parameters, etc.

The Constant Off timer period can be determined from:

$$t_{off} = R_{slew} \cdot C_{off} \cdot \ln\left(\frac{V_{chrg}}{V_{trip}}\right) \qquad (5.1.10)$$

Where:

T_{off} = Constant-OFF Time

R_{slew} = Slew Rate Resistor

C_{off} = Off Time Capacitor

V_{chrg} = Initial Capacitor Charge Voltage

V_{trip} = Capacitor Lower Trip Threshold

Substituting nominal values given:

$T_{off} = 0.75 \cdot R_{slew} \cdot C_{off}$

Solving for C_{off}

$$C_{off} = \frac{T_{off}}{0.75 R_{slew}}$$

In the example, to set the OFF timer for a 50% duty cycle:

Given:

T_{off} = 14.67µs

R_{slew} = 100KΩ (typical Value)

$$C_{off} = \frac{14.67e^{-6}}{100e^{3}}$$

$C_{off} \approx$ 146pF

5.1.4 Minimum ON Time

The bandwidth of the PWM loop was optimized to reject unwanted switching noise while providing

sufficient response, commensurate with the switching speed of the output drivers. At higher frequencies the switching losses inherent in the drivers start to negative any of the power dissipation savings gained with PWM operation.

The current sense amplifier has a minimum slew rate of 0.31V/µs. With a worst case Motor peak start-up current of 2.5A and Sense Resistor of 0.33, the resultant R_{sense} voltage would be equal to 825mV. With a minimum gain of 3.8V/V, the CSA output voltage would have to slew to 3.14V. Therefore it would require approximately 10µs for the output voltage to reach the required commanded level.
If an ON time were selected that was less than this time, the motor current would overshoot the desired level resulting in incorrect current control possibly exceeding the output capabilities of the drivers.

5.1.5 Noise Blanking

Referring to Figure 5-8, when operating with lower levels of current (i.e. < 700mA, with Rsense = 0.33Ω), the possibility exiss where the noise due to output Turn-ON can exceed the Commanded Current Level causing prematire Turn-OFF.

In order to provide noise immunity from this switching noise, a blanking circuit automatically rejects any signal appearing at the output of the CSA for a 3µs period.

Figure 5-9 is an additional block diagram of the PWM control loop including the noise blanking circuit. The output of A3 goes high when ever the voltage at the CSA input is more positive then the Control Voltage.
This is the case when either the motor current or the turn-ON transient has reached the commanded level. The output of A3 is gates by N11. In order to provide a blanking period, Q1 is turned

Figure 5-8

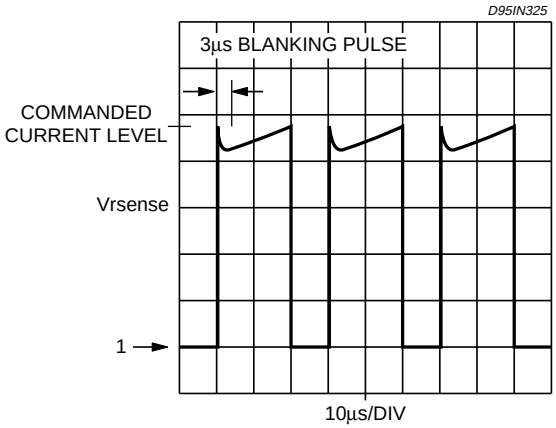
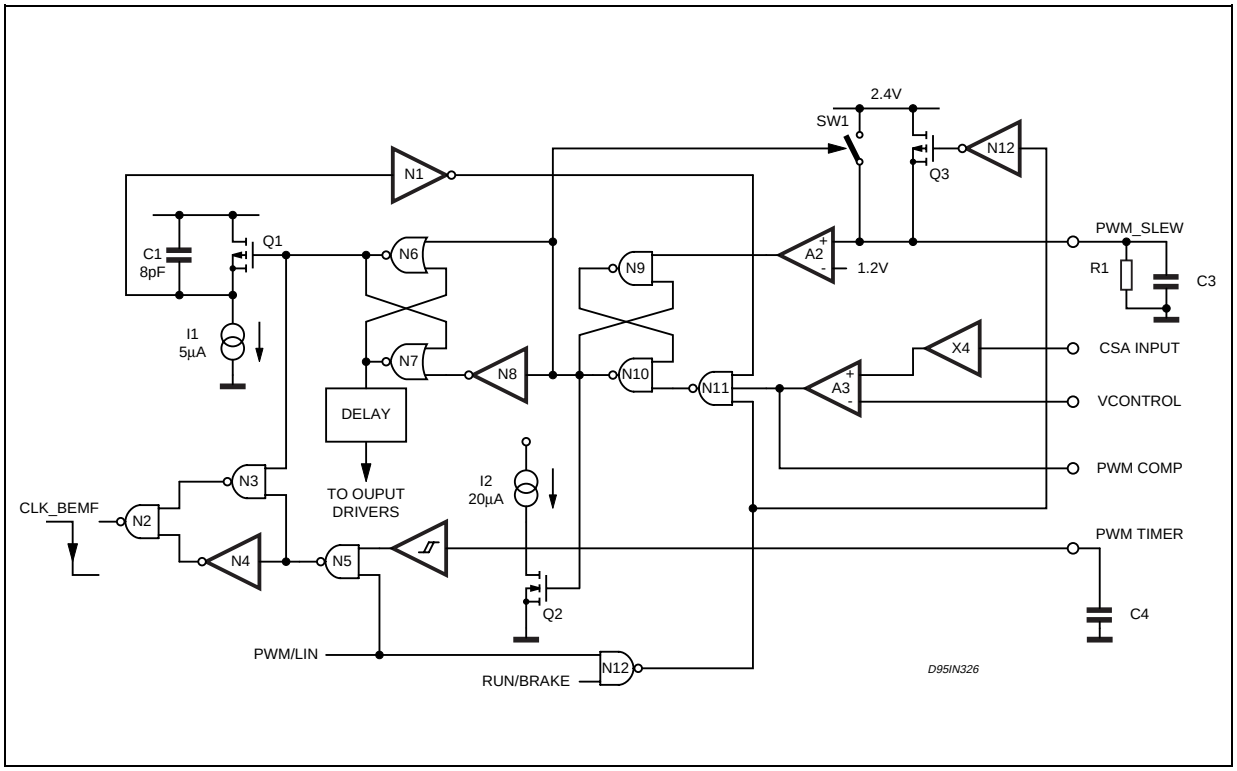


Figure 5-9



ON during the Constant-OFF time, charging C1 to the internal rail. At the end of the OFF time, Q1 is turned OFF allowing current source I1 to discharge the capacitor towards ground. While the voltage on C1 is above the low input threshold of N1, the output of N1 is low, preventing any change of state at the output of N11 due to a high A3 output. When the capacitor reaches the low input threshold of N1, N1 chnges state allowing A3 to control the state of N11.

5.1.6 Masking/Bemf Sampling in PWM

The method of sampling the floating phase for the bemf zero crossing defers between Linear and PWM operation. In Linear Mode, the bemf is sampled continuously after the mask time-out, until the zero crossing is detected. Then the mask is enabled for a time based on the commutation phase delay plus the additional time based on the previous period as explained earlier.

With PWM operation however, the switching noise at turn ON (after the Constant-OFF time) can be significant, especially at low RPMs where the bemf is the lowest. In order to provide the greatest noise immunity in PWM, the floating phase is monitored only at the point where the output is about to be turned OFF.

In operation, when the motor current reaches the commanded level, the floating phase is first monitored to determine if the bemf has crossed the zero. The output is then turned OFF for the Constant-OFF time out.

As the motor current increases through, the increasing bemf causes the motor current to naturally decrease. Eventually a point is reached where the PWM is running at 100% duty cycle and the motor current cannot reach the commanded level. At this time the bemf is no longer smpled, preventing further commutation of the output.

The PWM Limit Timer is used to set up a maximum ON time. When this limit is exceeded the method of sensing the bemf is essentially the same as in the case of operating in linear mode.

Figure 5-10 is an oscillograph of the controller operating in PWM mode. The top trace is A_{out}. The 2nd trace is the voltage seen at the PWM/SLEW pin indicating the exponential discharging of the timing capacitor during the OFF time. Trace 3 is the voltage appearing on the PWM Timer capacitor, while trace 4 is the motor current.

Referring again to Figure 5-9, and 5-10 transistor Q2 is turned ON at the beginning of the OFF time, discharging the external capacitor C4 to near ground level. At the end of the OFF-Time, Q2 is turned off and C4 starts charging linearly via I2. C4 is again discharged at the beginning of the OFF time and the cycle repeats. As long as C4 does not reach the threshold of A1 (typically 3.5V), the bemf is only sampled just before turn-off of the output. As the motor is starting up in figure 5-10, the duty cycle is roughly 50%. The PWM limit timer is reset to ground by the start of the OFF timer before reaching the 3.5V threshold.

In figure 5-11, as the motor spins up, the on time of the output increases and the PWM limit timer reaches the 3.5V. Eventually the duty cycle reaches 100% and the sampling of the bemf is essentially the same as in the linear mode.

The selection of components for the PWM timer is not critical. Since the objective is to sample the bemf only at turn OFF to maximize the signal to noise ratio, the PWM timer slope can be set up to convert to the full bemf sampling after a few revolutions of the motor when the bemf has reached an appropriate voltage output.

Figure 5-10

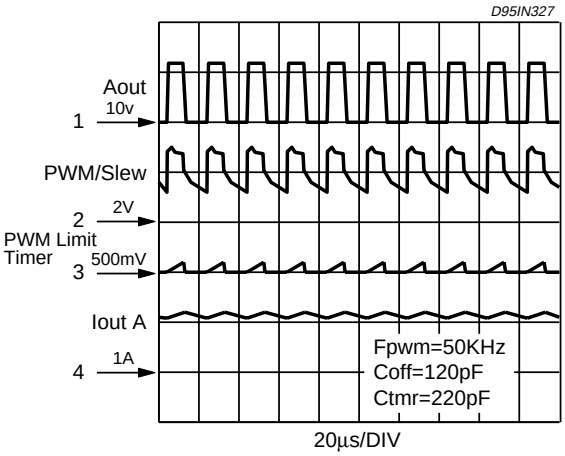
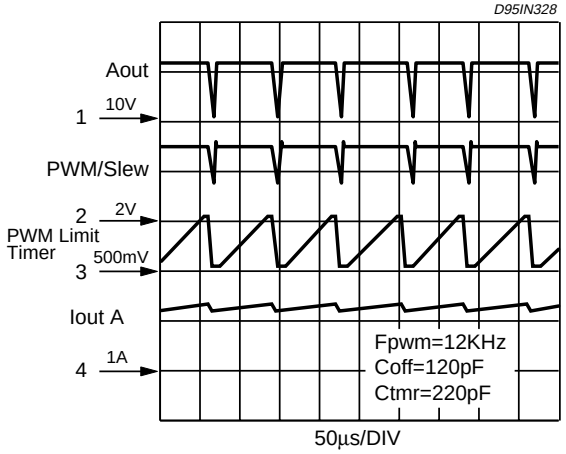
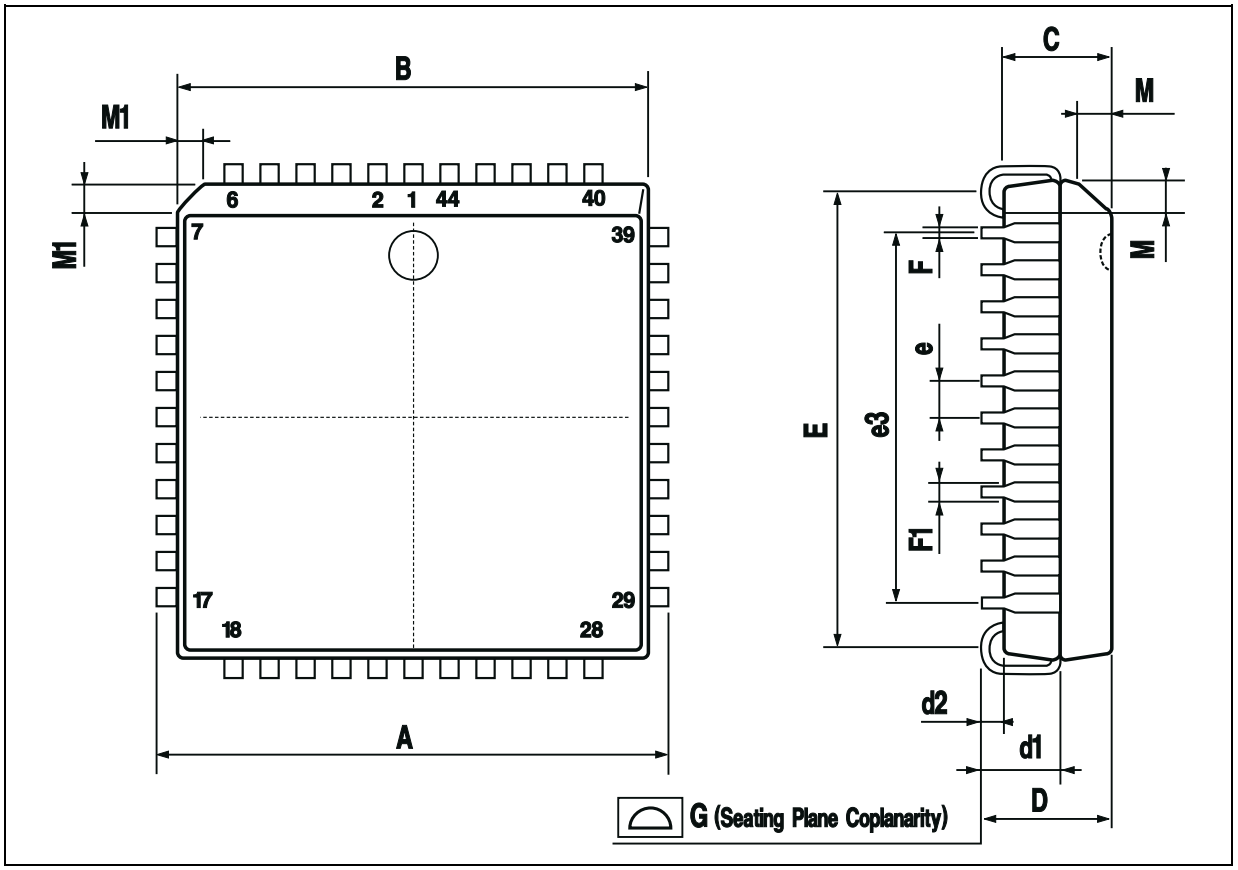


Figure 5-11



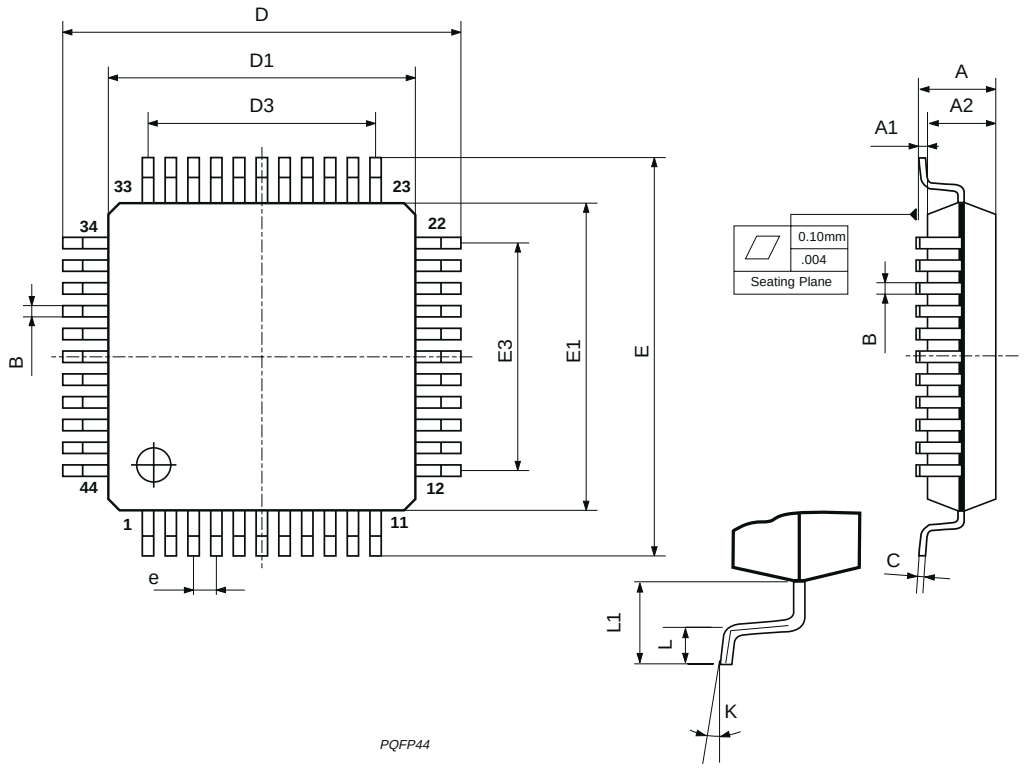
PLCC44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	



PQFP44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.40			0.134
A1	0.25			0.010		
A2	2.55	2.80	3.05	0.100	0.110	0.120
B	0.35		0.50	0.0138		0.0197
C	0.13		0.23	0.005		0.009
D	16.95	17.20	17.45	0.667	0.677	0.687
D1	13.90	14.00	14.10	0.547	0.551	0.555
D3		10.00			0.394	
e		1.00			0.039	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		10.00			0.394	
L	0.65	0.80	0.95	0.026	0.0315	0.0374
L1		1.60			0.063	
K	0°(min.), 7°(max.)					



TQFP64 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)